PRODUCT SPECIFICATION

CDTECH Model: **S150HWU01EP**

CUSTOMER Model: -

Description: **15.0 ” TFT-LCD Module**

Version: **1.0**

CDTECH	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2024.12.3	2024.12.3	2024.12.3

	SIGNATURE	DATE
CUSTOMER APPROVAL		

Record of Revisions

Version	Revise Date	Description	Page
1.0	2024-12-3	First Release	-

Contents

1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	15.0	inch
Number of Pixels	1920 (H) RGB x 720 (V)	pixels
Display Mode	Normally Black	-
Viewing Direction	Free	-
Interface	LVDS	-
Display Colors	16.7M	colors
Outline Dimension	369.96 (H) x 146.96 (V) x 6.43 (D)	mm
Active Area	355.68 (H) x 133.38 (V)	mm
Pixel Pitch	0.1852 (H) x 0.1852 (V)	mm
Driver IC	HX82102-A00DPD200-A-P	-
Operation Temperature	-20~70	℃
Storage Temperature	-30~80	℃

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Analog Supply voltage	VDD	-0.3	5.0	V	Note 1

Note 1:Permanent damage may occur to the LCD module if beyond this specification.
Functional operation should be restricted to the conditions described under normal operating conditions.

3. Elecrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

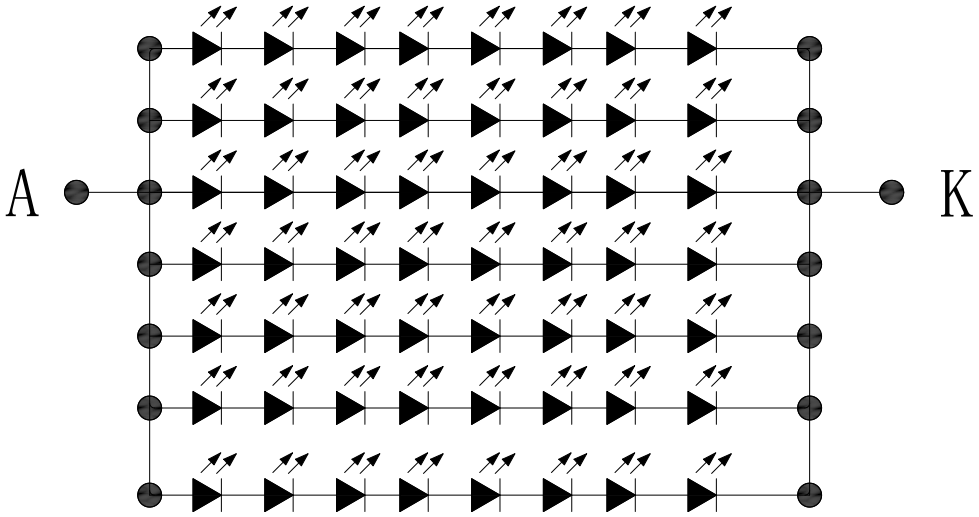
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Supply voltage	VDD	3.0	3.3	3.6	V	
Analog supply current	I_{VDD}	-	TBD	-	mA	VDD=3.3V
Logic input voltage	VIH	0.7*VDD	-	VDD	V	
	VIL	GND	-	0.3*VDD	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I_F	-	420	-	mA	
Driving Voltage	V_F	21.6	-	27.2	V	
Power consumption	W_{BL}	9.072	-	11.424	W	
LED Life-Time	N/A	-	30,000	-	Hours	Ta=25℃ Note 1

Note 1:LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :



4. Interface Pin Assignment

4.1 LCM Pin Assignment

No.	Symbol	Description
1	NC	No connection
2-3	GND	Ground
4	CSB(NC)	No connection
5	SCL(NC)	No connection
6	SDA(NC)	No connection
7	RESET	Global reset pin
8	STBYB	STBYB = L, timing controller, sourcedriver will turn off STBYB = H, normal operation (Default)
9-10	VDD	supply voltage
11-12	GND	Ground
13	OLVD3P	+ LVDS differential data input
14	OLVD3N	- LVDS differential data input
15	GND	Ground
16	OLVD2P	+ LVDS differential data input
17	OLVD2N	- LVDS differential data input
18	GND	Ground
19	OLVDCLKP	+ CLKP differential clock input
20	OLVDCLKN	- CLKN differential clock input
21	GND	Ground
22	OLVD1P	+ LVDS differential data input
23	OLVD1N	- LVDS differential data input
24	GND	Ground
25	OLVD0P	+ LVDS differential data input
26	OLVD0N	- LVDS differential data input
27-28	GND	Ground
29	FAIL_DET(NC)	No connection
30-31	VDD	supply voltage
32	ATREN(NC)	No connection
33	VDD_OTP(NC)	No connection
34	NC	No connection
35-36	GND	Ground

37	NC	No connection
38	NC	No connection
39	NC	No connection
40	NC	No connection
41	LEDA1(NC)	No connection
42	LEDA2(NC)	No connection
43	LEDA3(NC)	No connection
44	LEDA4(NC)	No connection
45	NC	No connection
46	LEDK1(NC)	No connection
47	LEDK2(NC)	No connection
48	LEDK3(NC)	No connection
49	LEDK4(NC)	No connection
50	NC	No connection

5. Interface Characteristics

5.1 Power on/off sequence

A. If VSP and VSN are generated by PFM circuits and PWR_SPEED=1:

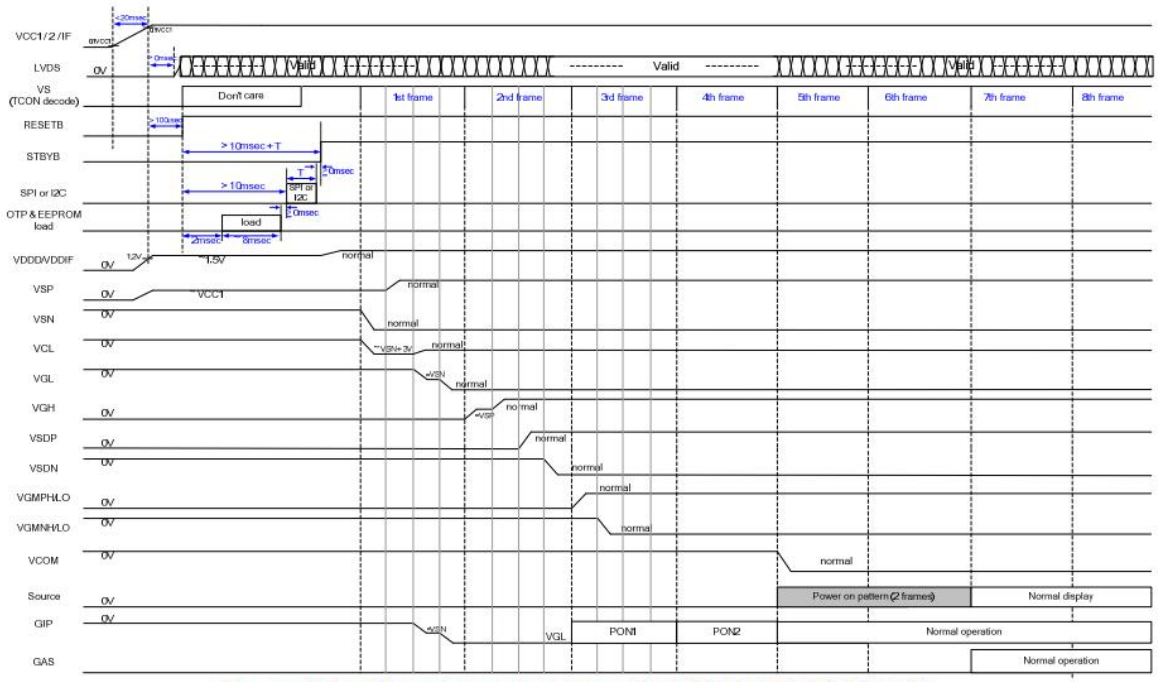


Figure 6-13: Power-on sequence with PFM(PWR_SPEED=1)

B. If VSP and VSN are generated by PFM circuits and PWR_SPEED=0:

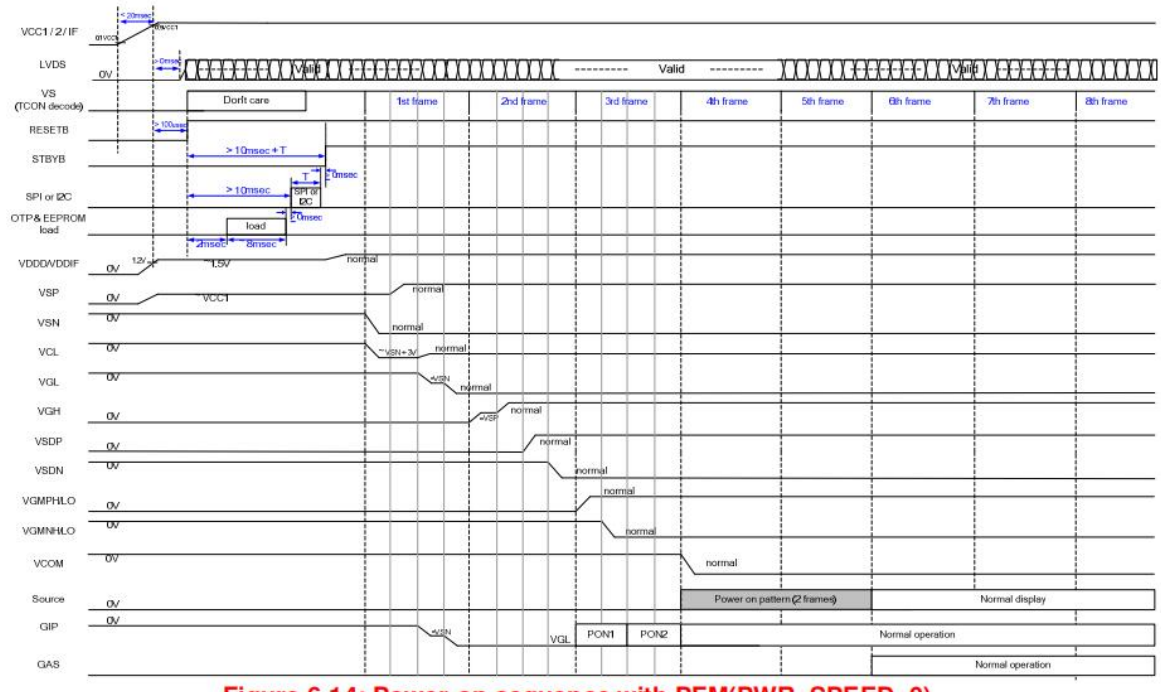


Figure 6-14: Power-on sequence with PFM(PWR_SPEED=0)

C. VSP=VSDP and VSN=VSDN by external power supply, VGH and VGL generated by internal charge pump circuits (PWR_SPEED=1)

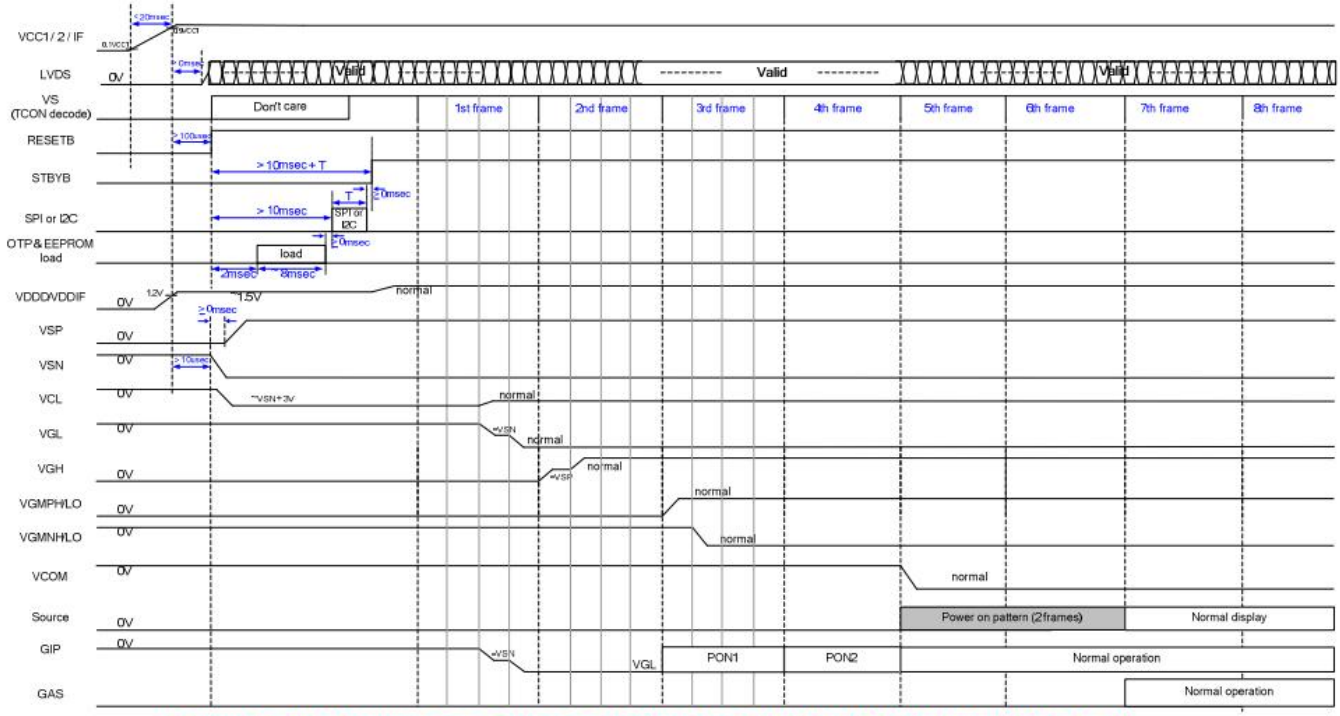


Figure 6-15: Power-on sequence withexternal VSP/VSN (PWR_SPEED=1)

D. VSP=VSDP and VSN=VSDN by external power supply, VGH and VGL generated by internal charge pump circuits (PWR_SPEED=0)

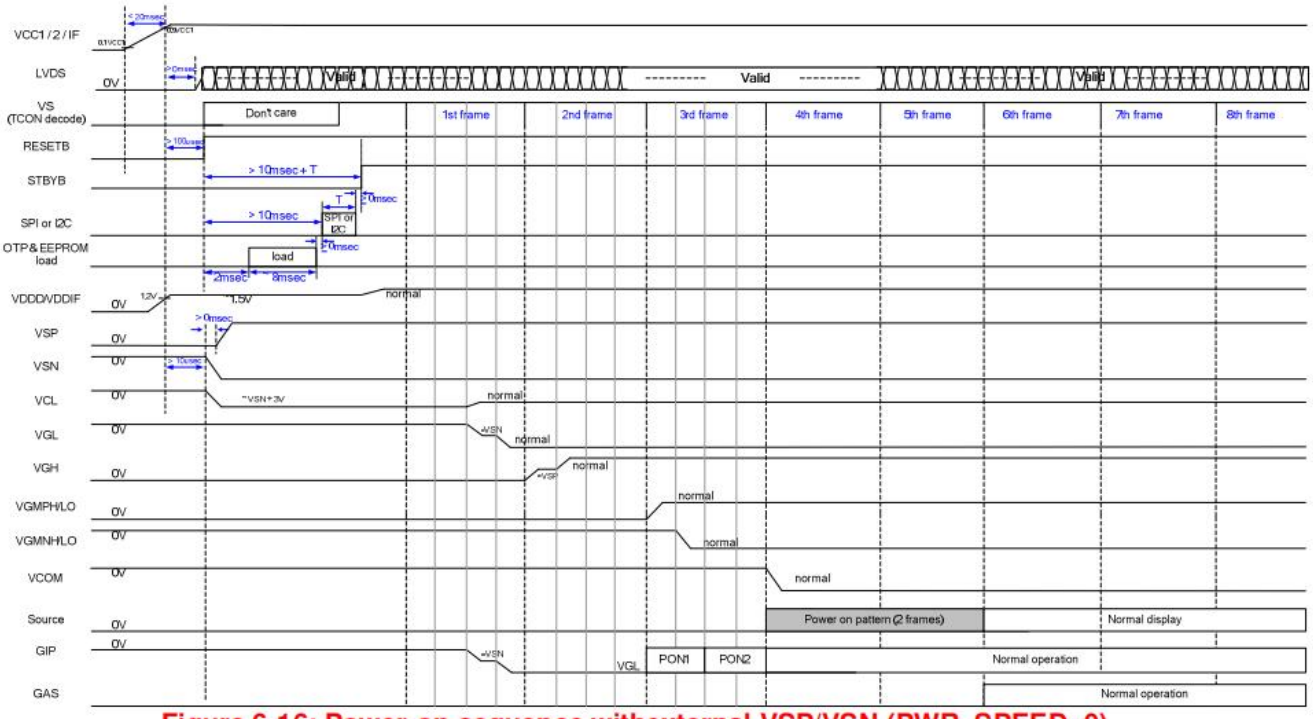


Figure 6-16: Power-on sequence withexternal VSP/VSN (PWR_SPEED=0)

E. VSP=VSDP and VSN=VSDN by external power supply, and VGH and VGL by external power supply (PWR_SPEED=1)

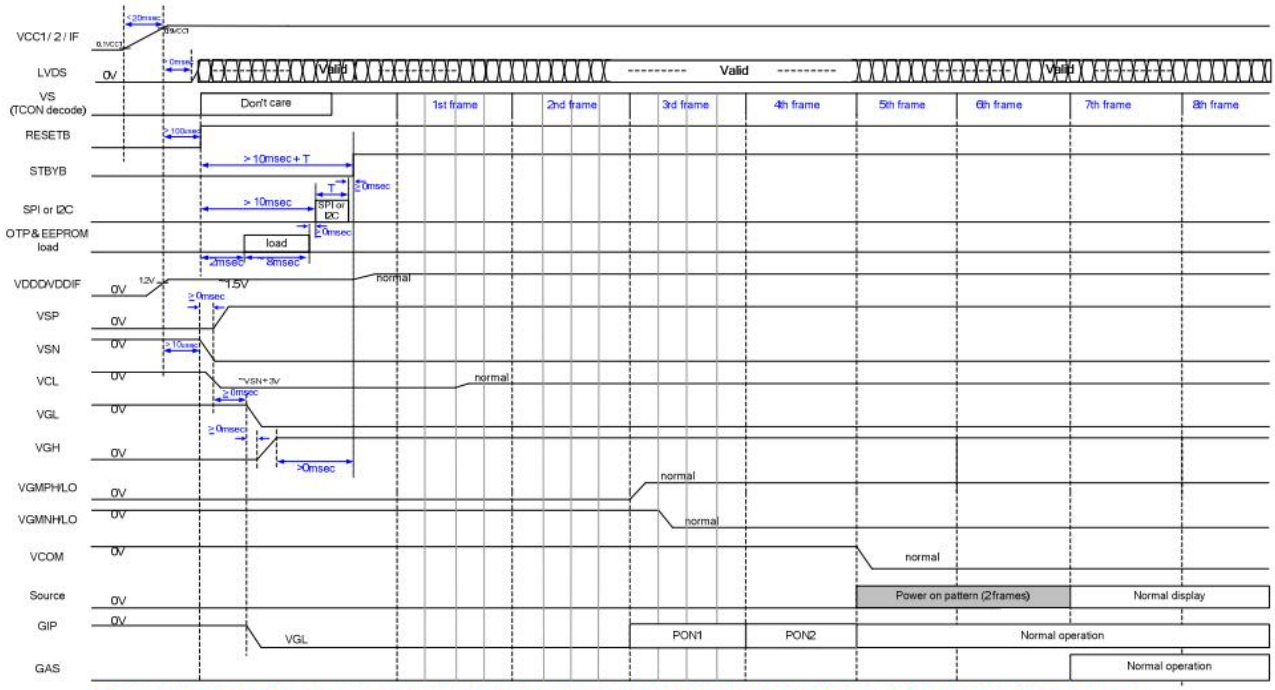


Figure 6-17: Power-on sequence with external VSP/VSN/VGH/VGL (PWR_SPEED=1)

F. VSP=VSDP and VSN=VSDN by external power supply, and VGH and VGL by external power supply (PWR_SPEED=0)

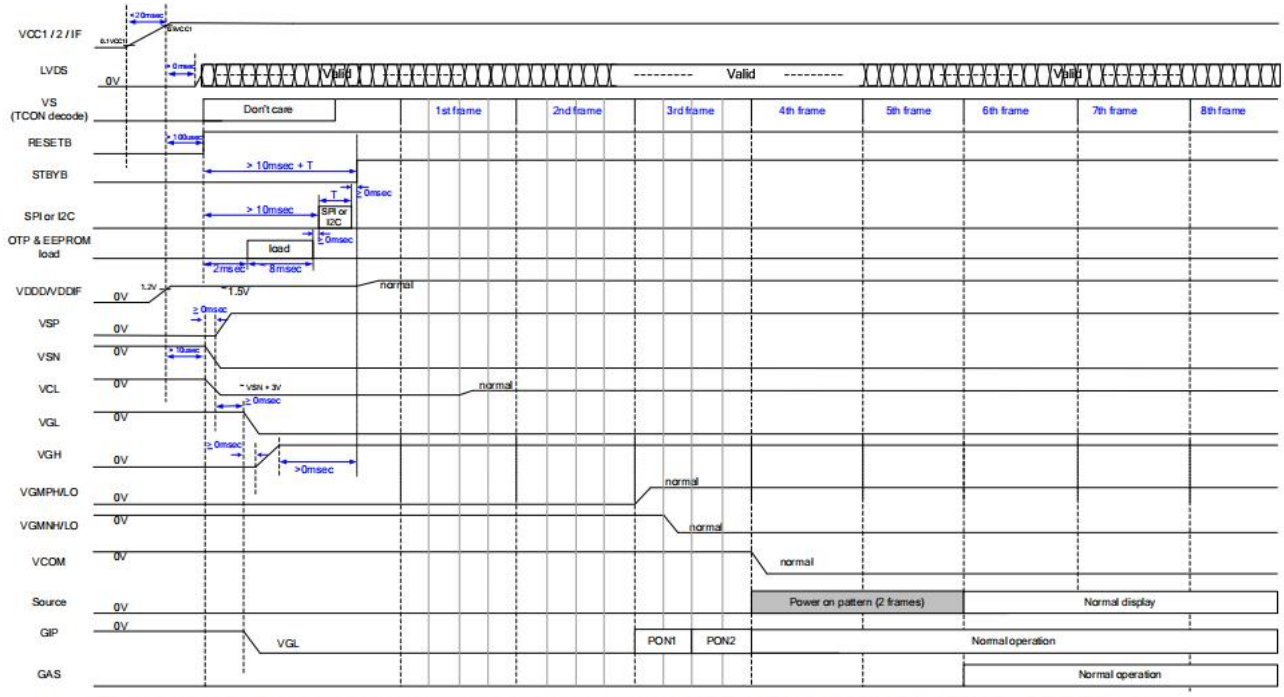


Figure 6-18: Power-on sequence with external VSP/VSN/VGH/VGL (PWR_SPEED=0)

A. If VSP and VSN are generated by PFM circuits:

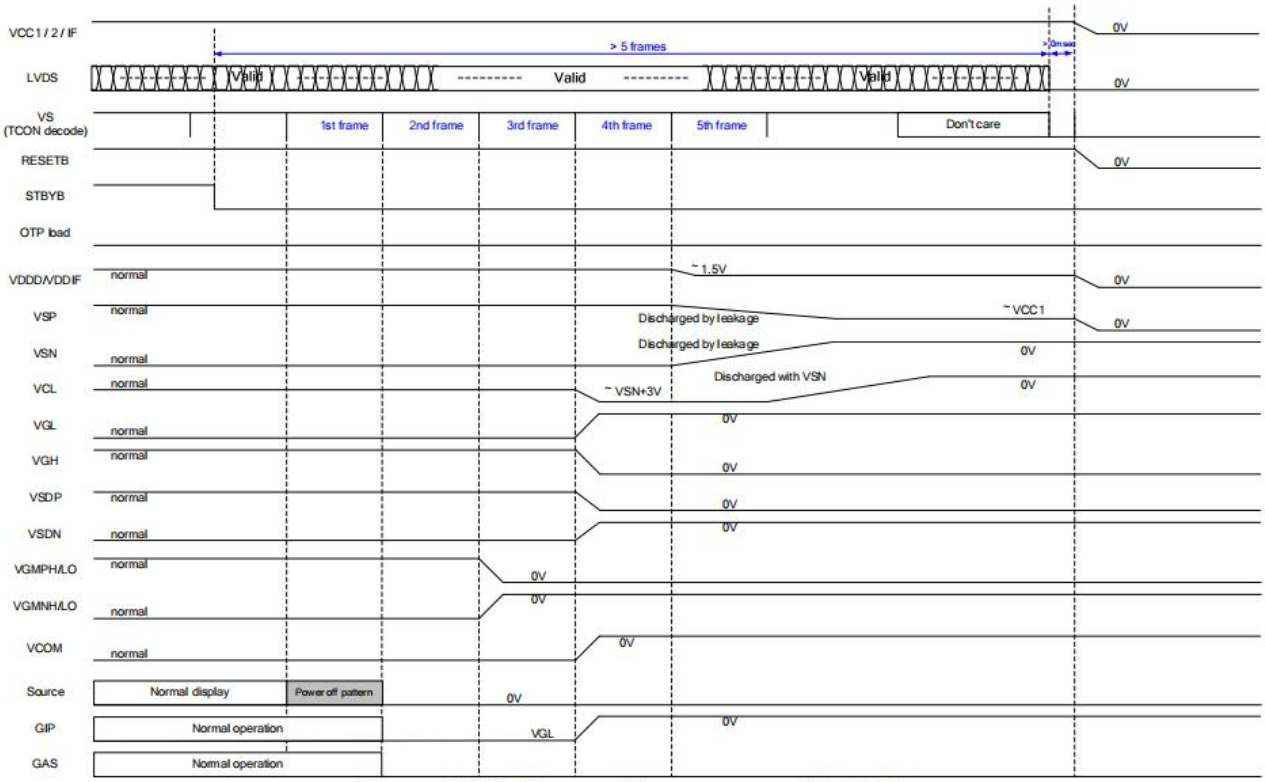


Figure 6-19: Power-off sequence with PFM

B. If VSP=VSDP and VSN=VSDN by external power supply, VGH and VGL generated by internal charge pump circuits:

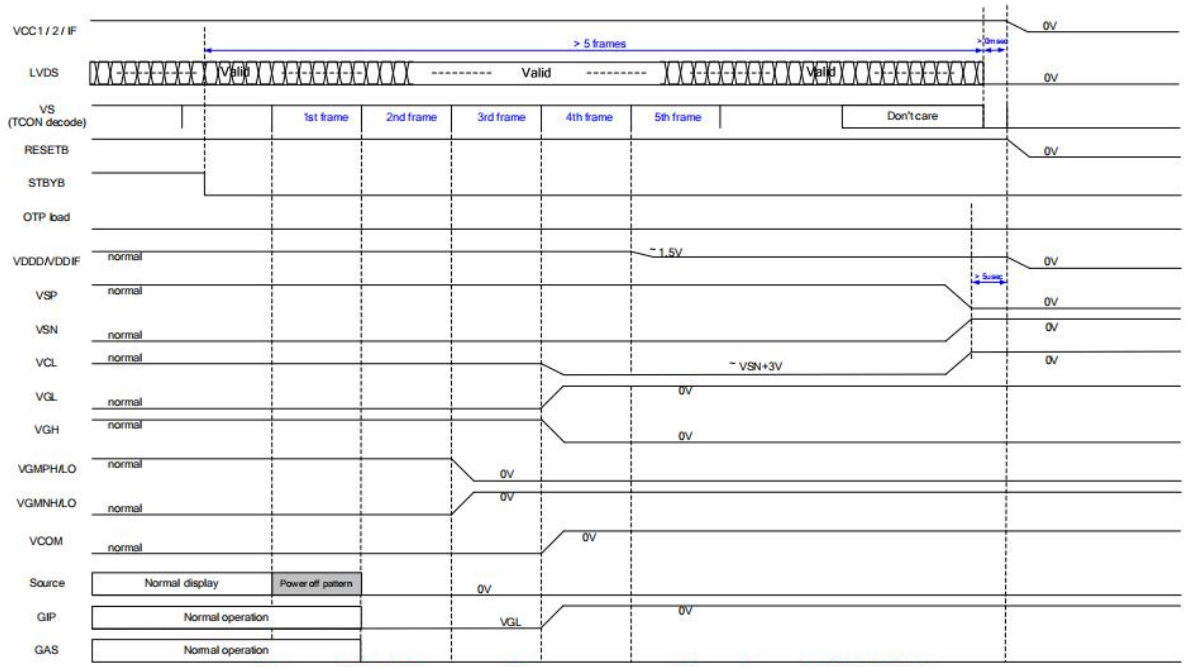


Figure 6-20: Power-off sequence with external VSP/VSN

C. If VSP=VSDP and VSN=VSDN by external power supply, and VGH and VGL generated by external power supply:

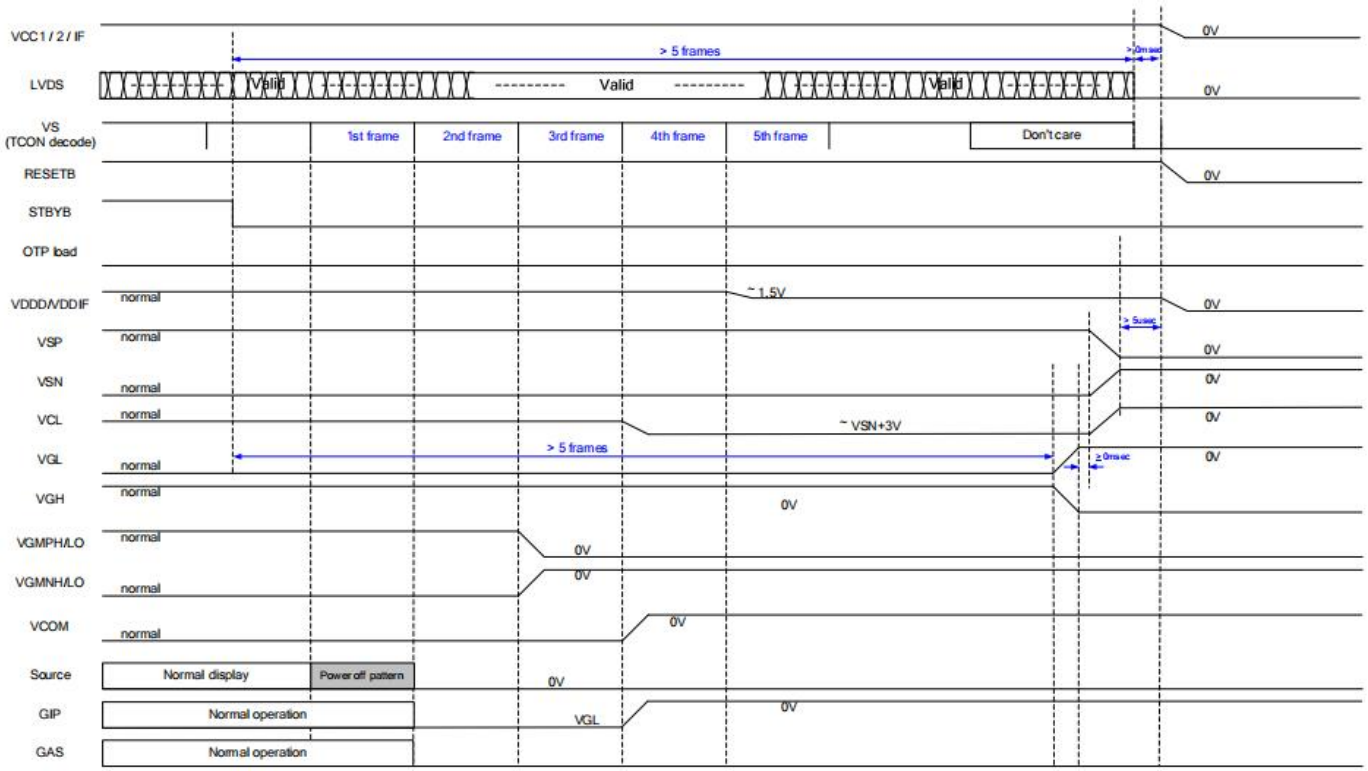


Figure 6-21: Power-off sequence with external VSP/VSN/VGH/VGL

5.2 PFM setting parameter

In HX82102-A-LT, PFM applies different settings to the power on sequence. Below table is the parameter setting for PFM soft start and normal mode.

	Soft Start	Normal
PFM parameter	VSPON_SS1[3:0] VSNON_SS1[3:0] VSPOFF_SS1[3:0] VSNOFF_SS1[3:0] VSPON_SS2[3:0] VSNON_SS2[3:0] VSPOFF_SS2[3:0] VSNOFF_SS2[3:0]	VSPON[4:0] VSNON[4:0] VSPOFF[3:0] VSNOFF[3:0]

Note: (1) VSPON_SS1 / VSPOFF_SS1 (Page1_R14h)
(2) VSNON_SS1 / VSNOFF_SS1 (Page1_R15h)
(3) VSPON_SS2 / VSPOFF_SS2 (Page1_R0Ah)
(4) VSNON_SS2 / VSNOFF_SS2 (Page1_R0Bh)
(5) VSPON / VSPOFF (Page1_R08h/ Page1_R06h[7])
(6) VSNON / VSNOFF (Page1_R09h/ Page1_R06h[6])

Table 6.3: PFM setting parameter

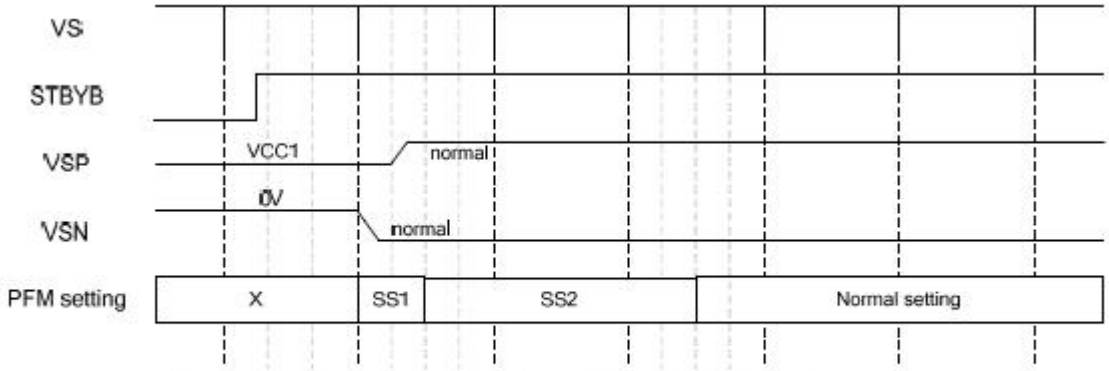


Figure 6-22: PFM power on setting(PFM_SS_SEL=0)

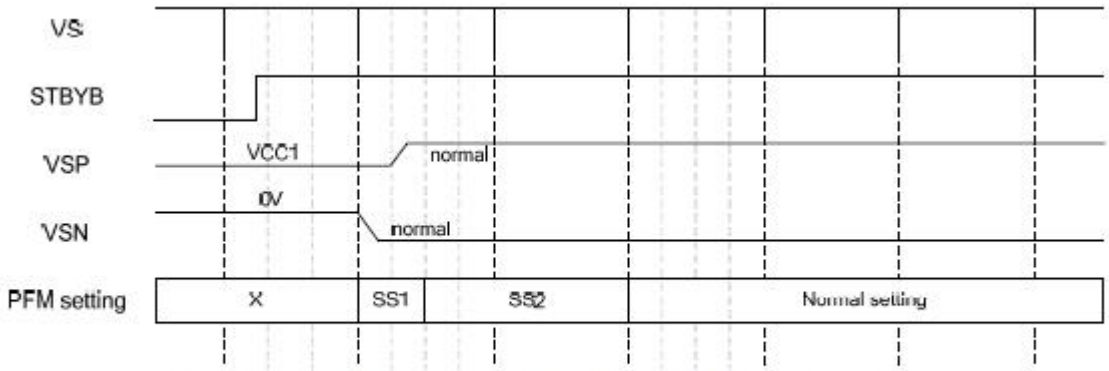


Figure 6-23: PFM power on setting(PFM_SS_SEL=1)

5.3 LVDS mode AC electrical characteristics

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_{OP}=-40~105℃)

Parameter	Symbol	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Clock frequency (1-port/2-port)	F_{LVCYC}	15	-	110/105	MHz
Clock period (1-port/2-port)	T_{LVCYC}	9.09/9.52	-	-	ns
1 data bit time	UI	-	1/7	-	T_{LVCYC}
Clock high time	T_{LVCH}	-	4	-	UI
Clock low time	T_{LVCL}	-	3	-	UI
Position 1	T_{POS1}	-0.2	0	0.2	UI
Position 0	T_{POS0}	0.8	1	1.2	UI
Position 6	T_{POS6}	1.8	2	2.2	UI
Position 5	T_{POS5}	2.8	3	3.2	UI
Position 4	T_{POS4}	3.8	4	4.2	UI
Position 3	T_{POS3}	4.8	5	5.2	UI
Position 2	T_{POS2}	5.8	6	6.2	UI
Input eye width	T_{EYEW}	0.6	-	-	UI
Input eye border	T_{EX}	-	-	0.2	UI
LVDS wake up time	T_{ENLVDS}	-	-	150	us
LVDS port to port skew	T_{skew_EO}	-1		1	UI

Table 9.2: LVDS mode AC electrical characteristics

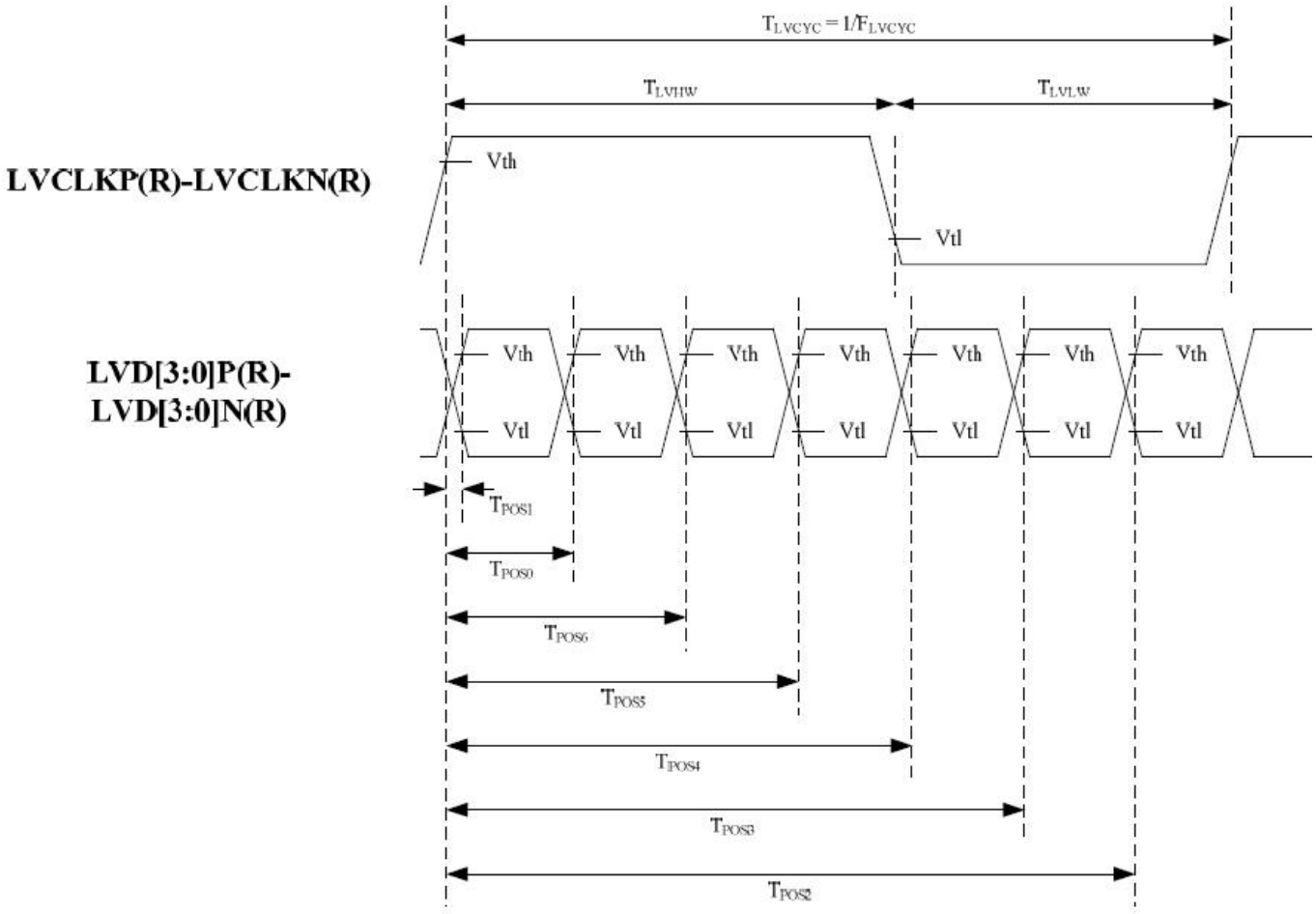
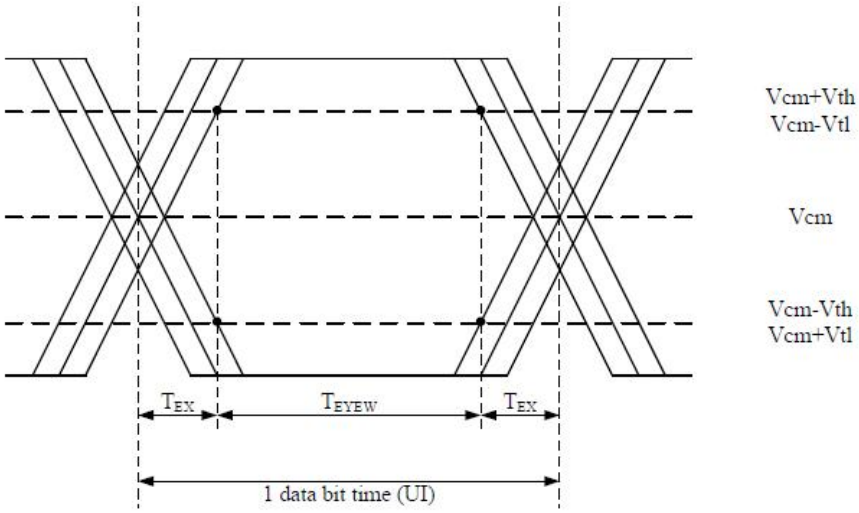


Figure 9-2: LVDS input timing

Single-ended:
LVD[3:0]P,
LVD[3:0]N



Differential:
LVD[3:0]P-LVD[3:0]N

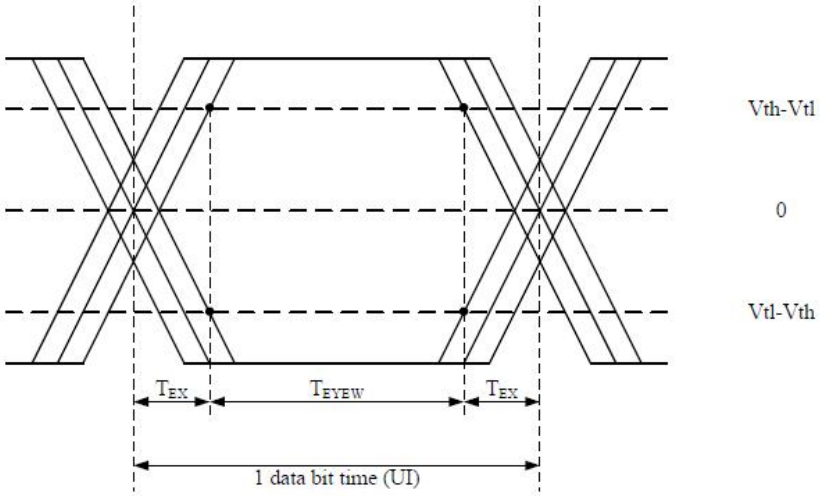


Figure 9-3: LVDS input eye diagram

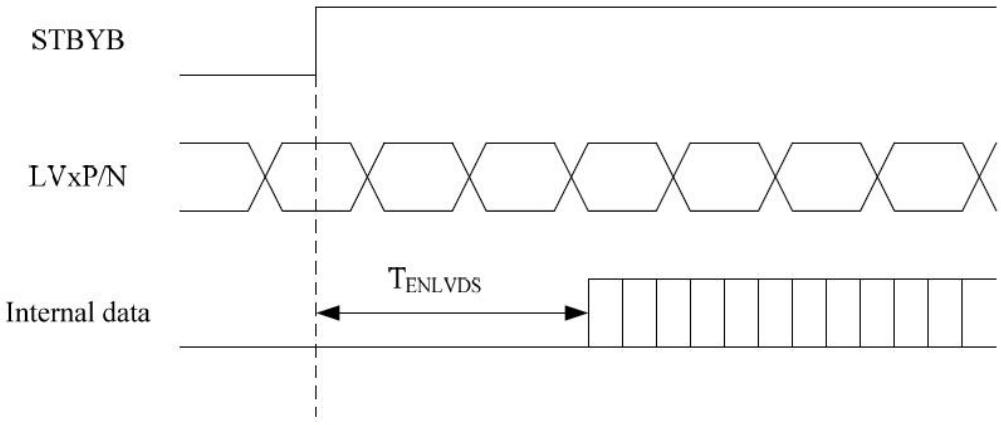


Figure 9-4: LVDS wake up time

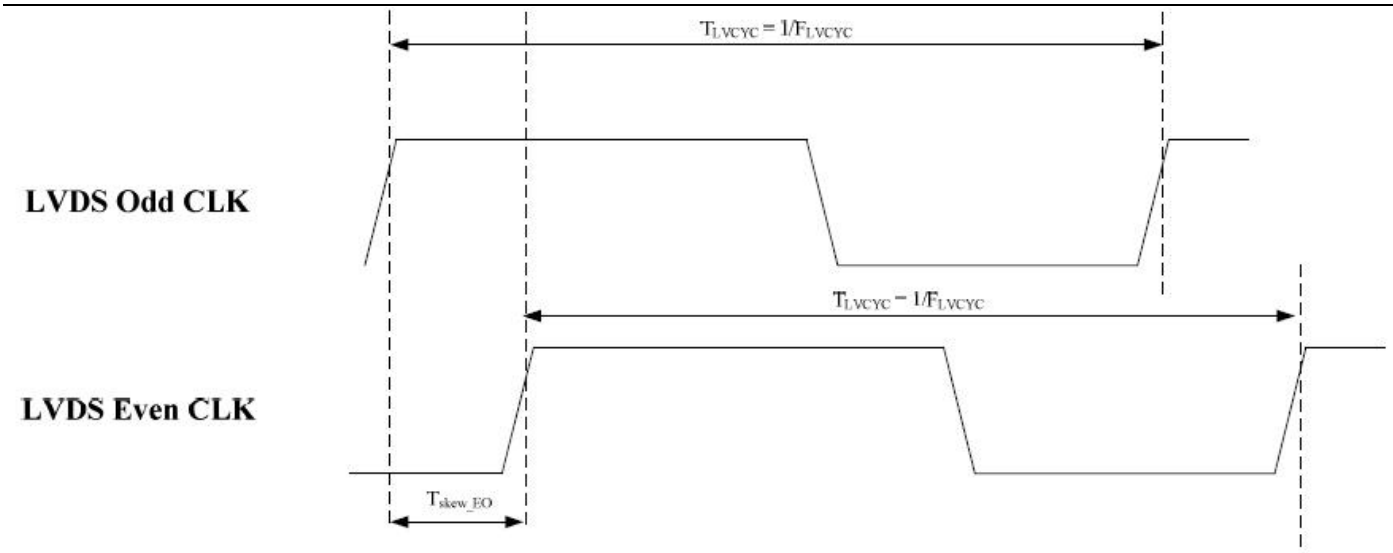


Figure 9-5: LVDS clock to clock skew

LVDS with SSC
The LVDS receiver can support spread spectrum clock (SSC) .Limitation is listed as below.

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Modulation Frequency	SSC_{MF}	LVDS clock frequency center at 110MHz	-	-	200	KHz
		LVDS clock frequency center at 80MHz	-	-	200	KHz
		LVDS clock frequency center at 60MHz	-	-	150	KHz
		LVDS clock frequency center at 40MHz	-	-	100	KHz
		LVDS clock frequency center at 20MHz	-	-	100	KHz
		LVDS clock frequency center at 15MHz	-	-	100	KHz
Modulation Rate	SSC_{MR}	LVDS clock frequency + SSCMR in the range of 15MHZ~105Mhz	-	-	±3	%

Table 9.3: SSC limitation of LVDS interface

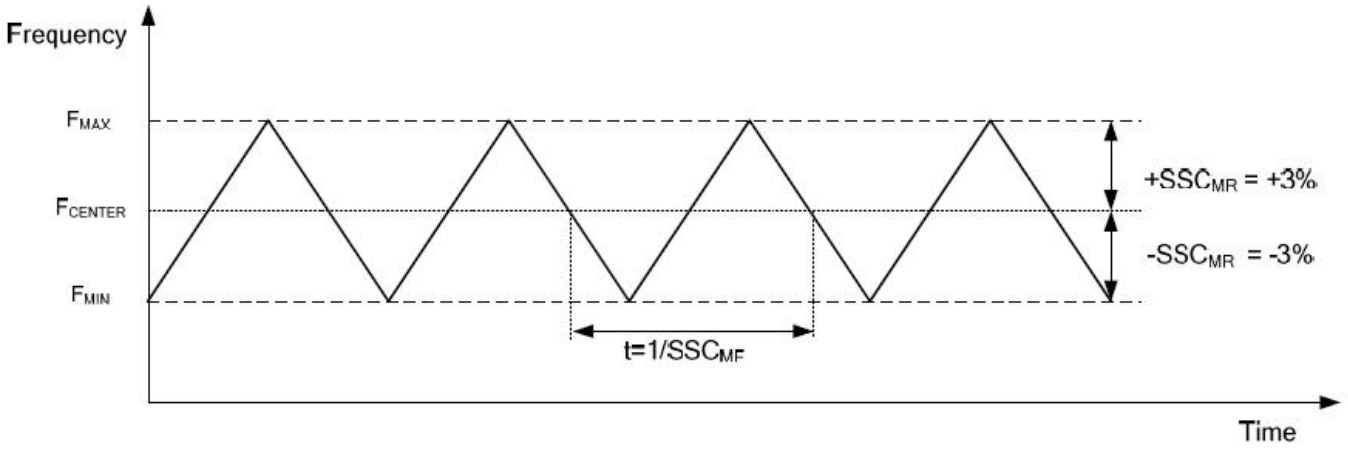


Figure 9-6: SSC figure

5.4 Reset timing

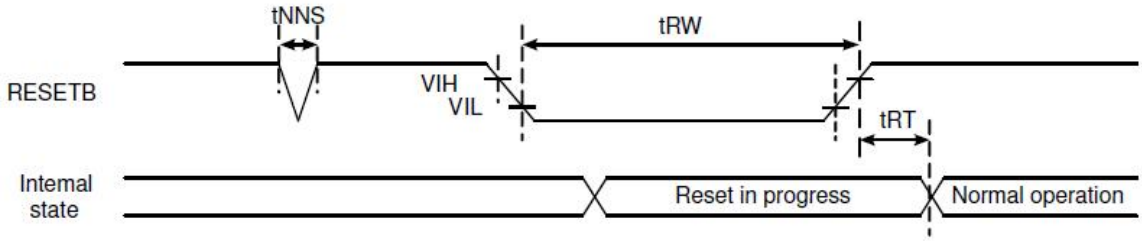


Figure 9-7: Reset timing

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_{OP}=-40~105℃)

Signal	Paramete	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
RESETB	Reset pulse width	tRW	10	-	-	μs
	Reset complete time	tRT	-	-	5	μs
	Negative spike noise width	tNNS	-	-	100	ns

Table 9.4: Reset timing parameter

5.5 Display interface

5.5.1 8bit LVDS interface

For 1-port LVDS 8-bit mode with VESA format, only the odd port (with OLVxxx pins) is used.

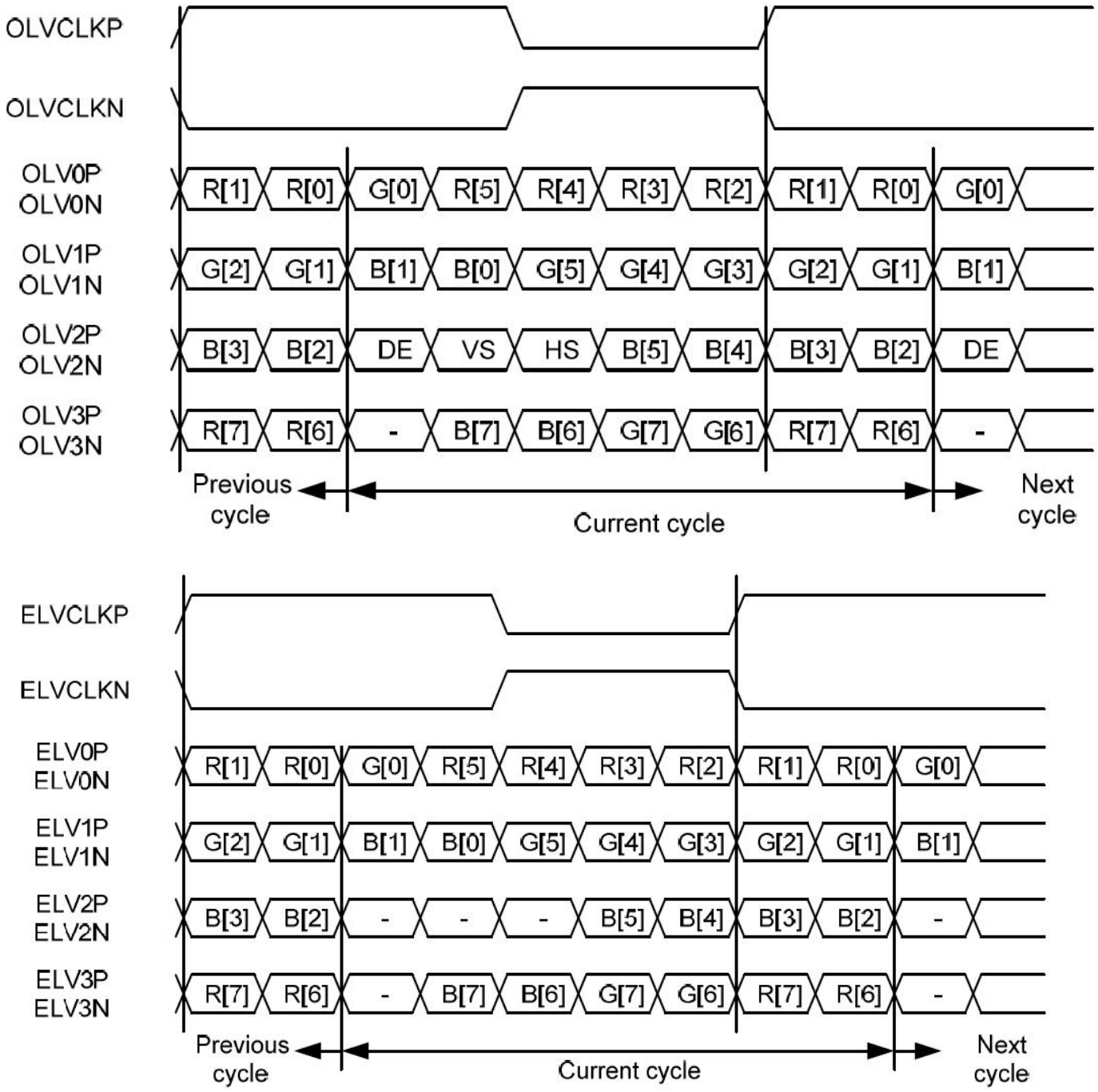


Figure 6-5: 2-port LVDS signals, VESA format (8-bit)

For 1-port LVDS 8-bit mode with JEIDA format, only the odd port (with OLVxxx pins) is used.

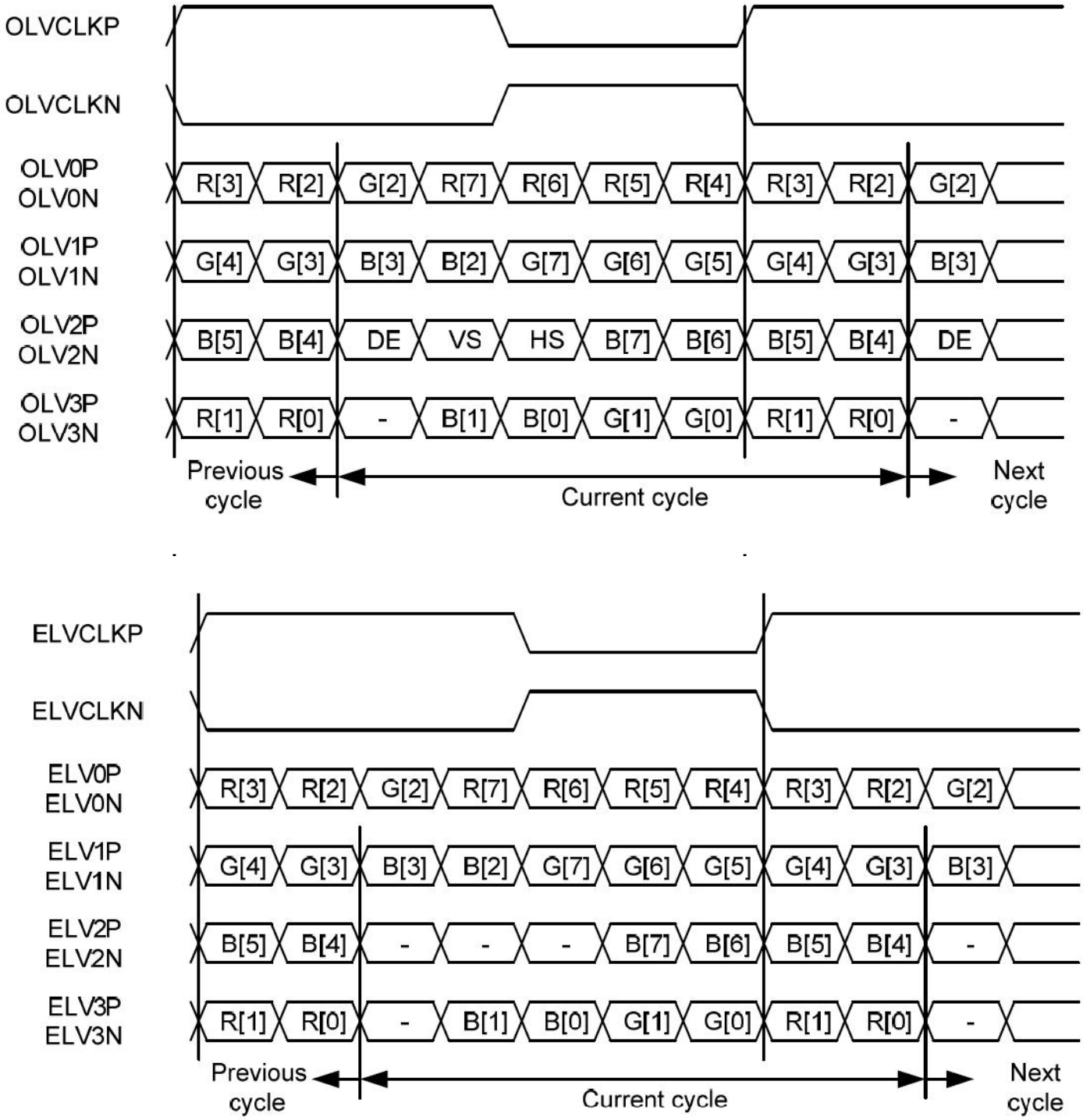


Figure 6-6: 2-port LVDS signals, JEIDA format (8-bit)

5.5.2 6bit LVDS interface

For 1-port LVDS 6-bit mode with VESA format, only the odd port (with OLVxxx pins) is used.

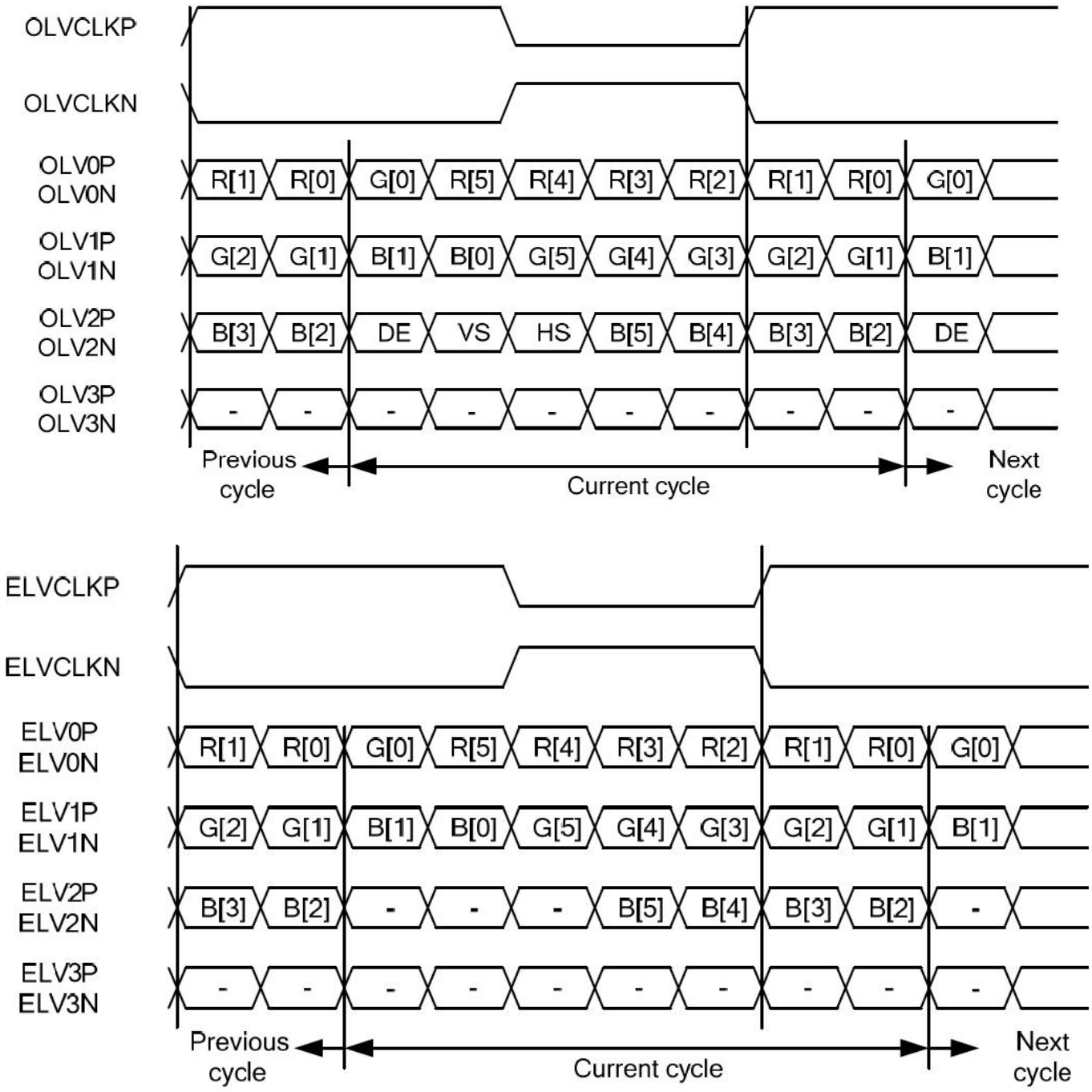


Figure 6-7: 2-port LVDS signals, VESA format (6-bit)

5.5.3 Parallel RGB with Sync mode at LVDS interface

- Horizontal

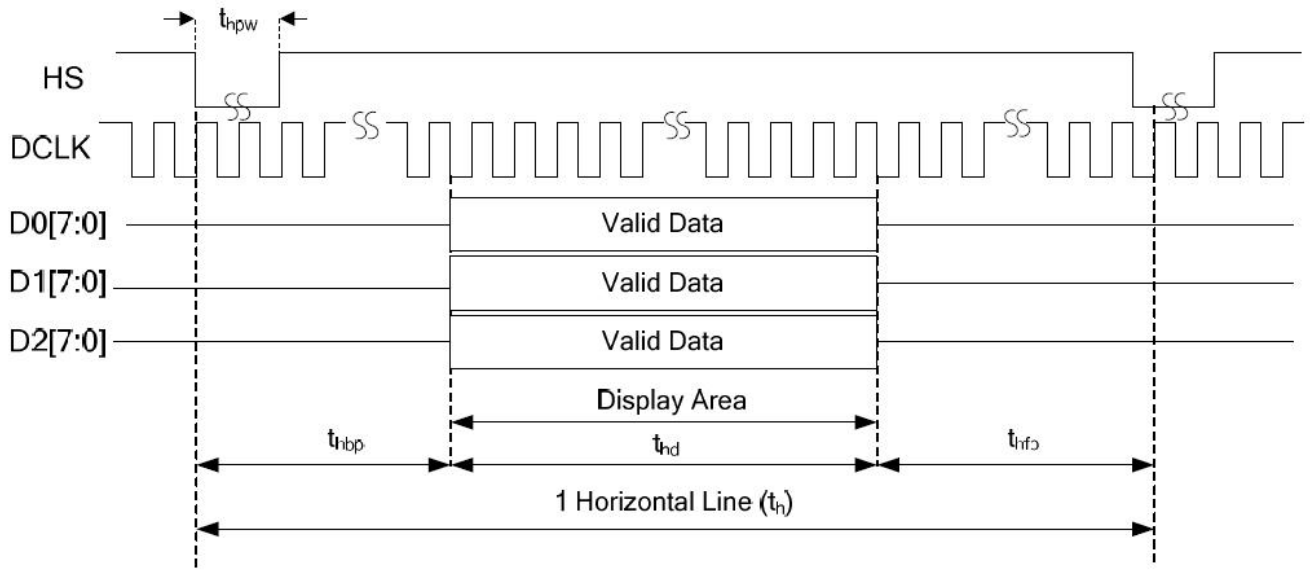


Figure 6-8: Horizontal input timing at Sync mode

- Vertical

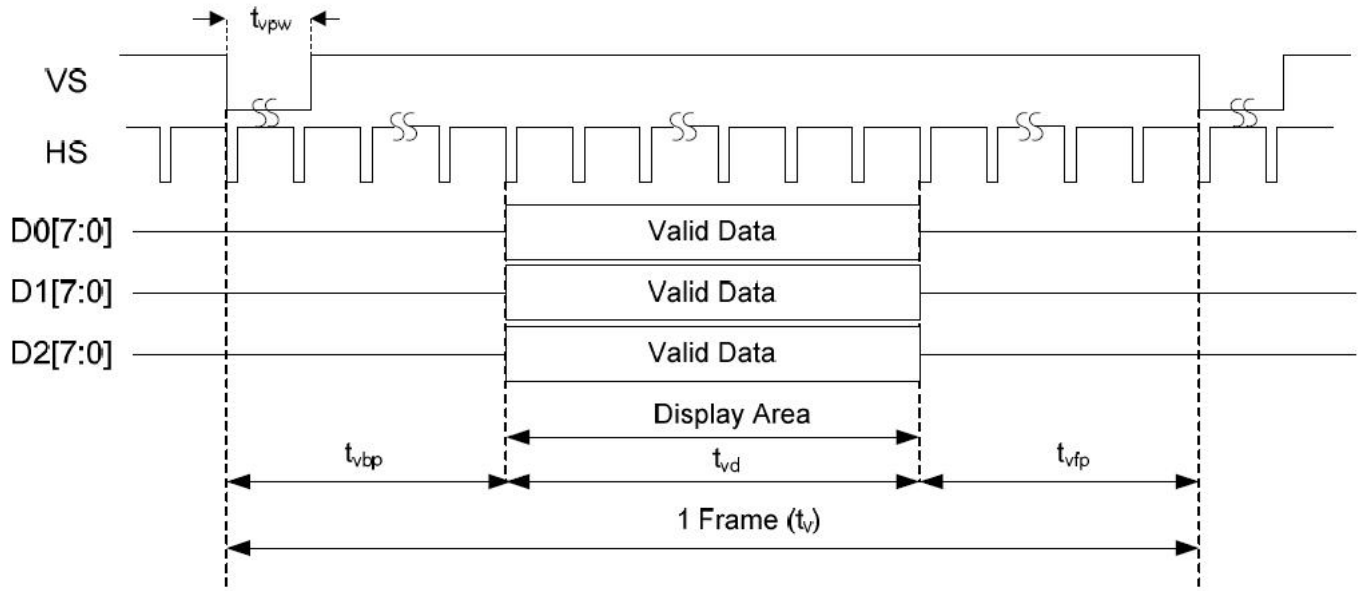


Figure 6-9: Vertical input timing at Sync mode

Parameter	Symbol	Panel Resolution									Unit
		2560xRGBx960 (Two Port)			1920xRGBx1080 (Two Port)			1920xRGBx720 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}		78.82			67.47			87.7		MHz
Horizontal valid data	t_{hd}		1280			960			1920		DCLK
Hsync pulse width	t_{hpw}	10	12		10	12		10	12		DCLK
Hsync back porch	t_{hbp}	5	16		5	16		5	16		DCLK
Hsync front porch	t_{hfp}	50	50		50	50		50	50		DCLK
1 horizontal line	t_h	1335	1346	1664	1015	1026	1248	1975	1986	2496	DCLK
Vertical valid data	t_{vd}		960			1080			720		H
Vsync pulse width	t_{vpw}	1	3		1	3		1	3		H
Vsync back porch	t_{vbp}	4	8		4	8		4	8		H
Vsync front porch	t_{vfp}	6	8		6	8		6	8		H
1 vertical field	t_v	970	976	1010	1090	1096	1134	730	736	756	H
Frame rate	FR		60			60			60		Hz

5.5.4 Parallel RGB with DE only mode at LVDS interface

It just needs DE signal only, when DE only mode enable.

- Horizontal

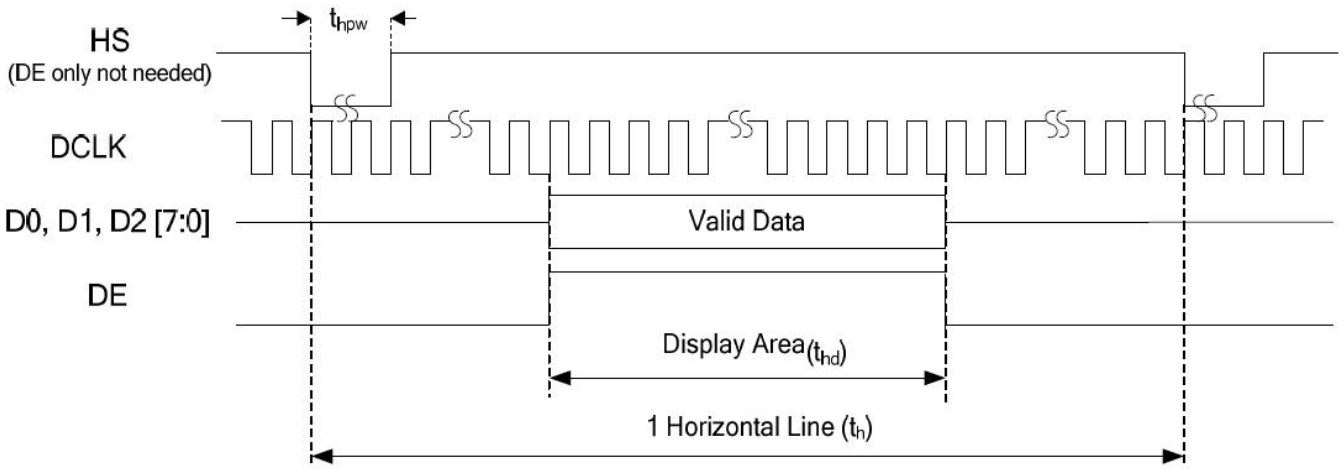


Figure 6-10: Horizontal input timing at DE only mode

• Vertical

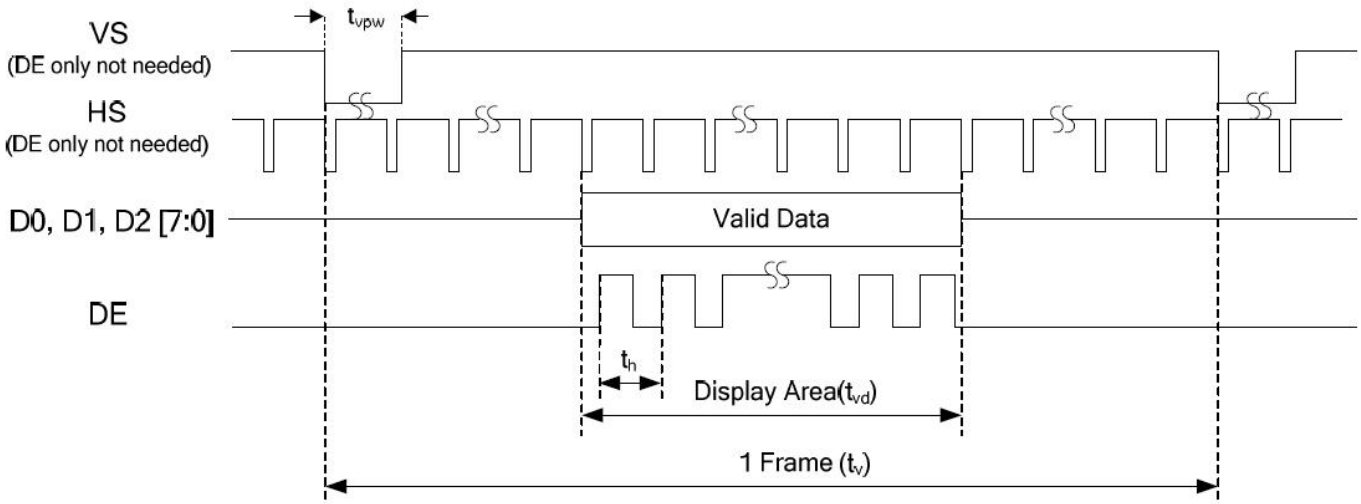
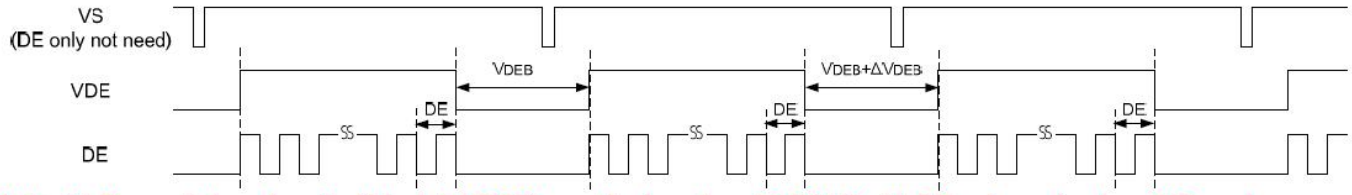


Figure 6-11: Vertical input timing at DE only mode



Note: (1) The variation of vertical blank (**ΔVDEB**) must be less than 50 DCLK with DE only mode when GIP mode (**GDSEL=0**) is used.

Figure 6-12: Vertical variation timing at DE only mode

Parameter	Symbol	Panel Resolution									Unit
		2560xRGBx960 (Two Port)			1920xRGBx1080 (Two Port)			1920xRGBx720 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}		78.82			67.47			87.7		MHz
Horizontal valid data	t_{hd}		1280			960			1920		DCLK
1 horizontal line	t_h	1335	1346	1664	1015	1026	1248	1975	1986	2496	DCLK
Vertical valid data	t_{vd}		960			1080			720		H
1 vertical field (5)	t_v	970	976	1010	1090	1096	1134	730	736	756	H
Frame rate	FR		60			60			60		Hz

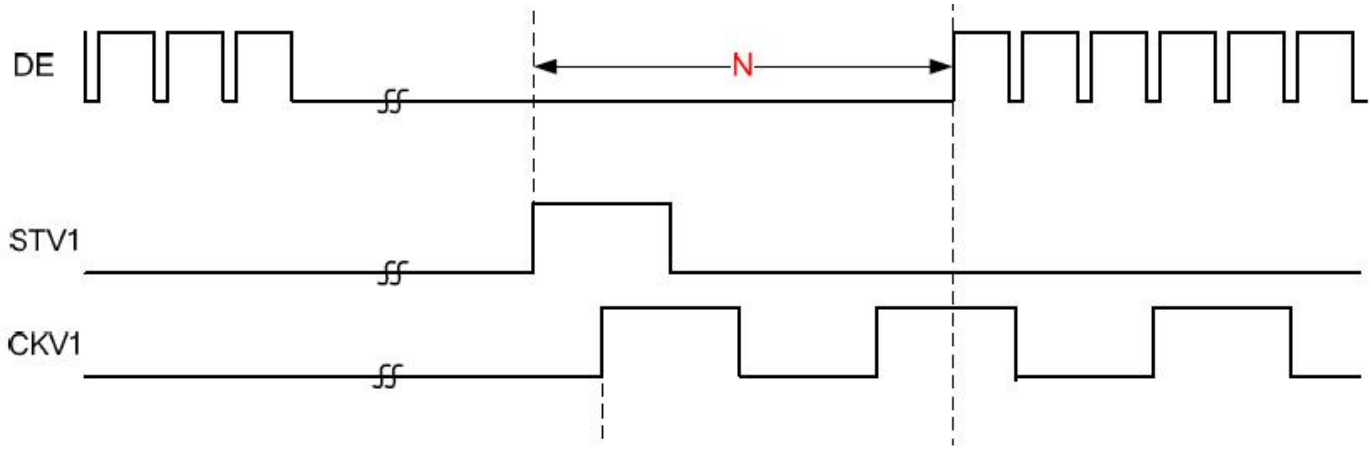


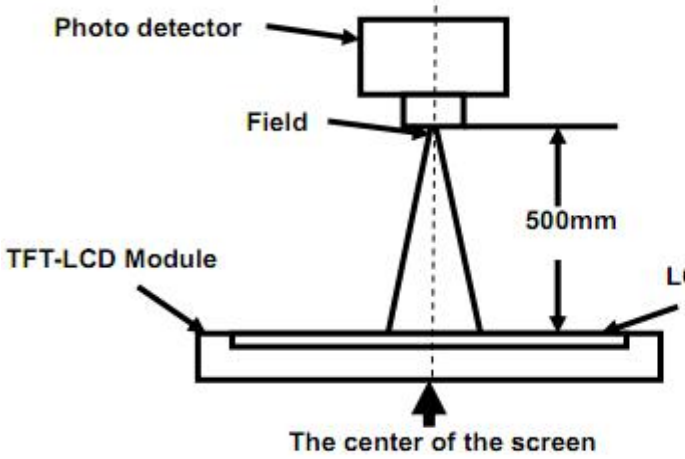
Table 6.2: Input timing table at DE only mode

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	Φ=90°(12 o'clock)	80	85	-	deg	Note2
	θ_B	Φ=270°(6 o'clock)	80	85	-	deg	Note2
	θ_L	Φ=180°(9 o'clock)	80	85	-	deg	Note2
	θ_R	Φ=0°(3 o'clock)	80	85	-	deg	Note2
Response Time	T_{ON}	Normal θ=Φ=0°	-	-	12	msec	Note4
	T_{OFF}		-	-	12	msec	Note4
Contrast Ratio	CR		1100	1300	-	-	Note1 Note3
Color Chromaticity	W_X		TBD	TBD	TBD	-	Note1 Note5
	W_Y		TBD	TBD	TBD	-	Note1 Note5
Luminance	L		900	1000	-	cd/m²	Note1 Note7
Luminance Uniformity	Y_U		70	80	-	%	Note1 Note6
NTSC	-		65	70	-	%	-

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Fig 1

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

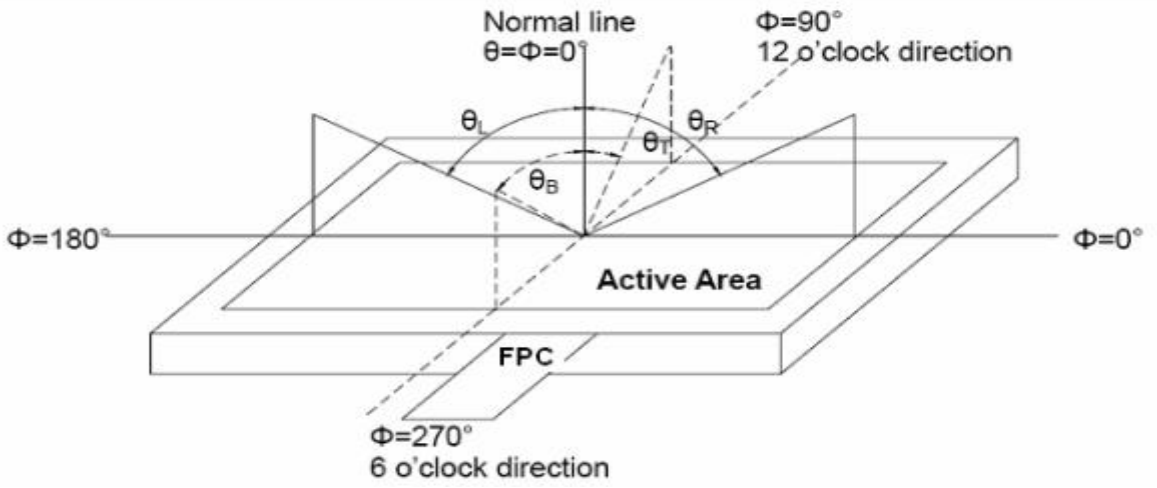


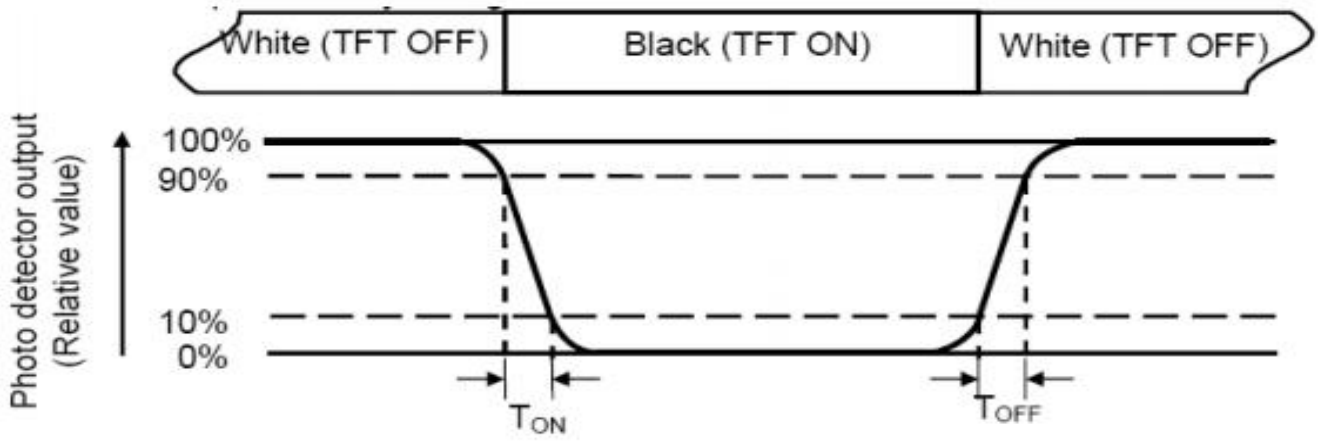
Fig 2 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.3-a/b

Note 7:Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

For more information see FIG.3-a/b

Note 8:Size : S≤5”(see Figure a) H,V : Active area
Light spot size ⌀ =5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or test spot position : see Figure a.
measurement instrument : TOPCON’s luminance meter SR-3A or BM-7 or compatible (see Figure 1).

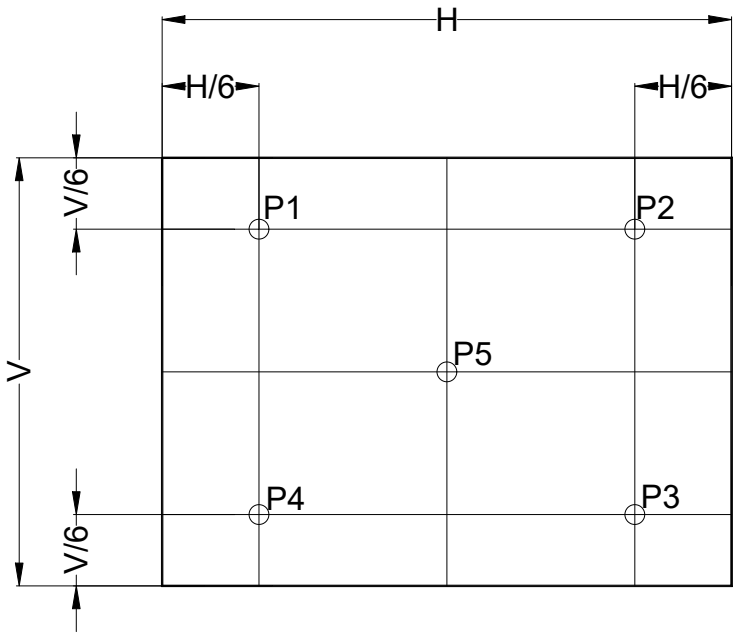


Fig. 3-a Definition of points

5”＜S≤12.3”(see Figure b) . H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens. test spot position : see Figure b.
measurement instrument : TOPCON’s luminance meter SR-3A or BM-7 or compatible (see Figure 1).

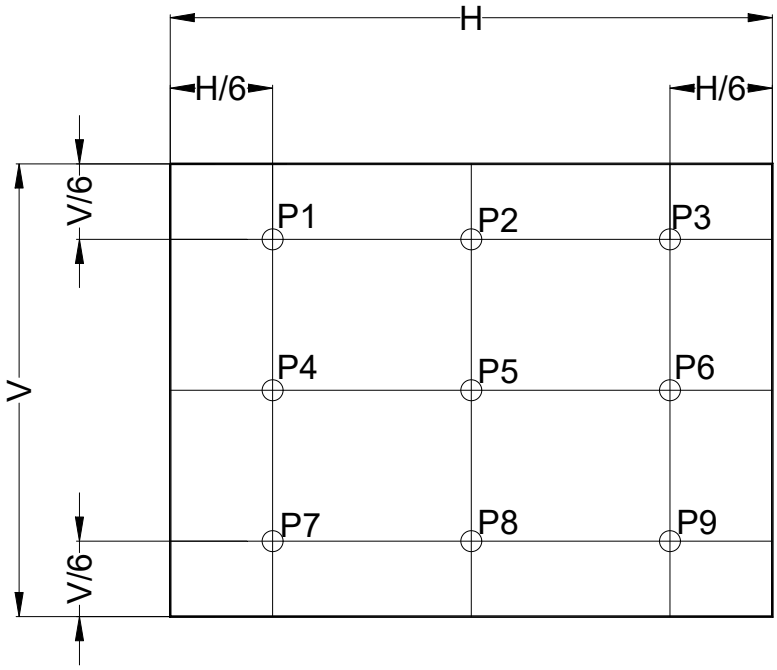


Fig. 3-b Definition of points

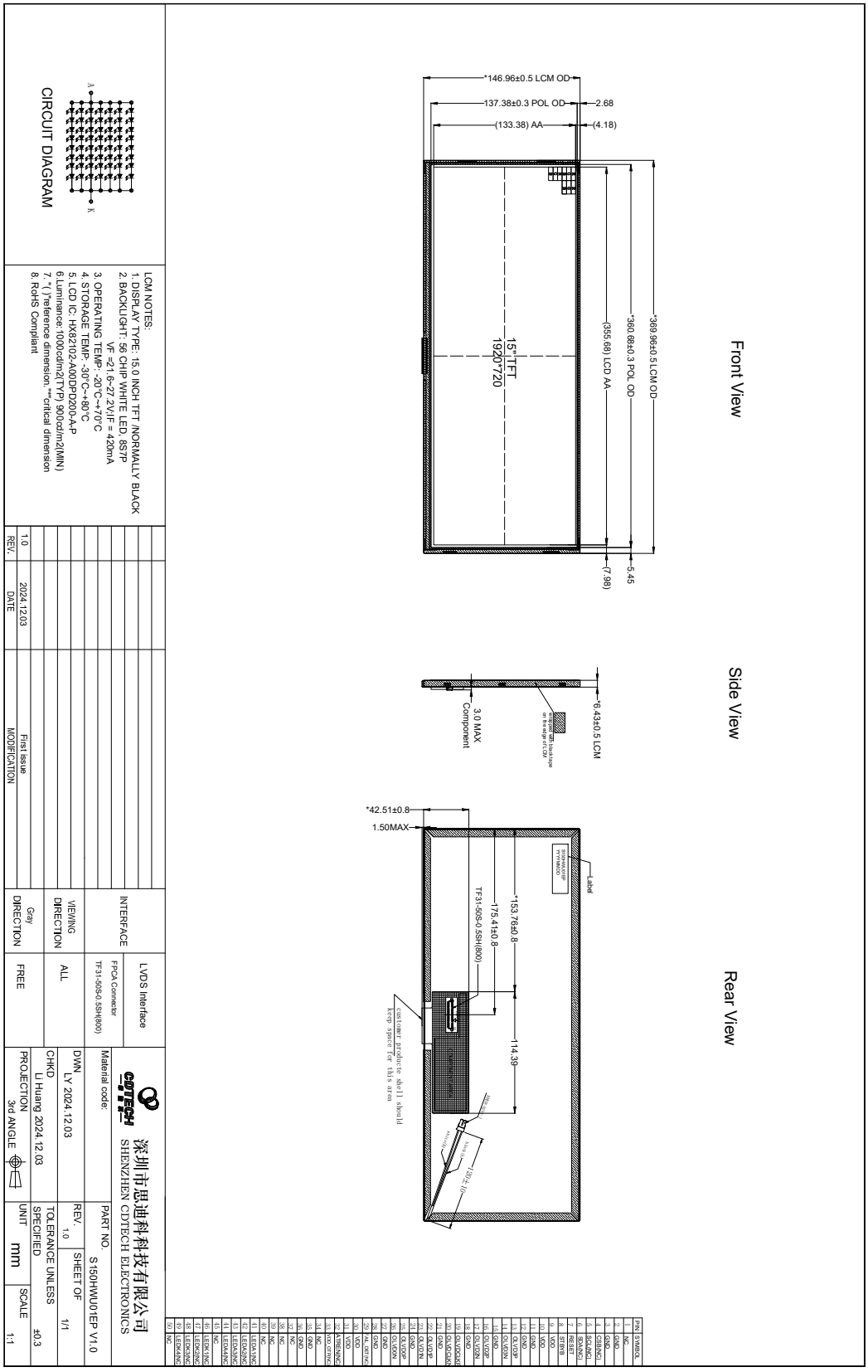
7. Reliability Test Items

Test Item	Test Conditions	
High Temperature Storage	Ta= +80℃	96hrs
Low Temperature Storage	Ta= -30℃	96hrs
High Temperature Operation	Ta= +70℃	96hrs
Low Temperature Operation	Ta= -20℃	96hrs
High Temperature and Humidity Storage	Ta= +60℃, 90% RH	96hrs
Thermal Shock (Non-operation)	-30℃/30 min ~ +80℃/30 min for 20 cycles Start with cold temperature end with high temperature	
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF	
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.	
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction	
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

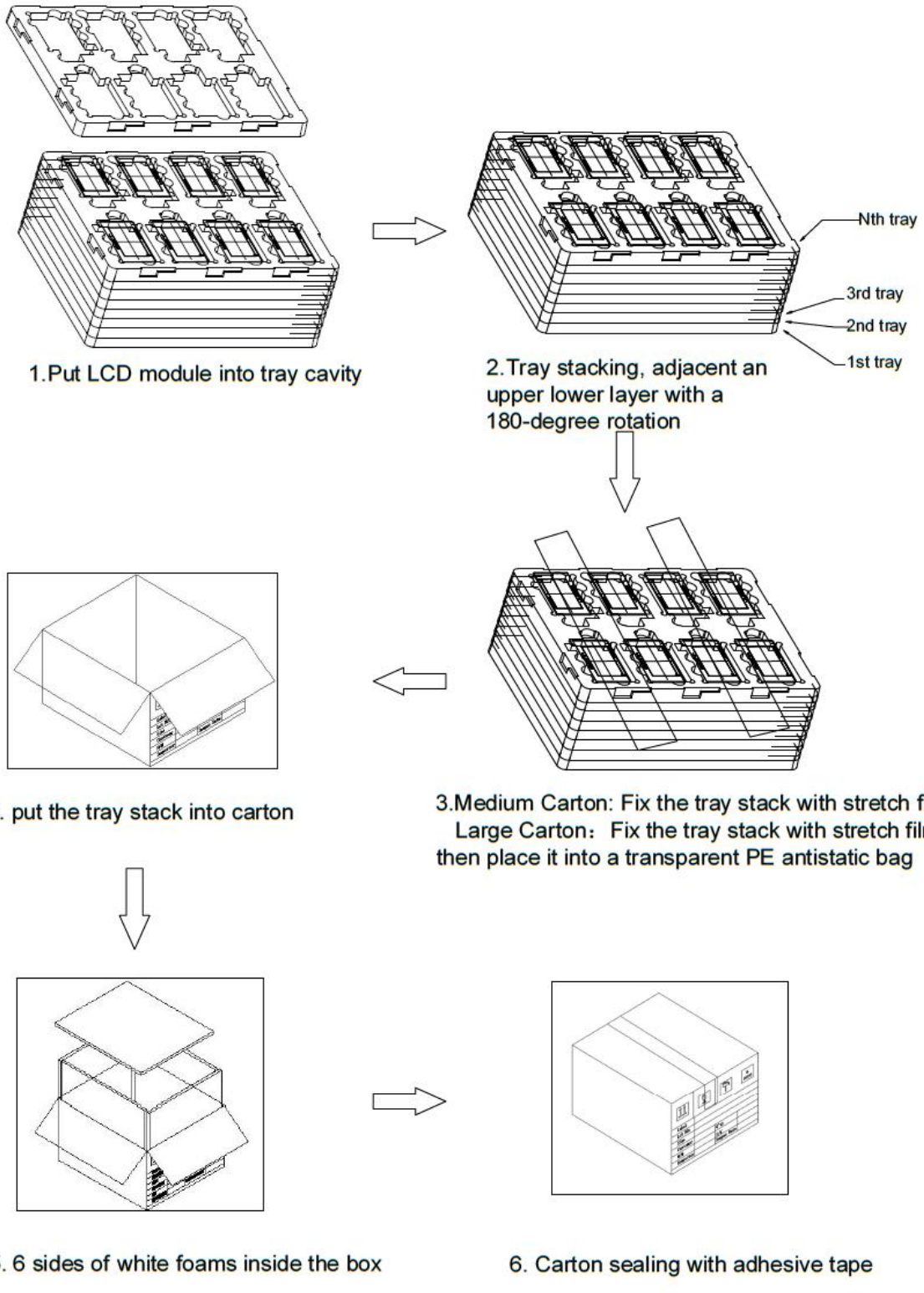
1). Air bubble in the LCD
2). Seal leak or Glass crack
3). Non display or abnormal display
4). Brightness reduction >50%

8. Mechanical Drawing



9. Packing

Packing Method



10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1.When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2.The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time,the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3.The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

10.4 Packaging instructions

when the customers using trays, they have to stack the adjacent trays in a 180° staggered to prevent pressure that could cause product damage.