DATA SHEET

(DOC No. HX82102-A-LT-DS)

HX82102-A-LT

1923CH TFT LCD Source Driver with TCON

Version 02 December, 2021

Himax Technologies, Inc.
http://www.himax.com.tw

Revision History

December, 2021

Version	Date	Description of changes
01	2021/11/25	New setup.
02	2021/12/22	Page 15 1. Correct the typo. Page 214 2. Modify CRC_FUNCTION_EN register description. Page 233 3. Modify max. standby current **(VCC1 + VCC2)** from 100μA to 400μA.

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1. General Description

The HX82102-A-LT is a highly integrated source driver with built-in timing controller for color TFT LCD panels. This driver supports multiple display resolutions, with functions of 1923-channel 8-bit dot-inversion source driver **(SD)**, timing controller **(TCON)**, power circuits, GIP or LTPS switch control, I2C interface **(I2C)** and serial peripheral interface **(SPI)**. This driver is for industrial or automotive products.

2. Features

General

- COG **(Chip on glass)** package
- Support LTPS panel **(MUX1:1/MUX2:4/MUX2:6)**
- Support a-TFT panel **(single gate/dual gate/triple gate)**
- Support Stripe and Zig-Zag type panel
- Support Normally Black and Normally White panels
- 8-bit per color true resolution **(16.7 million colors)**
- Cascade mode for high resolution
- Closed loop for IC connection resistance checking
- On-chip OTP **(One-Time-Programming)** memory for all registers
- OTP for 3-set gamma setting
- External EEPROM for all registers
- GAS function **(Gate all select)** for preventing image sticking when abnormal power off
- Touch panel synchronization signal TP_SYNC
- Over voltage protection in VCC/VSP/VSN
- Over current protection in VSP/VSN
- AEC-Q100 Compliant for Automotive Applications
- Operation temperature: -40℃ to +105℃

Timing controller

- Panel resolution:
  - 2560xRGBx960
  - 1920xRGBx1080
  - 1920xRGBx720
  - 1660xRGBx1660
  - 1560xRGBx720
  - 1540xRGBx720
  - 1440xRGBx540
  - 1280xRGBx720
  - 1280xRGBx480
  - 1024xRGBx600
  - 960xRGBx960
  - 800xRGBx480
  - 720xRGBx720

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  - 640xRGBx640
  - 540xRGBx540
  - 480xRGBx480
- Support 6-bit or 8-bit LVDS interface
- Support HS+VS mode and DE mode
- 3/4-wire SPI or I2C command setting
- Support digital gamma processing and contrast / brightness control on RGB data separately
- Internal pattern generator with basic patterns in built-in self testing **(BIST)** mode
- Provide self-protection function for missing CLK, HS, VS or DE input
- Provide IC fail detection function for LVDS/ Source/ Power
- CRC check function
- Adjust VCOM/VGH/VGL/VGMPH/VGMPL/VGMNH/VGMNL and analog gamma voltage by TS_H and TS_L pin setting

Source driver
- Support maximum 1923CH LCD source output
- Support Dot / 1+2Dot / 2+4Dot / Column inversion **(vertical direction)** for MUX1:1, MUX2:4 and MUX2:6
- Support column inversion for Zig-Zag type panel
- Support analog gamma
- Maximum ±6.6V output swing
- Right and left shift capability
- 3-layer staggered pad with 12μm pitch

Gate driver
- Provide twenty adjustable control output signals for GIP circuit
- Support LTPS mux switch control
- Support IGZO circuit

Power
- Main power supply VCC=3.0V to 3.6V
- Built-in PFM power control circuit for VSP and VSN
- Built-in regulators for gamma reference, TCON and LVDS power supplies
- Built-in charge pumps for GIP operation voltages VGH and VGL
- Built-in driving circuit for VCOM with SPI / I2C selection

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3. Block Diagram, DC/DC and Boost Circuit Construction

3.1. Block diagram

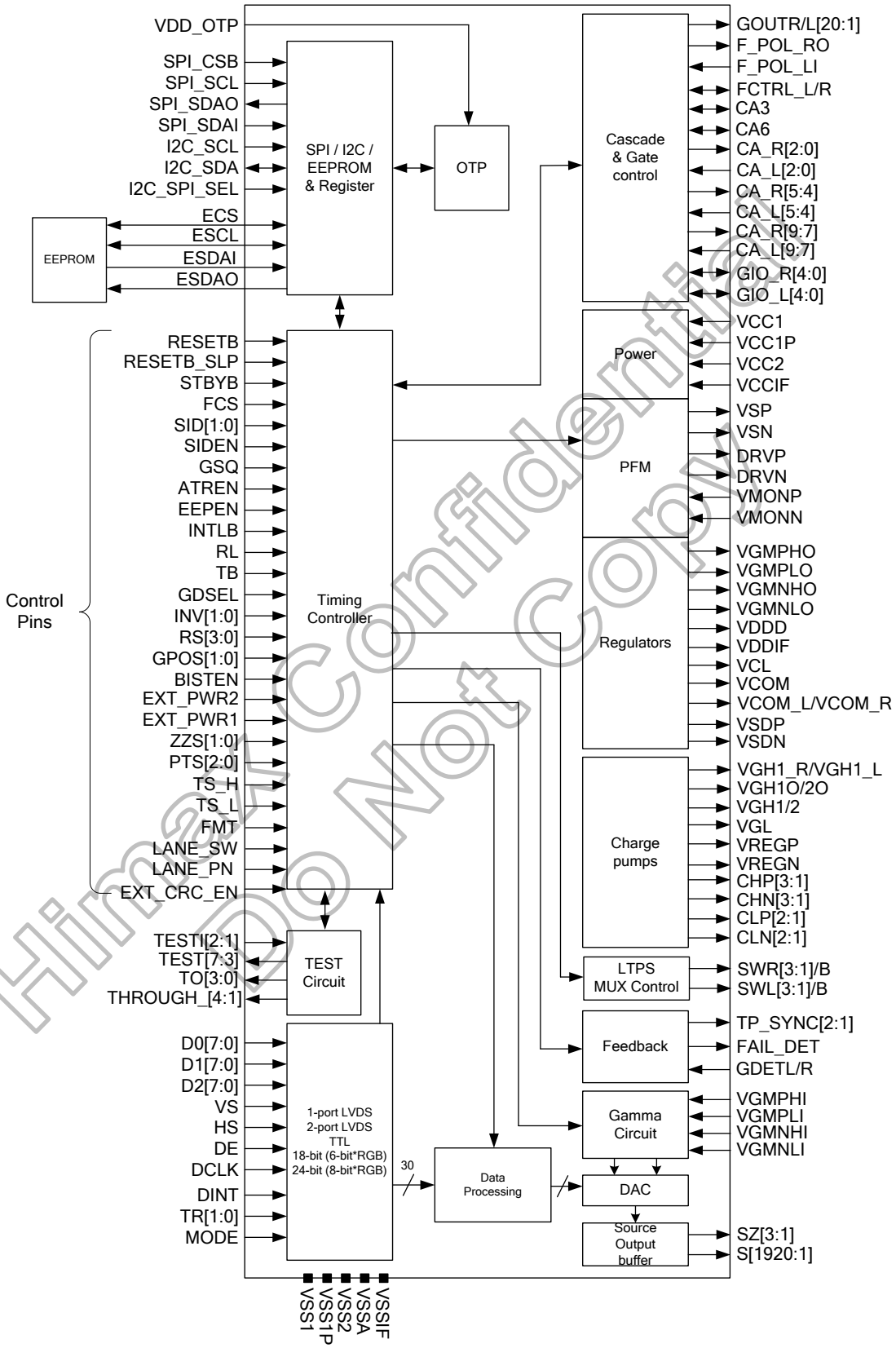

Figure 3.1: Block diagram

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3.2. DC/DC voltage construction

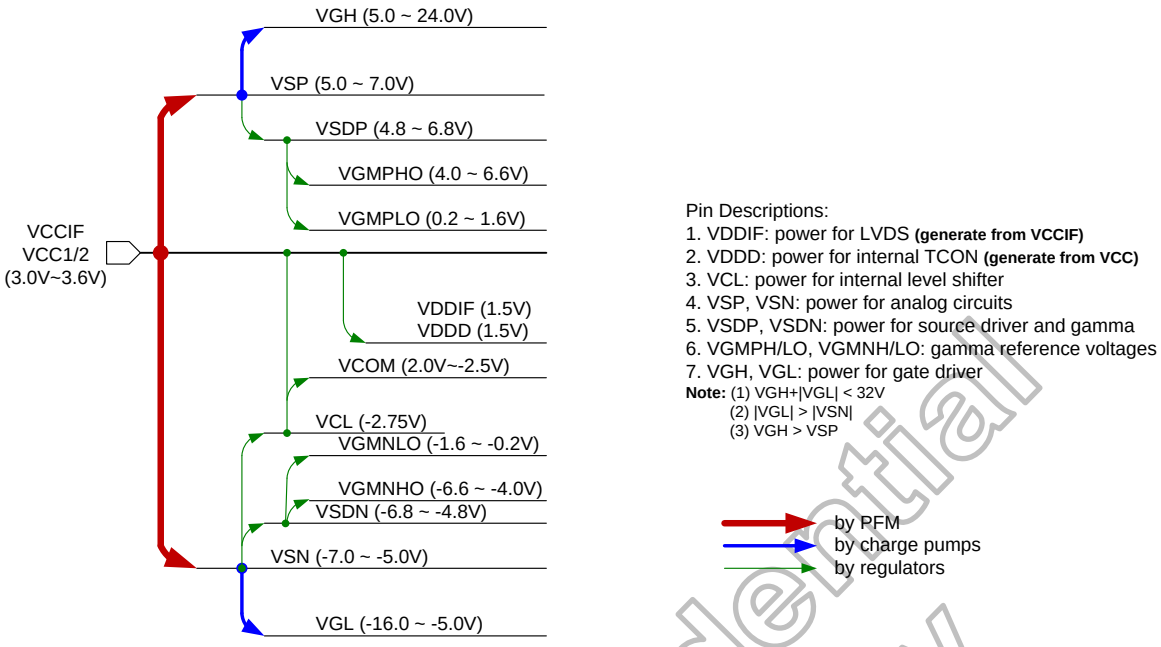

Figure 3.2: DC/DC voltage construction

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4. Pin Description

4.1. Pin description

<table>
<tr><th>Pin name</th><th>Type</th><th>Pulled internally</th><th>Description</th></tr>
<tr><td colspan="4">Input interface pins (VCC1/VSS1 level) (Refer to Ch. 4.2. Interface pin connection)</td></tr>
<tr><td>D00 ~ D07
D10 ~ D17
D20 ~ D27</td><td>I</td><td>-</td><td>Data input pins for TTL or LVDS mode.</td></tr>
<tr><td>DCLK</td><td>I</td><td>-</td><td>CLK for TTL mode.</td></tr>
<tr><td>HS</td><td>I</td><td>H</td><td>Horizontal sync signal for TTL mode.</td></tr>
<tr><td>VS</td><td>I</td><td>H</td><td>Vertical sync signal for TTL mode.</td></tr>
<tr><td>DE</td><td>I</td><td>L</td><td>Data enable signal for TTL mode.</td></tr>
<tr><td colspan="4">Input control pins, group 1 (Function controlled) (VCC1/VSS1 level)</td></tr>
<tr><td>RESETB</td><td>I</td><td>H</td><td>Global reset pin, active low.
If RESETB=L, the chip is in reset state.</td></tr>
<tr><td>RESETB_SLP</td><td>I</td><td>H</td><td>Reset after power off sequence, active low.
If RESETB_SLP=L, the chip is in sleep in state, and all register will be reset after RESETB_SLP rising edge.
When RESETB_SLP function not used, please connect to VCC1.
(RESET_SLP function (RESETB_SLP=0) at least needs 7 frames input timing for Power off sequence.)</td></tr>
<tr><td>STBYB</td><td>I</td><td>H</td><td>Standby mode setting pin, active low.
Timing controller, output buffer, DAC and power circuit all off when STBYB is low.</td></tr>
<tr><td>FCS</td><td>I</td><td>H</td><td>Function control by Hardware/Software selection.
(RL, TB, BISTEN function is the hardware setting “XOR” with register setting when FCS=L.)
<table>
<tr><th>FCS</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Hardware pin (Group 2)</td><td>Default</td></tr>
<tr><td>L</td><td>Software register</td><td>-</td></tr>
</table></td></tr>
<tr><td>SID[1:0]</td><td>I</td><td>-</td><td>Source driver ID (Position in chain) selection.
<table>
<tr><th>SID[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>Master</td><td>-</td></tr>
<tr><td>LH</td><td>Slave 1</td><td>-</td></tr>
<tr><td>HL</td><td>Slave 2</td><td>-</td></tr>
<tr><td>HH</td><td>Slave 3</td><td>-</td></tr>
</table>
(Refer to Ch. 5.4.1. Gate driver arrangement on panel.)</td></tr>
<tr><td>SIDEN</td><td>I</td><td>H</td><td>Enable chip ID identification in SPI or I2C.
<table>
<tr><th>SIDEN</th><th>Function</th><th>Note</th></tr>
<tr><td>1</td><td>Chip R/W by CHIP ID[1:0] setting</td><td>Default</td></tr>
<tr><td>0</td><td>Write to all chip, and read from Master only</td><td>-</td></tr>
</table>
(Refer to “Serial interface”.)</td></tr>
<tr><td>GSQ</td><td>I</td><td>L</td><td>Gate driver type selection.
<table>
<tr><th>GSQ</th><th>Function</th><th>Note</th></tr>
<tr><td>1</td><td>Type 2</td><td>-</td></tr>
<tr><td>0</td><td>Type 1</td><td>Default</td></tr>
</table>
(Refer to Ch. 5.4.3. Gate driver type definition.)</td></tr>
<tr><td>ATREN</td><td>I</td><td>L</td><td>Enable auto reload OTP/EEPROM every 60 frames. When stop reload or changing register values by SPI/I2C, ATREN should be kept L.
<table>
<tr><th>ATREN</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Enable auto-reload OTP/EEPROM</td><td>-</td></tr>
<tr><td>L</td><td>Disable auto-reload OTP/EEPROM</td><td>Default</td></tr>
</table>
(If EEPEN=H and ATREN=H, the result is auto reload from EEPROM.)
(If EEPEN=L and ATREN=H, the result is auto reload from OTP.)</td></tr>
</table>

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<table>
<tr><th>Pin name</th><th>Type</th><th>Pulled internally</th><th>Description</th></tr>
<tr><td>EXT_PWR2</td><td>I</td><td>L</td><td>External / Internal power supply selection
<table>
<tr><th>EXT_PWR2</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>External VGH / VGL power supply</td><td>-</td></tr>
<tr><td>L</td><td>Internal VGH / VGL power supply</td><td>Default</td></tr>
</table></td></tr>
<tr><td>EXT_PWR1</td><td>I</td><td>L</td><td>External / Internal power supply selection
<table>
<tr><th>EXT_PWR1</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>External VSDP / VSDN power supply</td><td>-</td></tr>
<tr><td>L</td><td>Internal VSDP / VSDN power supply</td><td>Default</td></tr>
</table>
(When EXT_PWR1=H, External VSP/VSN power supply enable, the VSDP need short to VSP and VSDN need short to VSN by external circuit.)
(When EXT_PWR1=L, Internal VSP/VSN power supply enable, the avarege current of I_{VSDP} and I_{VSDN} must to be smaller than 30mA.)</td></tr>
<tr><td>EEPEN</td><td>I</td><td>L</td><td>EEPROM reload setting enable
<table>
<tr><th>EEPEN</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Enable EEPROM reload setting</td><td>-</td></tr>
<tr><td>L</td><td>Disable EEPROM reload setting</td><td>Default</td></tr>
</table></td></tr>
<tr><td>I2C_SPI_SEL</td><td>I</td><td>L</td><td>SPI / I2C interface selection.
<table>
<tr><th>I2C_SPI_SEL</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>I2C interface mode</td><td>-</td></tr>
<tr><td>L</td><td>SPI interface mode</td><td>Default</td></tr>
</table></td></tr>
<tr><td colspan="4">Input control pins, group 2 (Function controlled by hardware or software setting) (VCC1/VSS1 level)</td></tr>
<tr><td>TR[1:0]</td><td>I</td><td>LL</td><td>Interface selection.
<table>
<tr><th>TR[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>Lx</td><td>TTL</td><td>Default</td></tr>
<tr><td>HL</td><td>1-port LVDS</td><td>-</td></tr>
<tr><td>HH</td><td>2-port LVDS</td><td>-</td></tr>
</table></td></tr>
<tr><td>MODE</td><td>I</td><td>H</td><td>Input timing mode selection.
<table>
<tr><th>MODE</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>HS+VS</td><td>Default</td></tr>
<tr><td>L</td><td>DE only</td><td>-</td></tr>
</table></td></tr>
<tr><td>INTLB</td><td>I</td><td>H</td><td>Interlaced / normal input selection.
<table>
<tr><th>INTLB</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Normal input</td><td>Default</td></tr>
<tr><td>L</td><td>Interlaced input</td><td>-</td></tr>
</table></td></tr>
<tr><td>RL</td><td>I</td><td>H</td><td>Horizontal shift direction (Source output) selection.
(RL function is the hardware setting “XOR” with register setting when FCS=L.)
<table>
<tr><th>RL</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Forward
(S1→S2→ …→ S1920)</td><td>Default</td></tr>
<tr><td>L</td><td>Reverse
(S1920→S1919→ …→ S1)</td><td>-</td></tr>
</table></td></tr>
<tr><td>TB</td><td>I</td><td>H</td><td>Vertical shift direction (Gate output) selection.
(TB function is the hardware setting “XOR” with register setting when FCS=L.)
<table>
<tr><th>TB</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Forward, Top→Bottom</td><td>Default</td></tr>
<tr><td>L</td><td>Reverse, Bottom→Top</td><td>-</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Pin name</th><th>Type</th><th>Pulled internally</th><th>Description</th></tr>
<tr><td>GDSEL</td><td>I</td><td>L</td><td>Select pin of GIP / Gate driver mode
<table>
<tr><th>GDSEL</th><th>Function</th><th>Note</th></tr>
<tr><td>L</td><td>GIP</td><td>Default</td></tr>
<tr><td>H</td><td>Traditional Gate driver</td><td>-</td></tr>
</table></td></tr>
<tr><td>INV[1:0]</td><td>I</td><td>HH</td><td>Inversion type selection.

When PTS = 3’b000/001/010/011//100/101for Single gate/ MUX 2:4/ MUX 2:6 (Zig-zag type only support column inversion)
<table>
<tr><th>INV[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>1 line dot inversion (Vertical)</td><td>-</td></tr>
<tr><td>LH</td><td>1+2 line inversion (Vertical)</td><td>-</td></tr>
<tr><td>HL</td><td>2+4 line inversion (Vertical)</td><td>-</td></tr>
<tr><td>HH</td><td>Column inversion (Vertical)</td><td>Default</td></tr>
</table>
When PTS = 3’b100 for Dual gate (Zig-zag type only support column inversion)
<table>
<tr><th>INV[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>1+2 dot inversion (Horizontal)</td><td>-</td></tr>
<tr><td>LH</td><td>2 dot inversion (Horizontal)</td><td>-</td></tr>
<tr><td>HL</td><td>1+2line 2dot inversion (Horizontal)</td><td>-</td></tr>
<tr><td>HH</td><td>2+4line 2dot inversion (Horizontal)</td><td>Default</td></tr>
</table>
When PTS = 3’b101 for Triple gate (Zig-zag type only support column inversion)
<table>
<tr><th>INV[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>Dot inversion (Vertical)</td><td>-</td></tr>
<tr><td>LH</td><td>3 line inversion (Vertical)</td><td>-</td></tr>
<tr><td>HL</td><td>6 line inversion (Vertical)</td><td>-</td></tr>
<tr><td>HH</td><td>Column inversion (Vertical)</td><td>Default</td></tr>
</table></td></tr>
<tr><td>RS[3:0]</td><td>I</td><td>-</td><td>Panel resolution selection.
<table>
<tr><th>RS[3:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LLLL</td><td>2560 x RGB x 960 (Except MUX1:1)</td><td>Default</td></tr>
<tr><td>LLLH</td><td>1920 x RGB x 1080</td><td>-</td></tr>
<tr><td>LLHL</td><td>1920 x RGB x 720</td><td>-</td></tr>
<tr><td>LLHH</td><td>1660 x RGB x 1660</td><td>-</td></tr>
<tr><td>LHLL</td><td>1560 x RGB x 720</td><td>-</td></tr>
<tr><td>LHLH</td><td>1540 x RGB x 720</td><td>-</td></tr>
<tr><td>LHHL</td><td>1440 x RGB x 540</td><td>-</td></tr>
<tr><td>LHHH</td><td>1280 x RGB x 720</td><td>-</td></tr>
<tr><td>HLLL</td><td>1280 x RGB x 480</td><td>-</td></tr>
<tr><td>HLLH</td><td>1024 x RGB x 600</td><td>-</td></tr>
<tr><td>HLHL</td><td>960 x RGB x 960</td><td>-</td></tr>
<tr><td>HLHH</td><td>800 x RGB x 480</td><td>-</td></tr>
<tr><td>HHLL</td><td>720 x RGB x 720</td><td>-</td></tr>
<tr><td>HHLH</td><td>640 x RGB x 640</td><td>-</td></tr>
<tr><td>HHHL</td><td>540 x RGB x 540</td><td>-</td></tr>
<tr><td>HHHH</td><td>480 x RGB x 480</td><td>-</td></tr>
</table></td></tr>
<tr><td>GPOS[1:0]</td><td>I</td><td>LL</td><td>Traditional Gate driver location select.
<table>
<tr><th>GPOS[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>Left side</td><td>Default</td></tr>
<tr><td>LH</td><td>Right side</td><td>-</td></tr>
<tr><td>HL</td><td>Interlaced driving at dual side</td><td>-</td></tr>
<tr><td>HH</td><td>Progressive driving the same line at dual side</td><td>-</td></tr>
</table>
(Refer to Ch. 5.4.4. Gate driver signal definition.)</td></tr>
</table>

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<table>
<tr><th>Pin name</th><th>Type</th><th>Pulled internally</th><th>Description</th></tr>
<tr><td>BISTEN</td><td>I</td><td>L</td><td>Enable built-in self test (BIST) function.
(BISTEN function is the hardware setting “XOR” with register setting when FCS=L.)
<table>
<tr><th>BISTEN</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>BIST mode</td><td>-</td></tr>
<tr><td>L</td><td>Normal mode</td><td>Default</td></tr>
</table></td></tr>
<tr><td>ZZS[1:0]</td><td>I</td><td>LL</td><td>Zig-zag type selection.
<table>
<tr><th>ZZS[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>Stripe panel</td><td>Default</td></tr>
<tr><td>LH</td><td>Zig-zag type 1</td><td>-</td></tr>
<tr><td>HL</td><td>Zig-zag type 2</td><td>-</td></tr>
<tr><td>HH</td><td>Stripe panel</td><td>-</td></tr>
</table></td></tr>
<tr><td>PTS[2:0]</td><td>I</td><td>LLL</td><td>Panel type selection.
<table>
<tr><th>PTS[2:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LLL</td><td>LTPS MUX 2:4</td><td>-</td></tr>
<tr><td>LLH</td><td>LTPS MUX 2:6_Type1</td><td>-</td></tr>
<tr><td>LHL</td><td>LTPS MUX 2:6_Type2</td><td>-</td></tr>
<tr><td>LHH</td><td>Single gate</td><td>Default</td></tr>
<tr><td>HLL</td><td>Dual gate</td><td>-</td></tr>
<tr><td>HLH</td><td>Triple gate</td><td>-</td></tr>
<tr><td>Hxx</td><td>-</td><td>-</td></tr>
</table></td></tr>
<tr><td>FMT</td><td>I</td><td>L</td><td>TTL or LVDS input data format selection:
If TR1=H, select LVDS format.
<table>
<tr><th>FMT</th><th>Function</th><th>Note</th></tr>
<tr><td>L</td><td>JEIDA format</td><td>Default</td></tr>
<tr><td>H</td><td>VESA format</td><td>-</td></tr>
</table></td></tr>
<tr><td>LANE_SW</td><td>I</td><td>L</td><td>LVDS lane swapping selection.
(Please refer to Ch. 4.2. Interface pin connection for lane arrangement.)</td></tr>
<tr><td>LANE_PN</td><td>I</td><td>L</td><td>LVDS lane PN polarity swapping selection.</td></tr>
<tr><td>DINT</td><td>I</td><td>H</td><td>Input data 6-bit or 8-bit selection.
<table>
<tr><th>DINT</th><th>Function</th><th>Note</th></tr>
<tr><td>L</td><td>6-bit</td><td>-</td></tr>
<tr><td>H</td><td>8-bit</td><td>Default</td></tr>
</table></td></tr>
<tr><td>EXT_CRC_EN</td><td>I</td><td>L</td><td>CRC function enable. (Do XOR operation with register CRC_EN)</td></tr>
<tr><td colspan="4">Serial interface pins (VCC1/VSS1 level)</td></tr>
<tr><td>SPI_CSB</td><td>I</td><td>H</td><td>Serial Interface chip enable signal for SPI interface.
SPI_CSB=L: Selected (Accessible).
SPI_CSB=H: Not selected (Inaccessible).</td></tr>
<tr><td>SPI_SCL</td><td>I</td><td>L</td><td>Serial interface clock input for SPI interface.</td></tr>
<tr><td>SPI_SDAI</td><td>I</td><td>L</td><td>Serial interface address and data input for SPI interface.</td></tr>
<tr><td>SPI_SDAO</td><td>O</td><td>-</td><td>Serial interface data output for SPI interface.</td></tr>
<tr><td>I2C_SDA</td><td>I/O</td><td>-</td><td>Serial interface address and data input/output for I2C interface.
(I2C interface need external pull high resistance(4.7KΩ).)</td></tr>
<tr><td>I2C_SCL</td><td>I</td><td>H</td><td>Serial interface clock input for I2C interface.
(I2C interface need external pull high resistance(4.7KΩ).)</td></tr>
<tr><td colspan="4">EEPROM interface pins (VCC1/VSS1 level)</td></tr>
<tr><td>ECS</td><td>I/O</td><td>L</td><td>Chip select enable signal for EEPROM CS.
ECS=L: Not accessing EEPROM.
ECS=H: Accessing EEPROM.</td></tr>
<tr><td>ESCL</td><td>I/O</td><td>L</td><td>Clock signal for EEPROM CLK.</td></tr>
<tr><td>ESDAI</td><td>I</td><td>L</td><td>Serial data input from EEPROM DO.</td></tr>
</table>

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Pin name	Type	Pulled internally	Description
ESDAO	O	-	Serial data **(address)** output for EEPROM DI.
Cascade and gate control pins(1)			
GIO_L[4:0]	I/O	-	Gate driver control pins at the left side.
FCTRL_L	I/O	L	GIP mode sync pin.
CA_L[2:0] CA_L[5:4] CA_L[9:7]	I/O	-	Cascade signal in/out pin.
CA6	I/O	-	Cascade signal pin. **(Open drain I/O)**
F_POL_LI	I	L	POL sync control signal.
CA3	I/O	-	Cascade signal pin. **(Open drain I/O)**
CA_R[2:0] CA_R[5:4] CA_R[9:7]	I/O	-	Cascade signal in/out pin.
GIO_R[4:0]	I/O	-	Gate driver control pins at the right side.
FCTRL_R	I/O	L	GIP mode sync pin.
F_POL_RO	O	-	POL sync control signal.
Special function pins			
TP_SYNC1	O	-	Output frame signal for Touch Panel application.
TP_SYNC2	O	-	Output frame signal for Touch Panel application.
FAIL_DET	O	-	Fail detection signal output.
TS_H TS_L	I	LL	Input High/Low temperature mode. [TS_H:TS_L] / Function / Note LL / Room temperature mode. / Default LH / Low temperature mode. / - HL / High temperature mode. / - HH / Reserved / -
GDETR	I	-	GIP detect input pin.
GDETL	I	-	GIP detect input pin.

Note: (1) Leave these pins open if not used. Refer to “cascade and gate control interface”.

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Pin name	Type	Description
Source and GIP output pins		
SZ1, SZ2, SZ3, S[1920:1]	O	Source driver output pins.
GOUTR[20:1]	O	GIP control output pins.
GOUTL[20:1]	O	GIP control output pins.
SWR[3:1] SWR[3:1]B	O	MUX Control output pins.
SWL[3:1] SWL[3:1]B	O	MUX Control output pins.
Power supply pins: Connected to power supply		
VCC1	P	Power input for main and I/O power **(3.0V to 3.6V)**.
VCC1P	P	Power input pin. Connected to VCC1.
VSS1	P	Ground pin for logic circuit and I/O **(0V)**.
VSS1P	P	Ground pin. Connected to VSS1.
VCC2	P	Power pin for internal references **(3.0V to 3.6V)**.
VSS2	P	Ground pin for internal reference circuit **(0V)**.
VSSA	P	Ground pin for analog circuit **(0V)**.
VCCIF	P	Power pin for LVDS/TTL interface I/O **(3.0V to 3.6V)**.
VSSIF	P	Ground pin for LVDS/TTL interface I/O **(0V)**.
VSP	P	Power input for source driver and power circuits **(5V to 7V)**.
VSN	P	Power input for source driver and power circuits **(-7V to -5V)**.
VDD_OTP	P	Power input for OTP programming **(8.6V)**. Leave this pin open or connect it to VCC1 when not programming OTP.
Regulator output and voltage reference input pins: Connected to capacitors		
VGMPHO	O	Internal regulator output for positive gamma reference voltage.
VGMPLO	O	Internal regulator output for positive gamma reference voltage.
VGMNHO	O	Internal regulator output for negative gamma reference voltage.
VGMNLO	O	Internal regulator output for negative gamma reference voltage.
VGMPHI	I	Positive gamma reference voltage.
VGMPLI	I	Positive gamma reference voltage.
VGMNHI	I	Negative gamma reference voltage.
VGMNLI	I	Negative gamma reference voltage.
VDDD	O	Internal regulator output for logic power supply **(1.5V)**.
VDDIF	O	Internal regulator output for interface power supply **(1.5V)**.
VCOM	O	Internal driving circuit for VCOM **(-2.5V to 2.0V)**.
VCL	O	Internal regulator output for negative level shifter **(-2.75V)**.
VSDP	O	Internal regulator output for source driver and gamma.
VSDN	O	Internal regulator output for source driver and gamma.
Charge pump and PFM pins: Connected to external components		
VGH1	O	Charge pump output for gate driver.
VGH1O	O	Discharge VGH1 to ground. **(Depend on register DCHG1R)**
VGH2	O	Charge pump output for gate driver.
VGH2O	O	Discharge VGH2 to ground. **(Depend on register DCHG2R)**
VGL	O	Charge pump output for gate driver.
CHP[3:1] CHN[3:1]	C	Capacitor connection pin for VGH charge pump.
CLP[2:1] CLN[2:1]	C	Capacitor connection pin for VGL charge pump.
VREGP	O	Regulator voltage for VGH charge pump. **(Only for diode connect type)** If not using external diode, let this pin floating.
VREGN	O	Regulator voltage for VGL charge pump. **(Only for diode connect type)** If not using external diode, let this pin floating.
DRVP	O	PFM output control signal for VSP.
DRVN	O	PFM output control signal for VSN.
VMONP	I	Input pin for positive voltage detection for PFM over current detection. When PFM function not used, please connect to GND.

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Pin name	Type	Description
VMONN	I	Input pin for negative voltage detection for PFM over current detection. When PFM function not used, please connect to GND.
Test pins, through pins and dummy pins		
TEST[7:3]	O	Logic test pins, these must be floating.
TESTI[2:1]	I	Logic test pins, these pins must be floating. **(Default pull low)**
TO[3:0]	O	Internal reference voltage test pin, these pins must be floating.
THROUGH_[4:1]	-	These sets of pins can be used for resistance measurement.
VCOM_R VCOM_L	-	These sets of pins can be used for VCOM connection to the panel.
VGH1_R VGH1_L	-	For GOA application, these pins must be connected to VGH1. For tradition gate application, these pins can be connected to VGH1 or VGH2.
DUMMY	-	Please let it floating.
S_DUMMY	-	Please let it floating.

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4.2. Interface pin connection

LANE_SW selection				LANE_SW=L		LANE_SW=H	
Pin name	**Pin type**	**TTL 8-bit**	**TTL 6-bit(1)**	**LVDS 2-port**	**LVDS 1-port**	**LVDS 2-port**	**LVDS 1-port**
D20	TTL/ Differential	DB0	VSS	-	-	-	-
D21		DB1	VSS	-	-	-	-
D22		DB2	DB0	-	-	-	-
D23		DB3	DB1	-	-	-	-
D24		DB4	DB2	ELV3P	-	ELV0P	-
D25		DB5	DB3	ELV3N	-	ELV0N	-
D26		DB6	DB4	ELV2P	-	ELV1P	-
D27		DB7	DB5	ELV2N	-	ELV1N	-
D10		DG0	VSS	ELVCLKP	-	ELVCLKP	-
D11		DG1	VSS	ELVCLKN	-	ELVCLKN	-
D12		DG2	DG0	ELV1P	-	ELV2P	-
D13		DG3	DG1	ELV1N	-	ELV2N	-
D14		DG4	DG2	ELV0P	-	ELV3P	-
D15		DG5	DG3	ELV0N	-	ELV3N	-
D16		DG6	DG4	OLV3P	OLV3P	OLV0P	OLV0P
D17		DG7	DG5	OLV3N	OLV3N	OLV0N	OLV0N
D00		DR0	VSS	OLV2P	OLV2P	OLV1P	OLV1P
D01		DR1	VSS	OLV2N	OLV2N	OLV1N	OLV1N
D02		DR2	DR0	OLVCLKP	OLVCLKP	OLVCLKP	OLVCLKP
D03		DR3	DR1	OLVCLKN	OLVCLKN	OLVCLKN	OLVCLKN
D04		DR4	DR2	OLV1P	OLV1P	OLV2P	OLV2P
D05		DR5	DR3	OLV1N	OLV1N	OLV2N	OLV2N
D06		DR6	DR4	OLV0P	OLV0P	OLV3P	OLV3P
D07		DR7	DR5	OLV0N	OLV0N	OLV3N	OLV3N
DCLK	TTL	CLK		-	-	-	-
HS		HS		-	-	-	-
VS		VS		-	-	-	-
DE		DE		-	-	-	-

Note: (1) In TTL 6-bit mode, unused pins D2[1:0], D1[1:0], D0[1:0] should be connected to ground. Unused pins in other modes can be floating.

Table 4.1: Interface pin connection

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4.3. Recommended wiring resistance values

The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Pad type	Pad	Resistance
Power supply pins	VCC1	< 5Ω
	VCC1P	< 5Ω
	VSS1	< 5Ω
	VSS1P	< 5Ω
	VCC2	< 5Ω
	VSS2	< 3Ω
	VSSA	< 3Ω
	VCCIF	< 5Ω
	VSSIF	< 3Ω
	VSP	< 3Ω
	VSN	< 3Ω
	VDD_OTP	< 5Ω
Special function pins	FAIL_DET	< 20Ω
	TS_L	< 50Ω
	TS_H	
	GDETR/GDETL	< 20Ω
Regulator output and reference input pins	VGMPHI/VGMPLI	< 20Ω
	VGMNHI/VGMNLI	
	VGMPHO/VGMPLO	
	VGMNHO/VGMNLO	
	VDDD	< 5Ω
	VDDIF	< 5Ω
	VCOM	< 30Ω
	VCL	< 10Ω
	VSDP	< 3Ω
	VSDN	< 3Ω
SPI /I2C pins	SPI_CSB	< 20Ω
	SPI_SCL	
	SPI_SDAI	
	SPI_SDAO	
	I2C_SDA	
	I2C_SCL	
Cascade pins	CA_R[2:0]	< 100Ω
	CA_R[5:4]	
	CA_R[9:7]	
	CA_L[2:0]	
	CA_L[5:4]	
	CA_L[9:7]	
	CA3	
	CA6	
	GIO_R[4:0]	
	GIO_L[4:0]	
	FCTRL_L	
	FCTRL_R	
	F_POL_LI	
	F_POL_RO	
Through pins	THROUGH_[4:1]	-
Input control pins	EXT_CRC_EN	< 150Ω

Pad type	Pad	Resistance
Input interface pins	D0[7:0] D1[7:0] D2[7:0] DCLK	< 20Ω
	HS	
	VS	
	DE	
Input control pins	RESETB	< 50Ω
	RESETB_SLP	
	STBYB	
	FCS	< 150Ω
	SID[1:0]	
	SIDEN	
	GSQ	
	ATREN	
	EXT_PWR1/2	
	DINT	
	EEPEN	
	TR[1:0]	
	MODE	
	INTLB	
	RL	
	TB	
	GDSEL	
	INV[1:0]	
	RS[3:0]	
	GPOS[1:0]	
	BISTEN	
	ZZS[1:0]	
	PTS[2:0]	
	I2C_SPI_SEL	
	FMT	
	LANE_SW	
	LANE_PN	
EEPROM	ECS	< 20Ω
	ESCL	
	ESDAI	
	ESDAO	
	VGH1/VGH2 VGH1_L/VGH1_R	<10Ω
	VGL	
Charge pump and PFM pins	CHP[3:1]	< 5Ω
	CHN[3:1]	
	CLP[2:1]	
	CLN[2:1]	
	VREGP/VREGN	< 5Ω
	DRVP/DRVN	< 5Ω
	VMONP/VMONN	< 20Ω
Through pins	VCOM_R	-
	VCOM_L	-
Other pins	TP_SYNC1/2	< 20Ω

Table 4.2: Recommended wiring resistance values

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4.4. Hardware pin option mapping software register option

The following settings can be chosen to be controlled by hardware input pin **(Group 2)** or by values in register Page00h and Page09h. When FCS is set to L, the chip is controlled by internal register. Otherwise, the chip is controlled by hardware pin.

Pin name	Register (Page00h)
GPOS[1:0]	R04h[5:4]
TR[1:0]	R02h[7:6]
MODE	R02h[4]
RL(1)	R03h[7]
TB(1)	R03h[6]
INV[1:0]	R03h[5:4]
RS[3:0]	R03h[3:0]
BISTEN(1)	R05h[4]
PTS[2:0]	R01h[6:4]
ZZS[1:0]	R01h[3:2]
GDSEL	R01h[7]
Pin name	**Register (Page09h)**
FMT	R01h[4]
LANE_SW	R01h[3]
LANE_PN	R01h[2]

Note: (1) RL, TB, BISTEN function is the hardware setting “XOR” register setting when FCS=L.

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5. Panel Application

5.1. Display resolution configuration

There are 16 resolutions supported. The source drivers can be cascaded to support maximum resolution 2560xRGBx960 with 4 chips at LTPS MUX1:1 panel structure.

LTPS MUX1:1 /single gate

Resolution		Setting	Source driver	
RGB (X)	Line (Y)	RS[3:0]	Chips cascaded (N)	Channels per chip
2560	960	0000	4	1920
1920	1080	0001	3	1920
1920	720	0010	3	1920
1660	1660	0011	3	1668/1656/1656
1560	720	0100	3	1560
1540	720	0101	3	1548/1536/1536
1440	540	0110	3	1440
1280	720	0111	2	1920
1280	480	1000	2	1920
1024	600	1001	2	1536
960	960	1010	2	1440
800	480	1011	2	1200
720	720	1100	2	1080
640	640	1101	1	1920
540	540	1110	1	1620
480	480	1111	1	1440

LTPS MUX2:4 /dual gate

Resolution		Setting	Source driver	
RGB (X)	Line (Y)	RS[3:0]	Chips cascaded (N)	Channels per chip(1)
2560	960	0000	2	1920
1920	1080	0001	2	1440
1920	720	0010	2	1440
1660	1660	0011	2	1248/1242
1560	720	0100	2	1170
1540	720	0101	2	1158/1152
1440	540	0110	2	1080
1280	720	0111	1	1920
1280	480	1000	1	1920
1024	600	1001	1	1536
960	960	1010	1	1440
800	480	1011	1	1200
720	720	1100	1	1080
640	640	1101	1	960
540	540	1110	1	810
480	480	1111	1	720

Note: (1) If GDSEL=L for GIP mode, the Vactive lines must be even number.
If GDSEL=L for GIP mode, the Vactive must be less than 2000 lines.

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LTPS MUX2:6 /triple gate

Resolution		Setting	Source driver	
RGB (X)	Line (Y)	RS[3:0]	Chips cascaded (N)	Channels per chip(1)
2560	960	0000	2	1280
1920	1080	0001	1	1920
1920	720	0010	1	1920
1660	1660	0011	1	1660
1560	720	0100	1	1560
1540	720	0101	1	1540
1440	540	0110	1	1440
1280	720	0111	1	1280
1280	480	1000	1	1280
1024	600	1001	1	1024
960	960	1010	1	960
800	480	1011	1	800
720	720	1100	1	720
640	640	1101	1	640
540	540	1110	1	540
480	480	1111	1	480

Note: (1) If GDSEL=L for GIP mode, the Vactive must be less than 1333 lines.

Table 5.1: Resolution table

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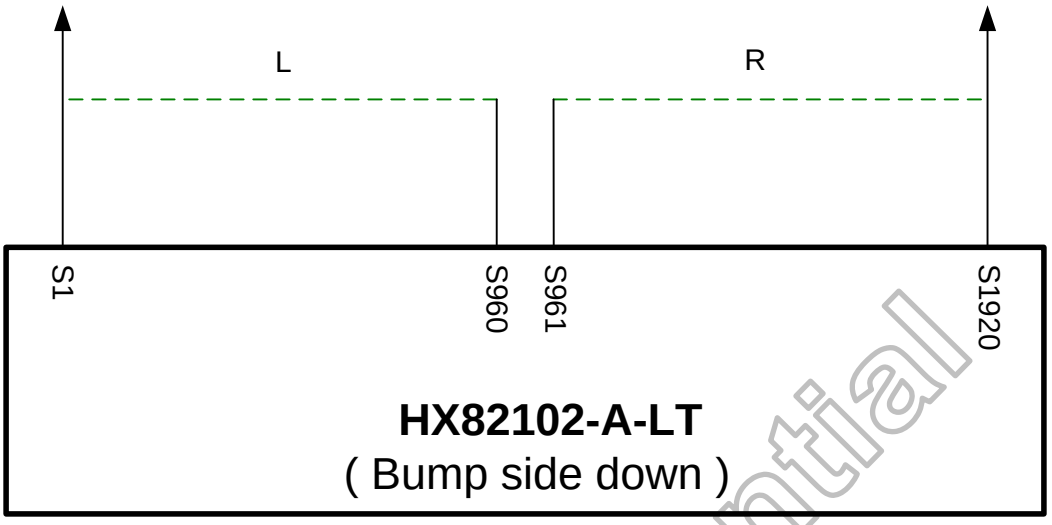
5.2. Source output channel valid range



Pixel	Master		Slave1		Slave2		Slave3	
	L	R	L	R	L	R	L	R
2560	S1~S960	S961~S1920	S1~S960	S961~S1920	S1~S960	S961~S1920	S1~S960	S961~S1920
1920	S1~S960	S961~S1920	S1~S960	S961~S1920	S1~S960	S961~S1920	X	X
1660	S1~S840	S1093~S1920	S1~S828	S1093~S1920	S1~S828	S1093~S1920	X	X
1560	S1~S780	S1141~S1920	S1~S780	S1141~S1920	S1~S780	S1141~S1920	X	X
1540	S1~S780	S1153~S1920	S1~S768	S1153~S1920	S1~S768	S1153~S1920	X	X
1440	S1~S720	S1201~S1920	S1~S720	S1201~S1920	S1~S720	S1201~S1920	X	X
1280	S1~S960	S961~S1920	S1~S960	S961~S1920	X	X	X	X
1024	S1~S768	S1153~S1920	S1~S768	S1153~S1920	X	X	X	X
960	S1~S720	S1201~S1920	S1~S720	S1201~S1920	X	X	X	X
800	S1~S600	S1321~S1920	S1~S600	S1321~S1920	X	X	X	X
720	S1~S540	S1381~S1920	S1~S540	S1381~S1920	X	X	X	X
640	S1~S960	S961~S1920	X	X	X	X	X	X
540	S1~S816	S1117~S1920	X	X	X	X	X	X
480	S1~S720	S1201~S1920	X	X	X	X	X	X

Table 5.2: MUX1:1 /single gate valid source output table

Pixel	Master		Slave1	
	L	R	L	R
2560	S1~S960	S961~S1920	S1~S960	S961~S1920
1920	S1~S720	S1201~S1920	S1~S720	S1201~S1920
1660	S1~S624	S1297~S1920	S1~S624	S1303~S1920
1560	S1~S588	S1339~S1920	S1~S588	S1339~S1920
1540	S1~S582	S1345~S1920	S1~S576	S1345~S1920
1440	S1~S540	S1381~S1920	S1~S540	S1381~S1920
1280	S1~S960	S961~S1920	X	X
1024	S1~S768	S1153~S1920	X	X
960	S1~S720	S1201~S1920	X	X
800	S1~S600	S1321~S1920	X	X
720	S1~S540	S1381~S1920	X	X
640	S1~S480	S1441~S1920	X	X
540	S1~S408	S1519~S1920	X	X
480	S1~S360	S1561~S1920	X	X

Table 5.3: MUX2:4 /dual gate valid source output table

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Pixel	Master		Slave1	
	L	R	L	R
2560	S1~S640	S1281~S1920	S1~S640	S1281~S1920
1920	S1~S960	S961~S1920	X	X
1660	S1~S832	S1093~S1920	X	X
1560	S1~S780	S1141~S1920	X	X
1540	S1~S772	S1153~S1920	X	X
1440	S1~S720	S1201~S1920	X	X
1280	S1~S640	S1281~S1920	X	X
1024	S1~S514	S1411~S1920	X	X
960	S1~S480	S1441~S1920	X	X
800	S1~S400	S1521~S1920	X	X
720	S1~S360	S1561~S1920	X	X
640	S1~S322	S1603~S1920	X	X
540	S1~S270	S1651~S1920	X	X
480	S1~S240	S1681~S1920	X	X

Table 5.4: MUX2:6 /triple gate valid source output table

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5.3. Panel structure

The HX82102-A-LT can support 5 types of driving method – stripe and zig-zag panel. User could set input pin PTS[2:0] and ZZS[1:0] to select panel type as following figures.

5.3.1. Single gate application

A. PTS[2:0] = 3'b011 and ZZS[1:0] = 2'b00/2'b11 for stripe panel.

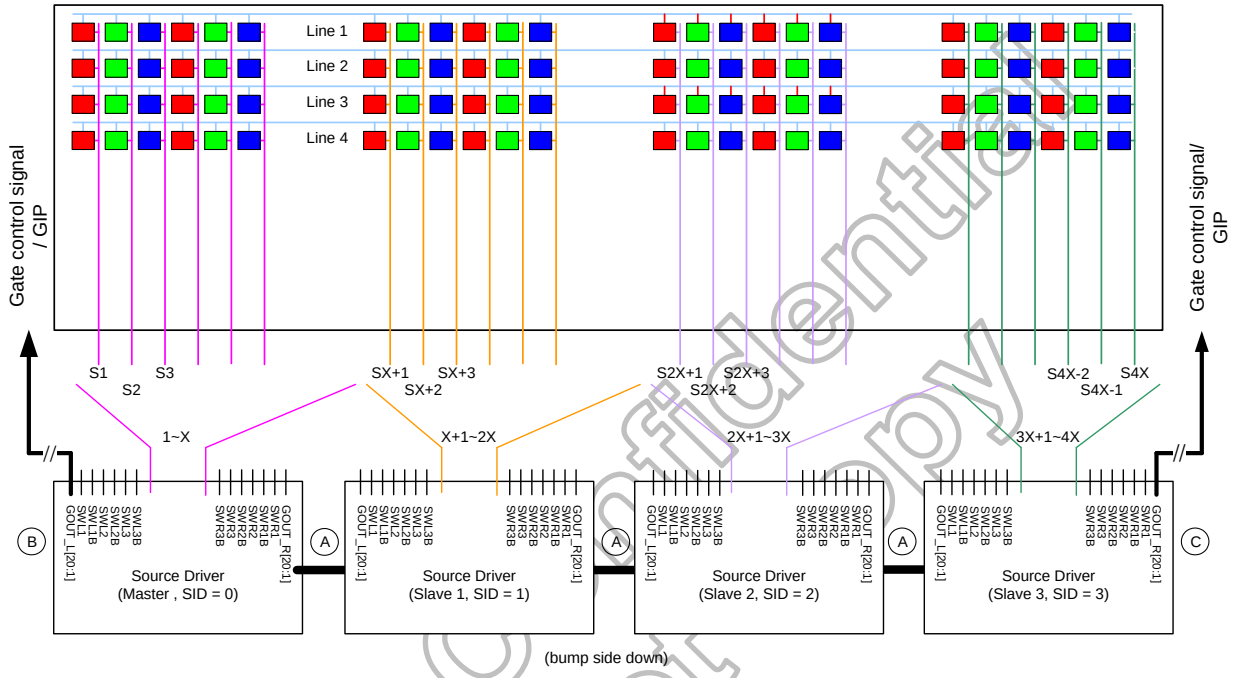

Figure 5.1: Single gate with Stripe panel application

B. PTS[2:0] = 3'b011 and ZZS[1:0] = 2'b01 for Zig-zag type1 panel.

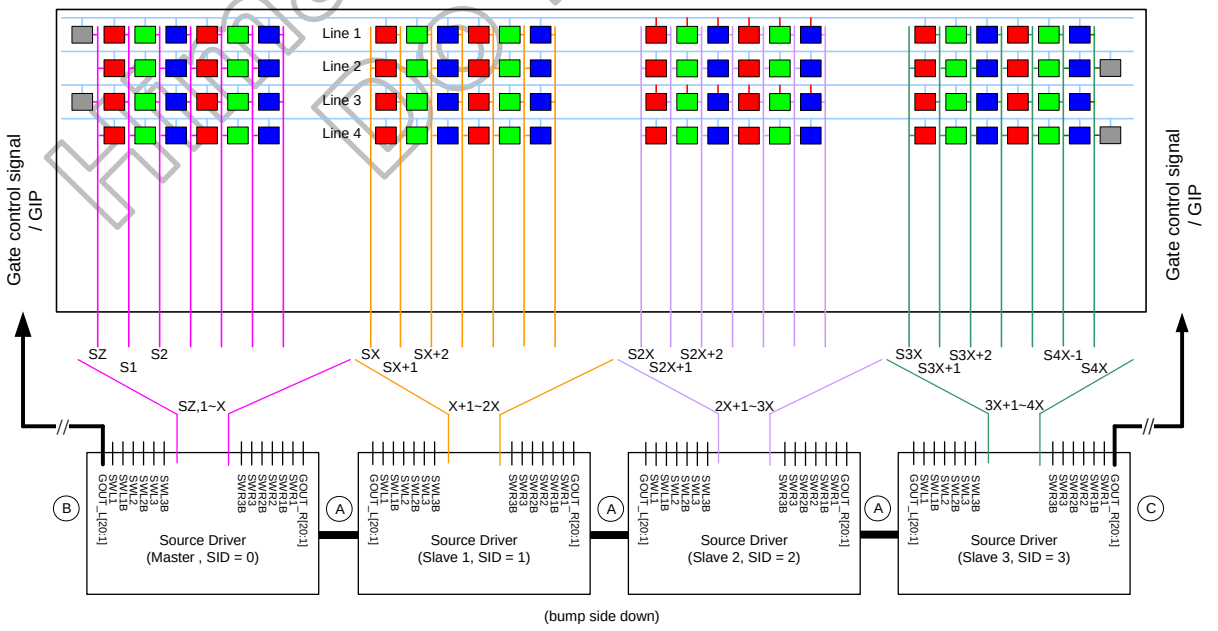

Figure 5.2: Single gate with Zig-zag type1 panel application

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C. PTS[2:0] = 3'b011 and ZZS[1:0] = 2'b10 for Zig-zag type2 panel.

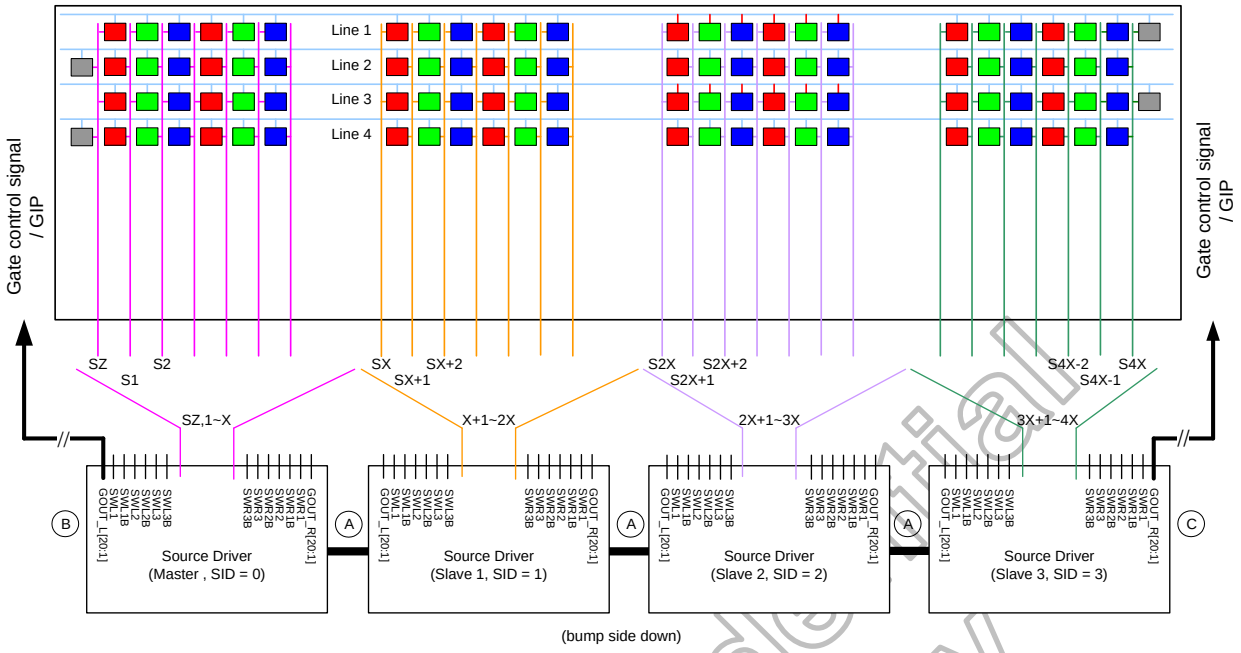

Figure 5.3: Single gate with Zig-zag type2 panel application

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5.3.2. Dual gate application

A. PTS[2:0] = 3'b100 and ZZS[1:0] = 2'b00 for stripe panel.

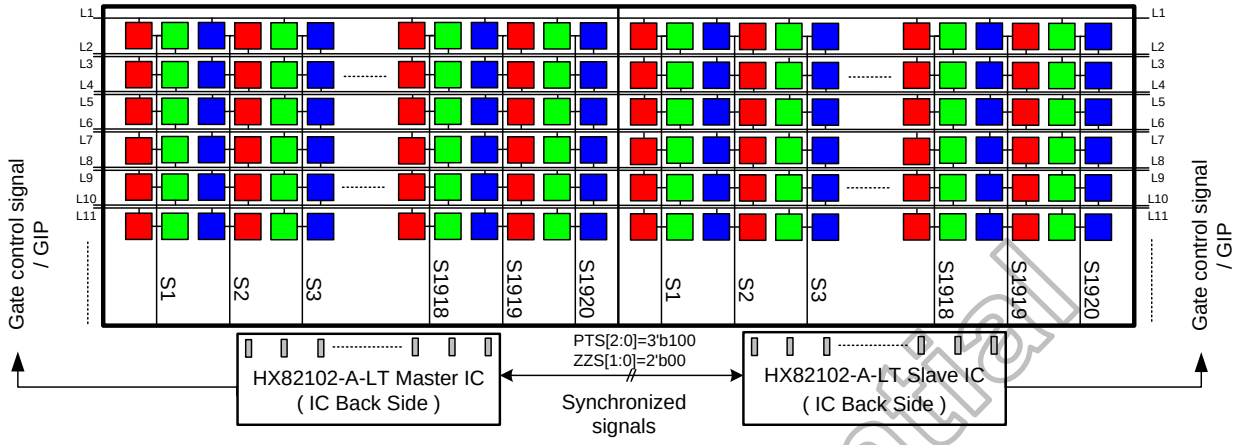

Figure 5.4: Dual gate with stripe panel application

B. PTS[2:0] = 3'b100 and ZZS[1:0] = 2'b01 for Zig-zag type1 panel.

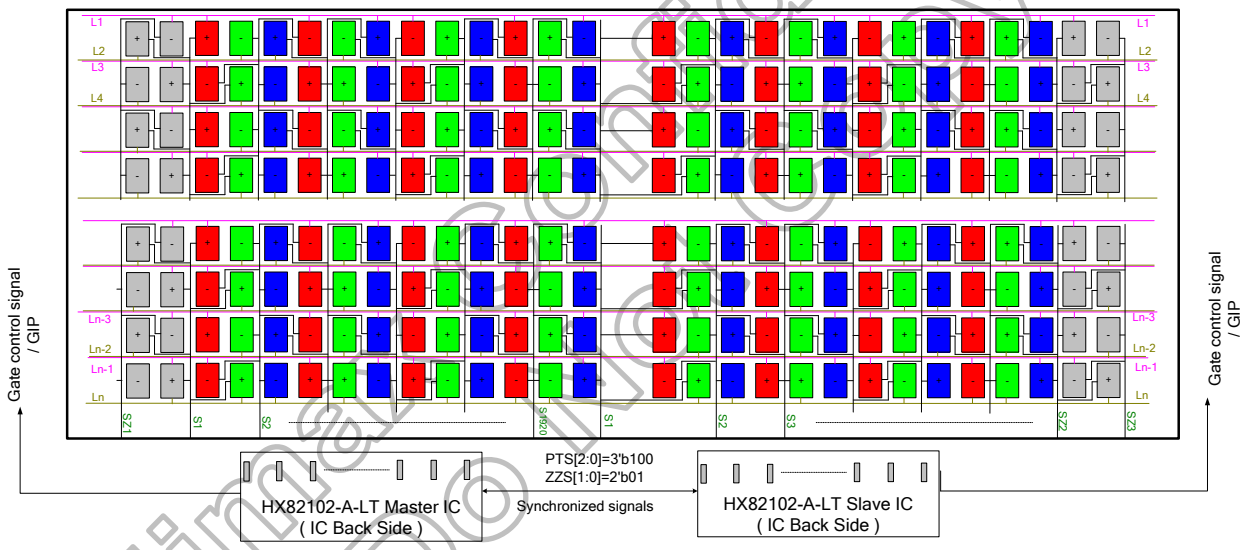

Figure 5.5: Dual gate with Zig-zag type1 panel application

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C. PTS[2:0] = 3’b100 and ZZS[1:0] = 2’b10 for Zig-zag type2panel.

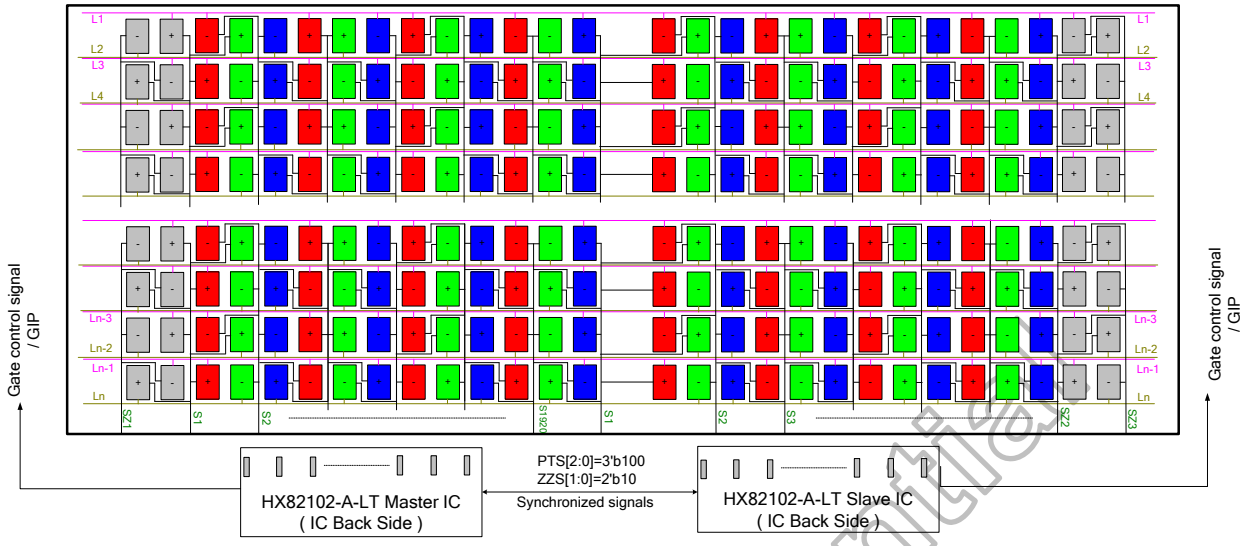

Figure 5.6: Dual gate with Zig-zag type2 panel application

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5.3.3. Triple gate application

A. PTS[2:0] = 3'b101 and ZZS[1:0] = 2'b00 for stripe panel.

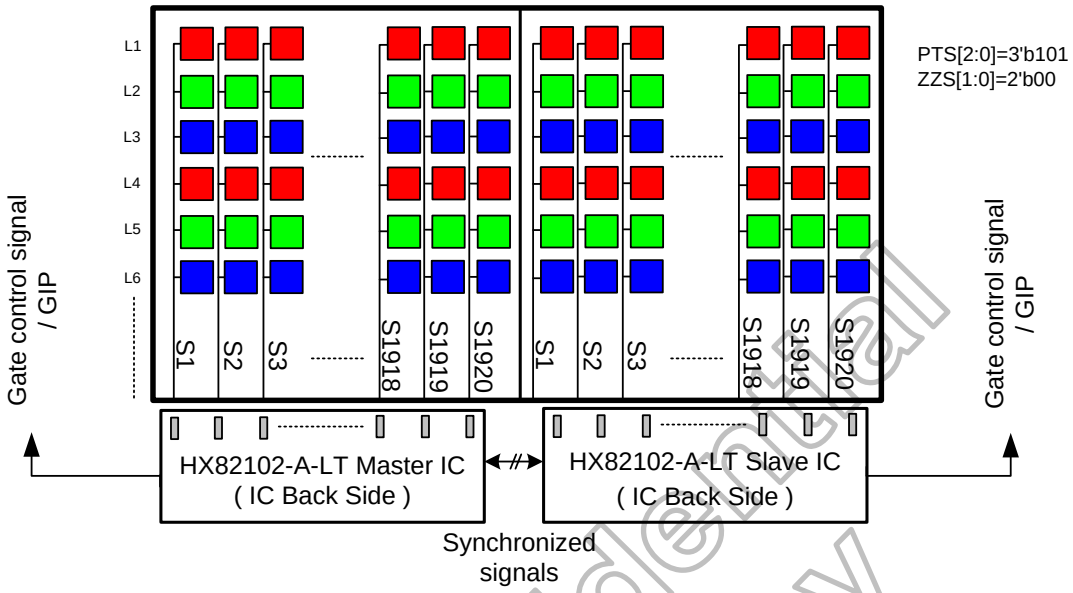

Figure 5.7: Triple gate with stripe panel application

B. PTS[2:0] = 3'b101 and ZZS[1:0] = 2'b01 for Zig-zag type1 panel.

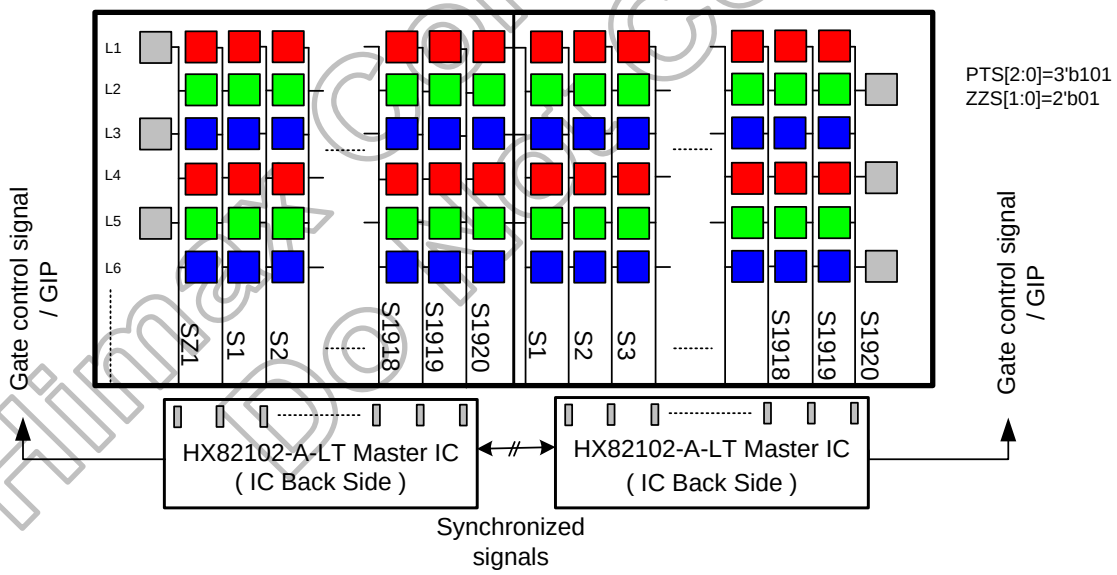

Figure 5.8: Triple gate with Zig-zag type1 panel application

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C. PTS[2:0] = 3’b101 and ZZS[1:0] = 2’b10 for Zig-zag type2 panel.

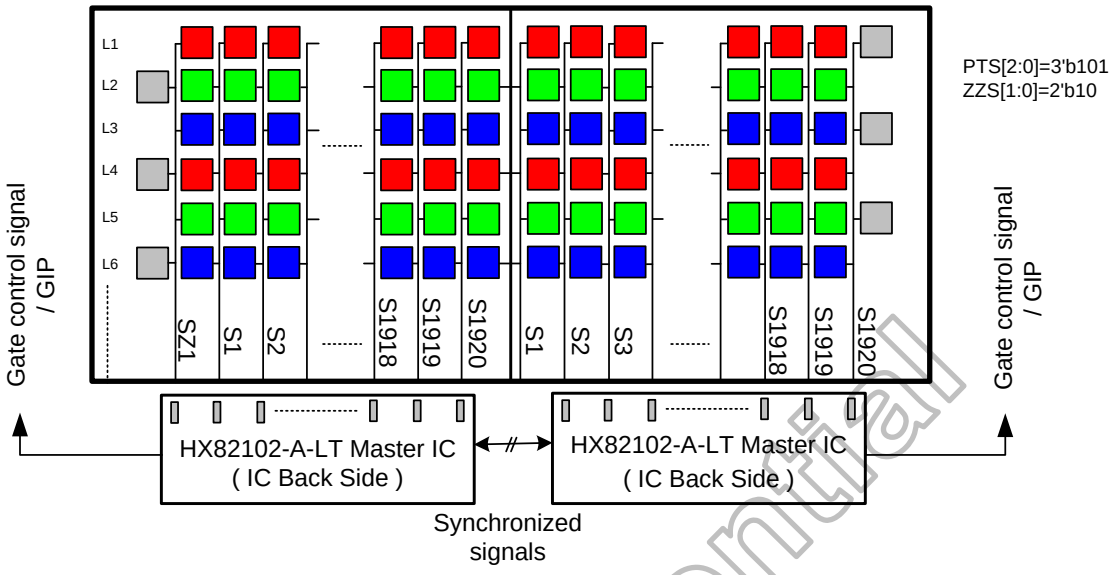

Figure 5.9: Triple gate with Zig-zag type2 panel application

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5.3.4. MUX 2:4 application

A. PTS[2:0] = 3'b000 and ZZS[1:0] = 2'b00/11 for stripe panel.

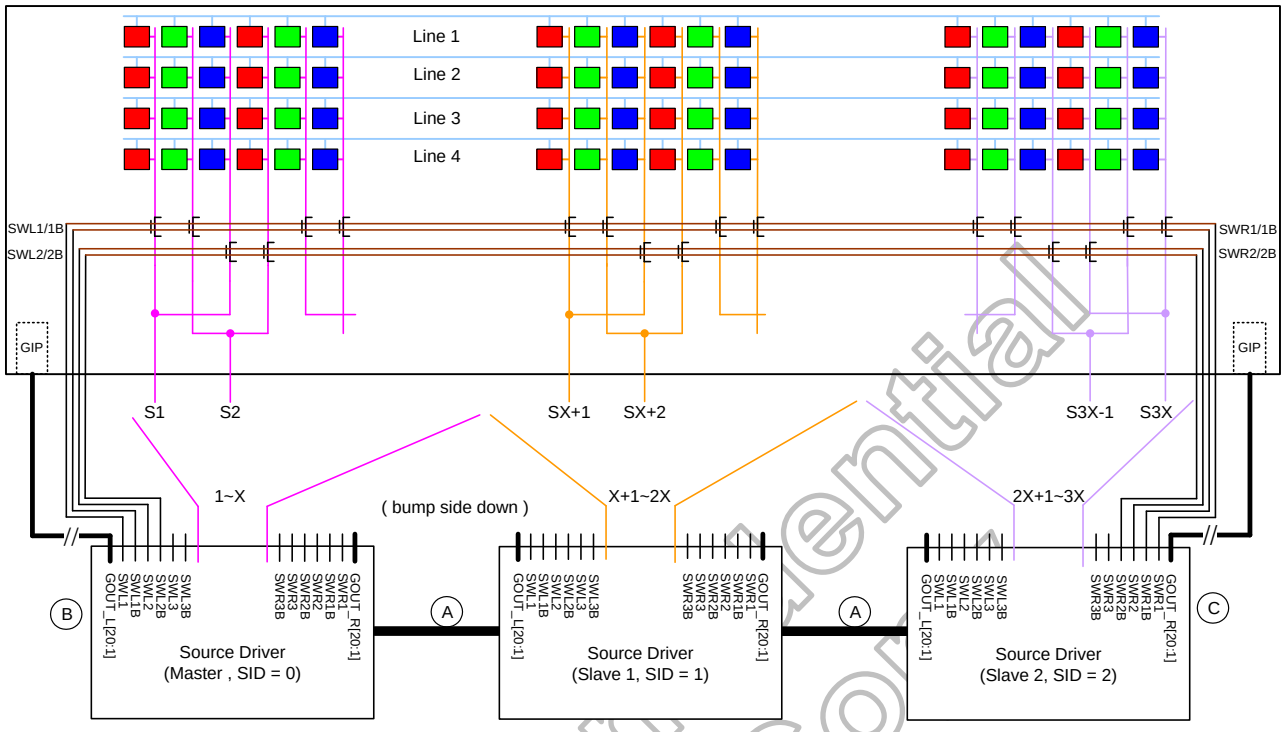

Figure 5.10: MUX2:4 with stripe panel application

B. PTS[2:0] = 3'b000 and ZZS[1:0] = 2'b01 for Zig-zag panel.

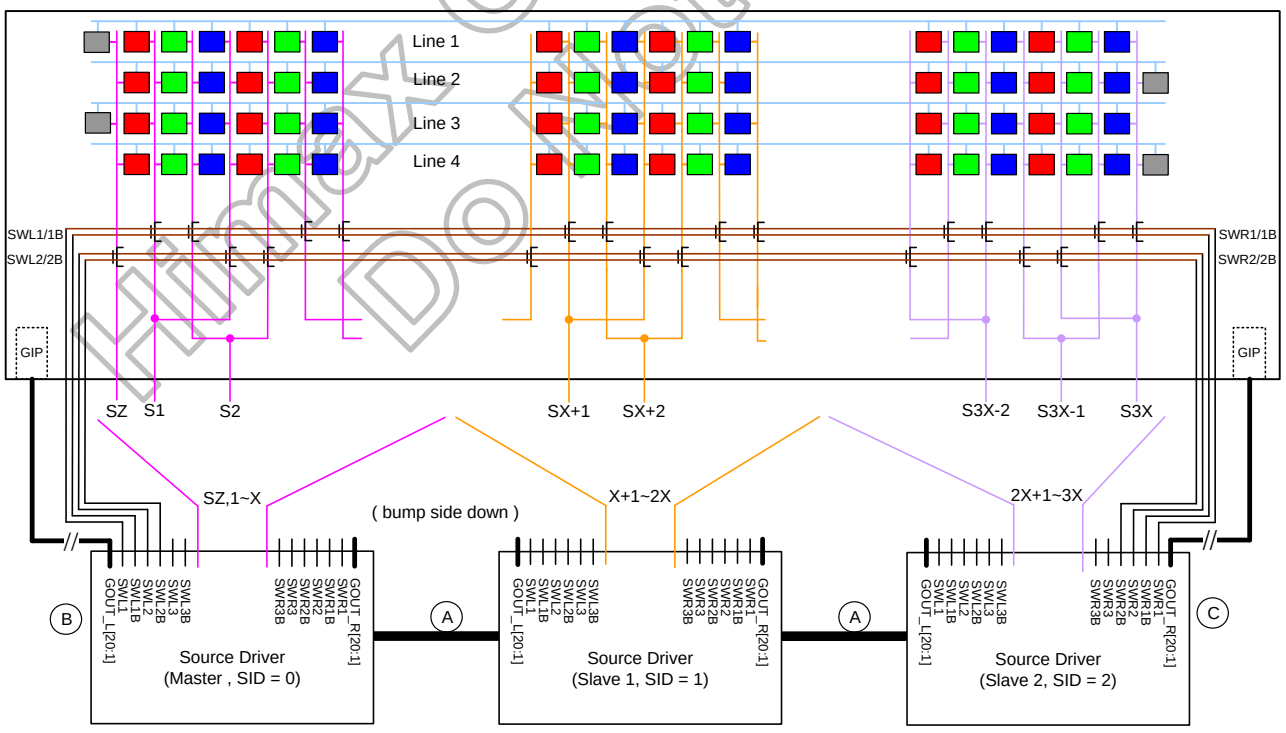

Figure 5.11: MUX2:4 with Zig-zag type1 panel application

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C. PTS[2:0] = 3'b000 and ZZS[1:0] = 2'b10 for Zig-zag panel.

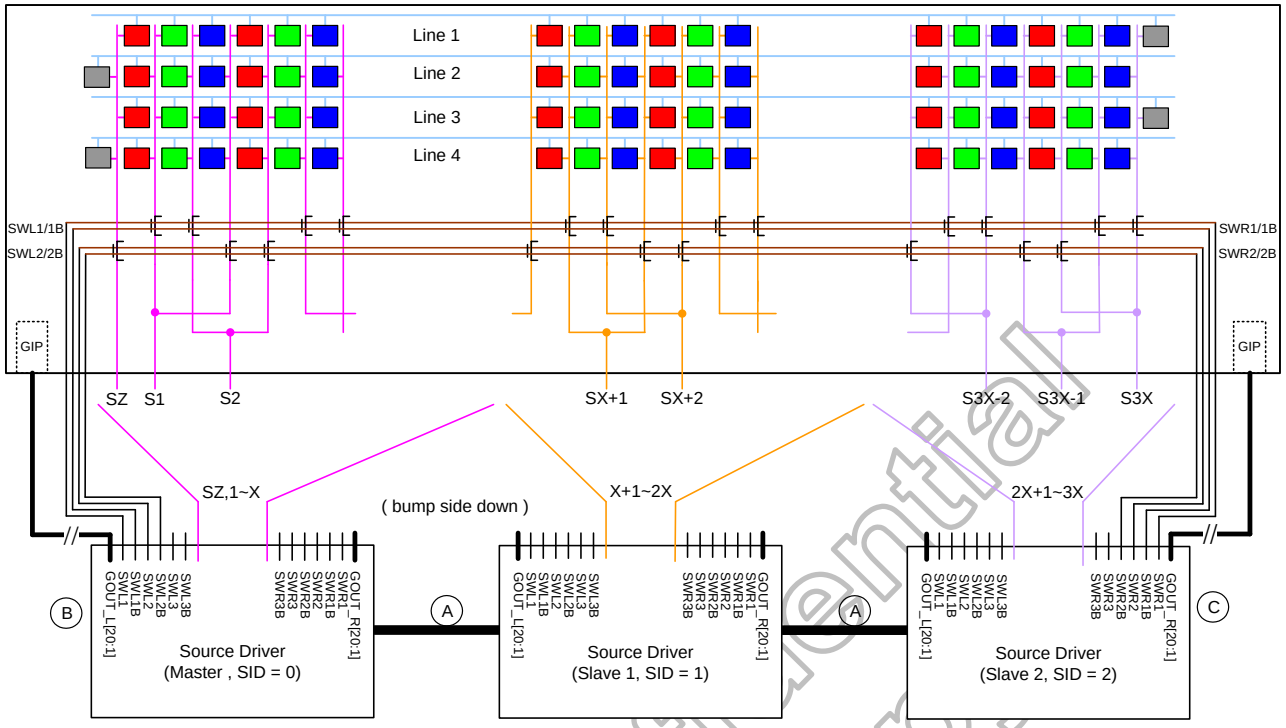

Figure 5.12: MUX2:4 with Zig-zag type2 panel application

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5.3.5. MUX 2:6 type1 application

A. PTS[2:0] = 3'b001 and ZZS[1:0] = 2'b00/11 for stripe panel.

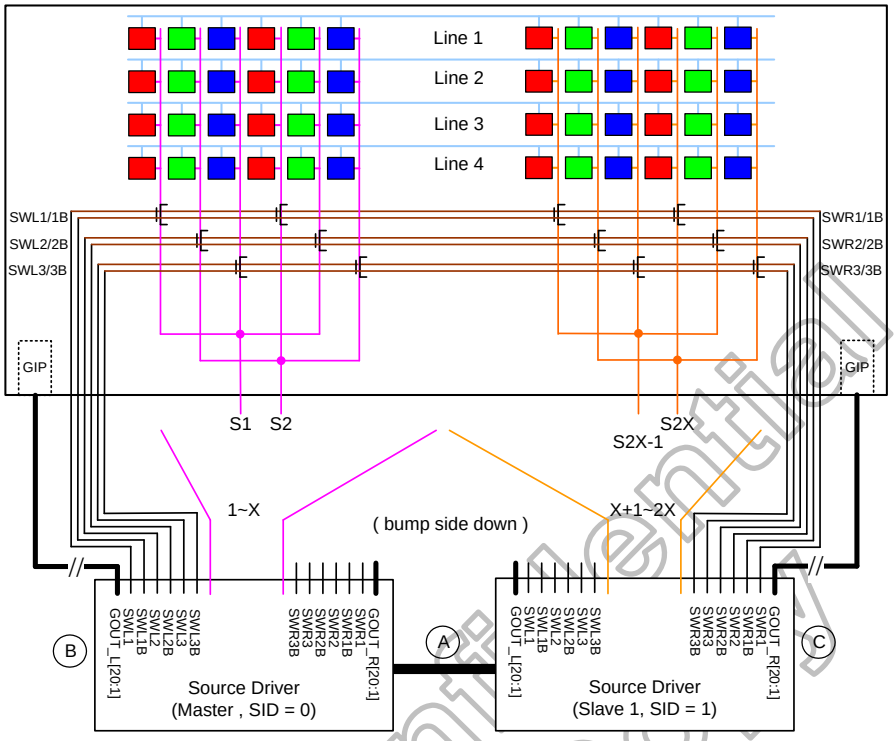

Figure 5.13: MUX2:6 type1 with stripe panel application

B. PTS[2:0] = 3'b001 and ZZS[1:0] = 2'b01 for Zig-zag panel.

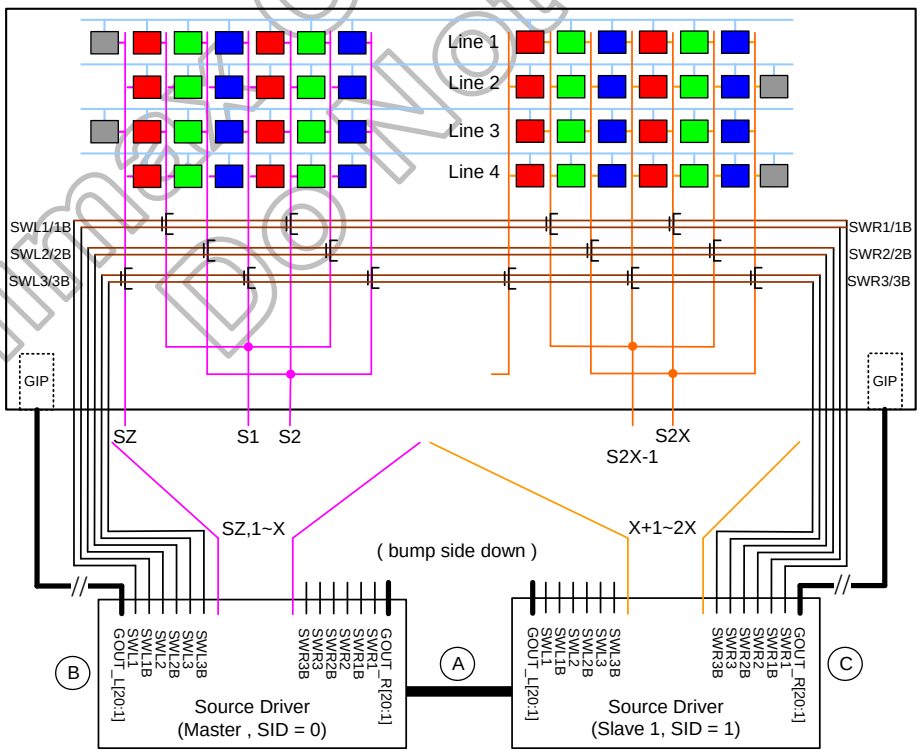

Figure 5.14: MUX2:6 type1 with Zig-zag type1 panel application

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C. PTS[2:0] = 3'b001 and ZZS[1:0] = 2'b10 for Zig-zag panel.

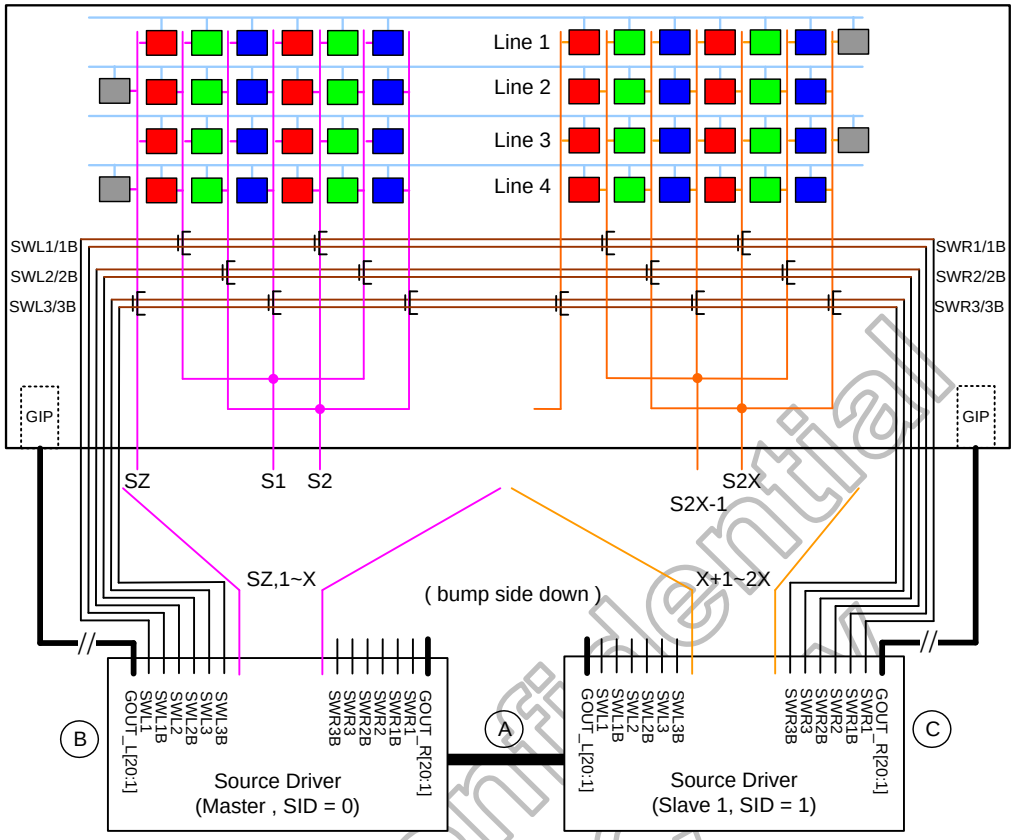

Figure 5.15: MUX2:6 type1 with Zig-zag type2 panel application

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5.3.6. MUX 2:6 type 2 application

A. PTS[2:0] = 3'b010 and ZZS[1:0] = 2'b00/11 for stripe panel.

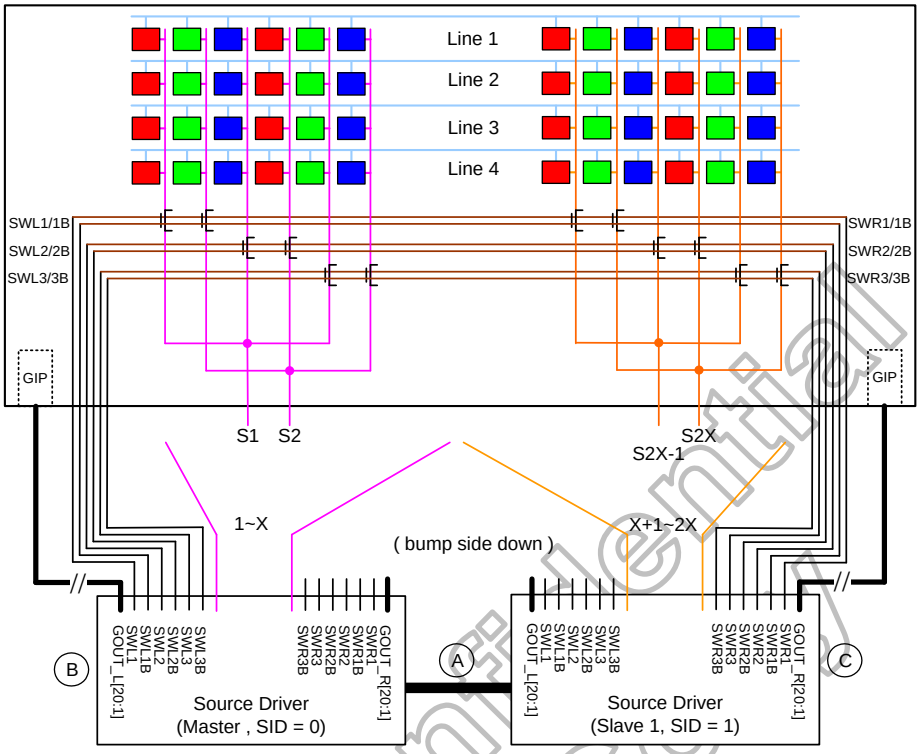

Figure 5.16: MUX2:6 type 2 with stripe panel application

B. PTS[2:0] = 3'b010 and ZZS[1:0] = 2'b01 for Zig-zag panel.

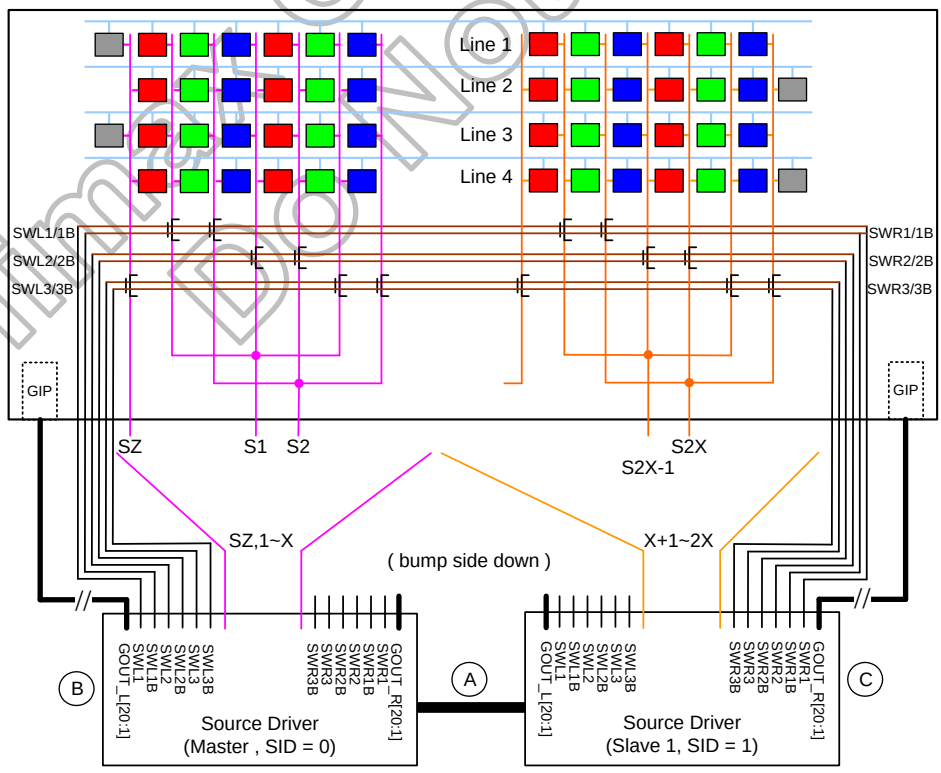

Figure 5.17: MUX2:6 type 2 with Zig-zag type1 panel application

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C. PTS[2:0] = 3'b010 and ZZS[1:0] = 2'b10 for Zig-zag panel.

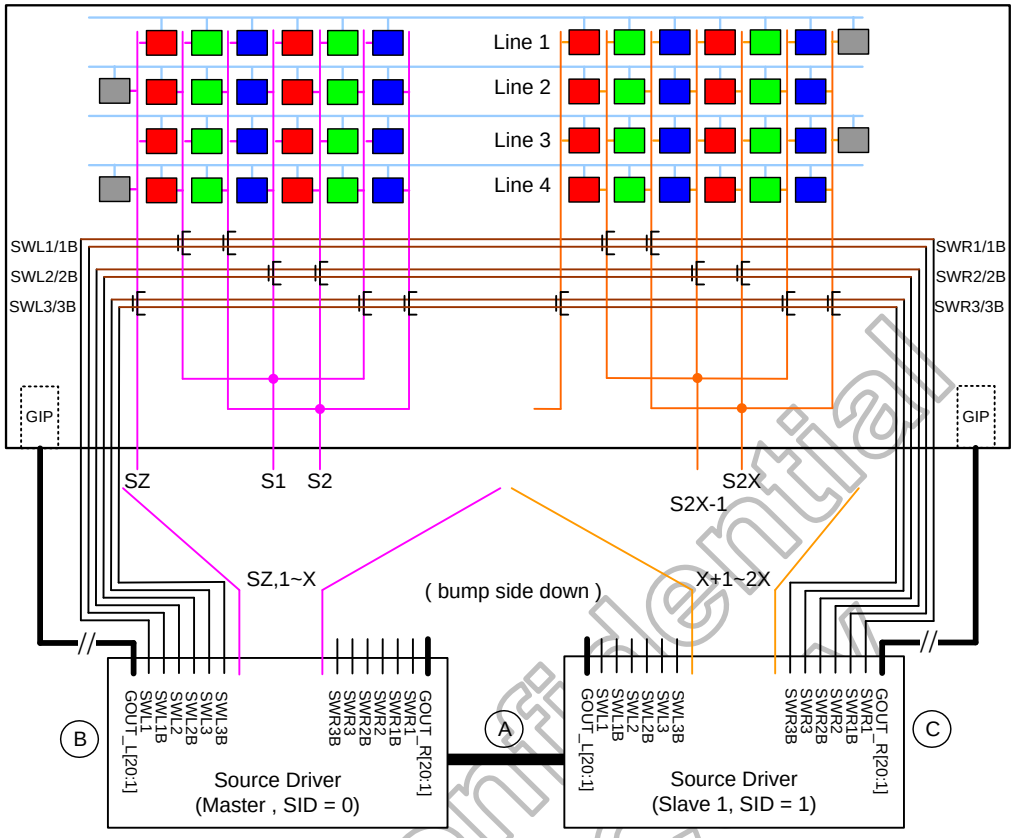

Figure 5.18: MUX2:6 type 2 with Zig-zag type2 panel application

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5.4. Cascade connection

5.4.1. Gate driver arrangement on panel

The pictures below show how source drivers and gate drivers are located on panel. "X" represents output channels per chip.

A. Gate driver**(s)** at the left side of the panel **(GPOS[1:0]=2'b00)**.

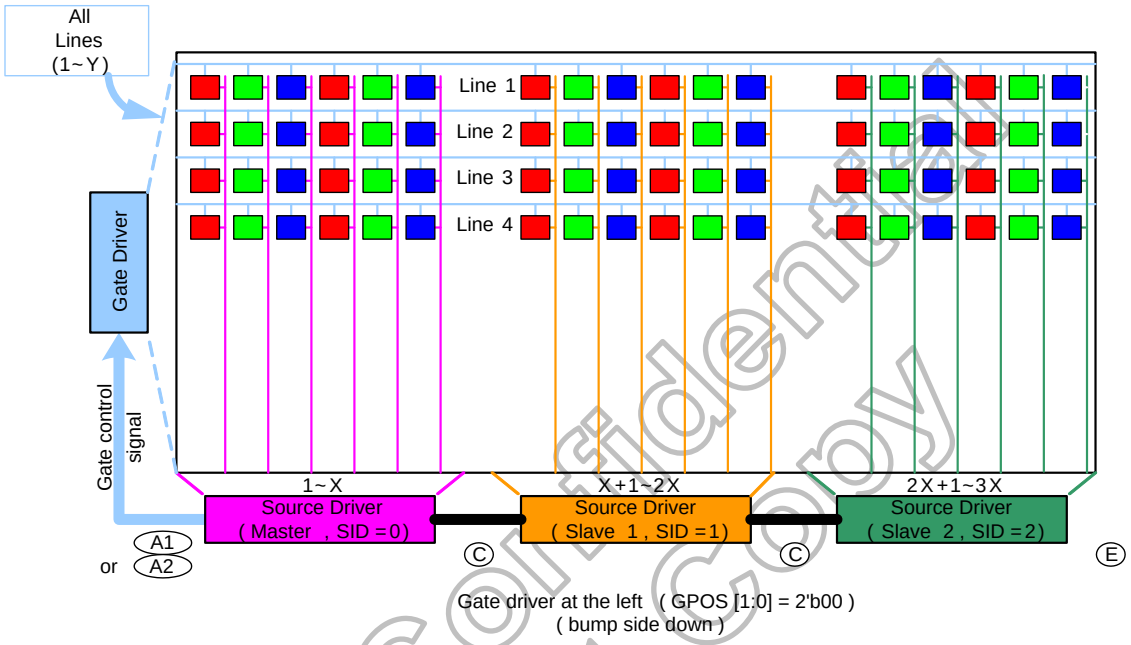

Figure 5.19: Gate driver(s) at the left side of the panel

B. Gate driver**(s)** at the right side of the panel **(GPOS[1:0]=2'b01)**.

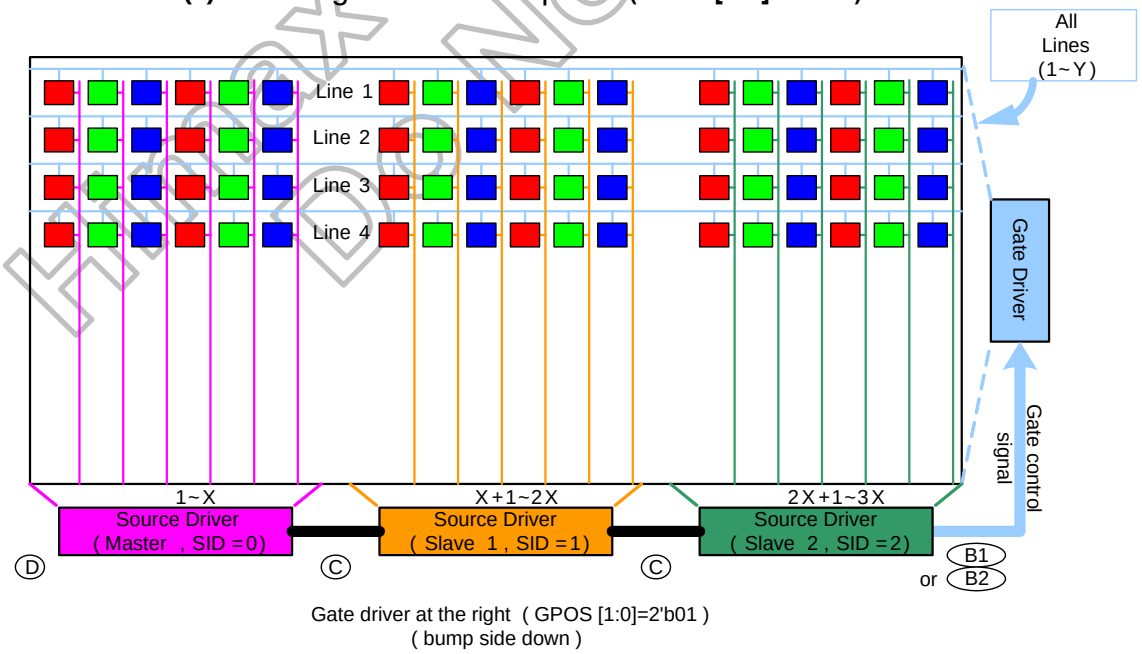

Figure 5.20: Gate driver(s) is at the right side of the panel

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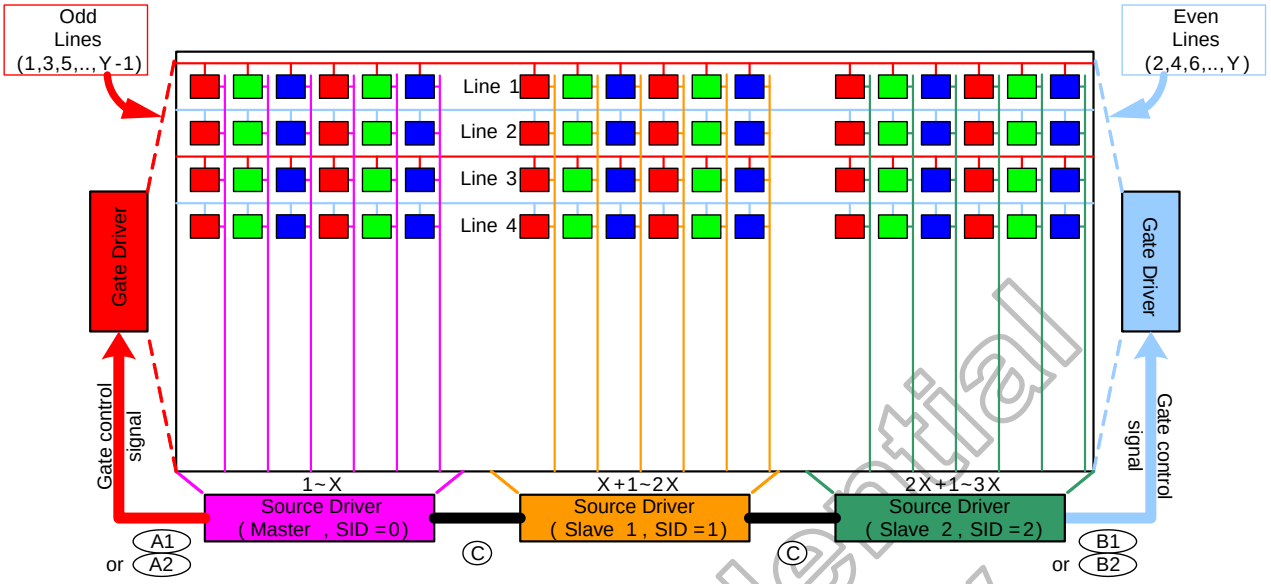
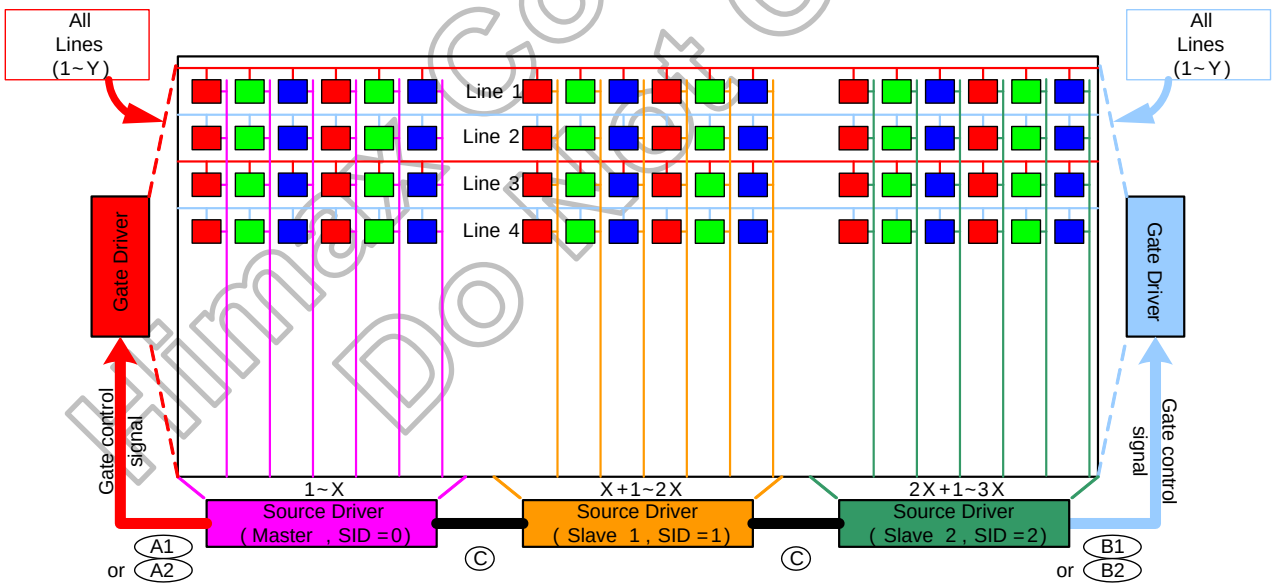
C. Gate drivers at the dual side of the panel. The left gate driver**(s)** controls the odd lines, and the right gate driver**(s)** controls the even lines **(GPOS[1:0]=2'b10)**.



Gate drivers at both sides, interlaced (GPOS [1:0] = 2'b10)
(bump side down)

Figure 5.21: Gate driver(s) at both sides of the panel, interlaced driving

D. Gate drivers at both sides of the panel. The left and the right gate drivers control the same lines at the same time **(GPOS[1:0]=2'b11)**.



Gate drivers at both sides, dual-side driving (GPOS [1:0] = 2'b11)
(bump side down)

Figure 5.22: Gate driver(s) at both sides of the panel, dual-side driving

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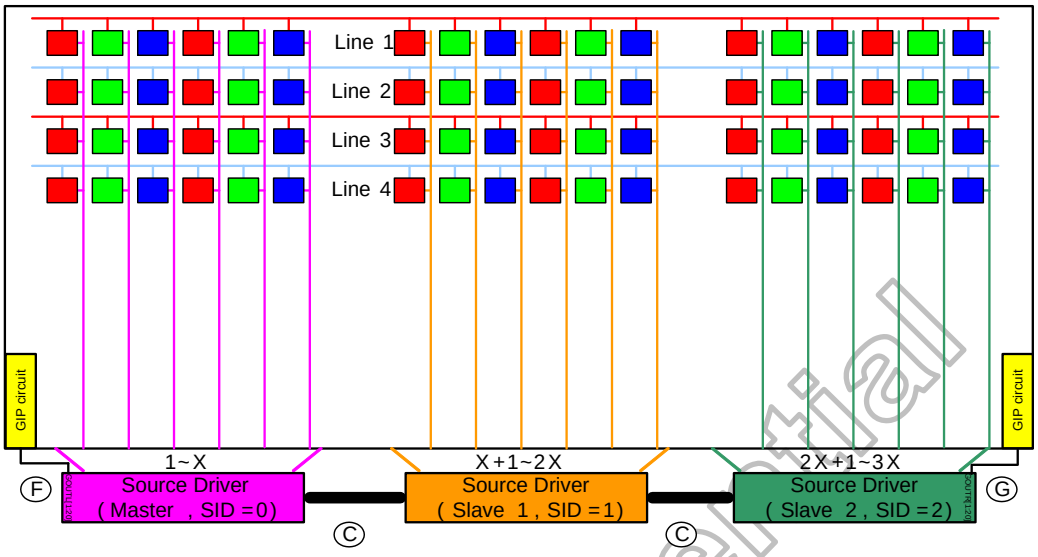
E. GIP mode selected **(GDSEL=L)**. The GOUTL/R[20:1] signals are set by registers. And support Left /Right/Dual side driving.



GIP mode (GDSEL=L), left/right/dual side driving
(bump side down)

Figure 5.23: GIP mode, left/right/dual side driving

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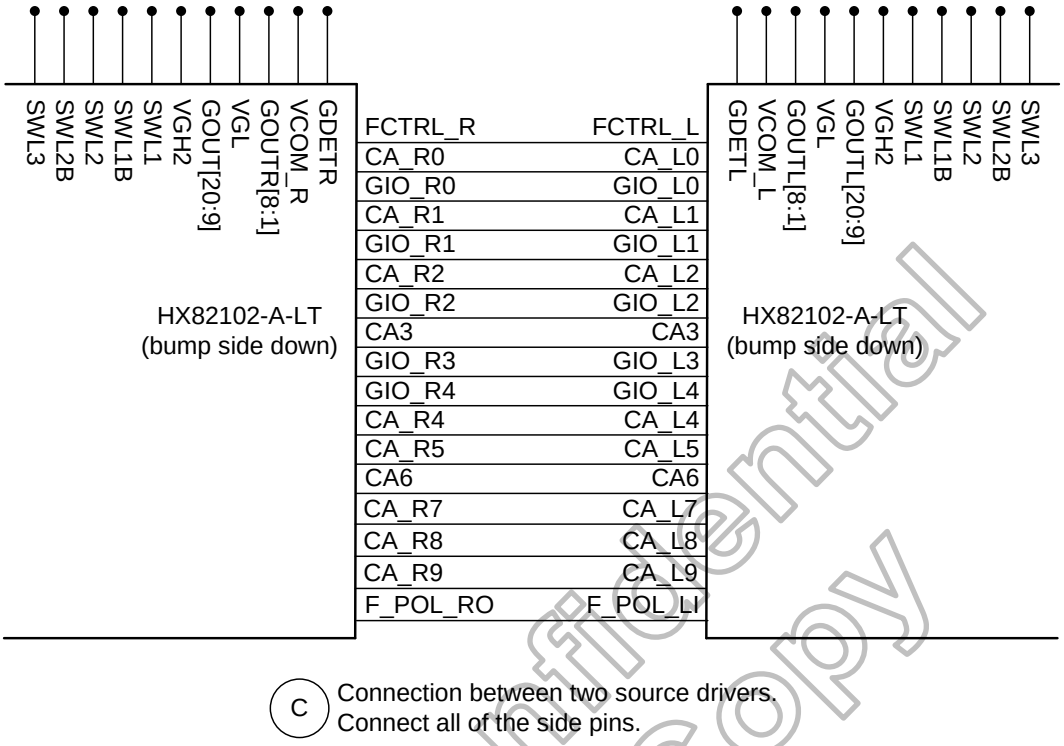
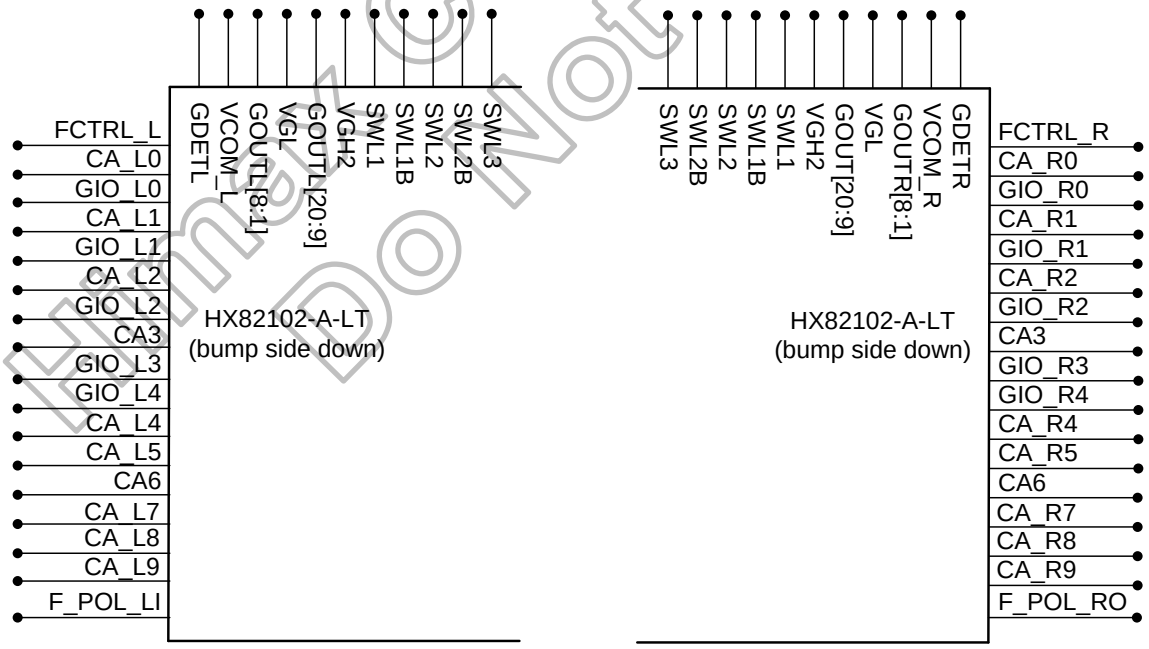
5.4.2. Cascade control interface

A. Between each source drivers, it is suggested to connect all of the side pins **(Case A)**.



C Connection between two source drivers.
Connect all of the side pins.



D Connection to nothing at the left side.
Leave all of the side pins open.

E Connection to nothing at the right side.
Leave all of the side pins open.

Figure 5.24: Cascade and GIP/SW control interface

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5.4.3. Gate driver type definition

Two type sequences of gate driver control pins are supported.

A. Type 1
GSQ should be set to L when using this type of gate driver, such as HX8660-B-LT, HX8677-C-LT and HX8678-A-LT. Note that CA_L2 and CA_R2 pins are used as up/down control.

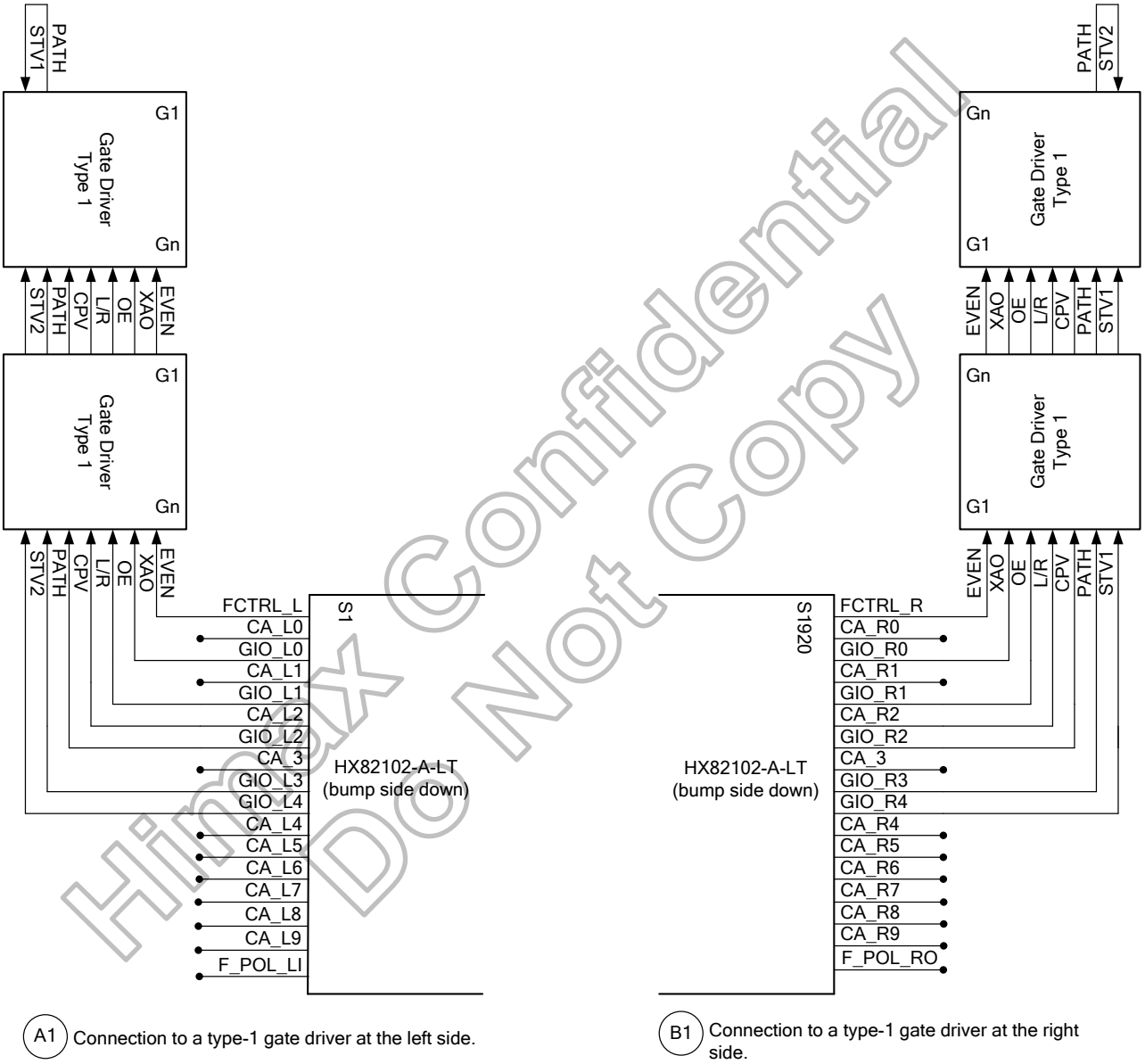

Figure 5.25: Gate control interface for type-1 gate drivers

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B. Type 2

GSQ should be set to H when using this type of gate driver such as HX8677-H. Note that CA_L0 and CA_R0 are used as up/down control.

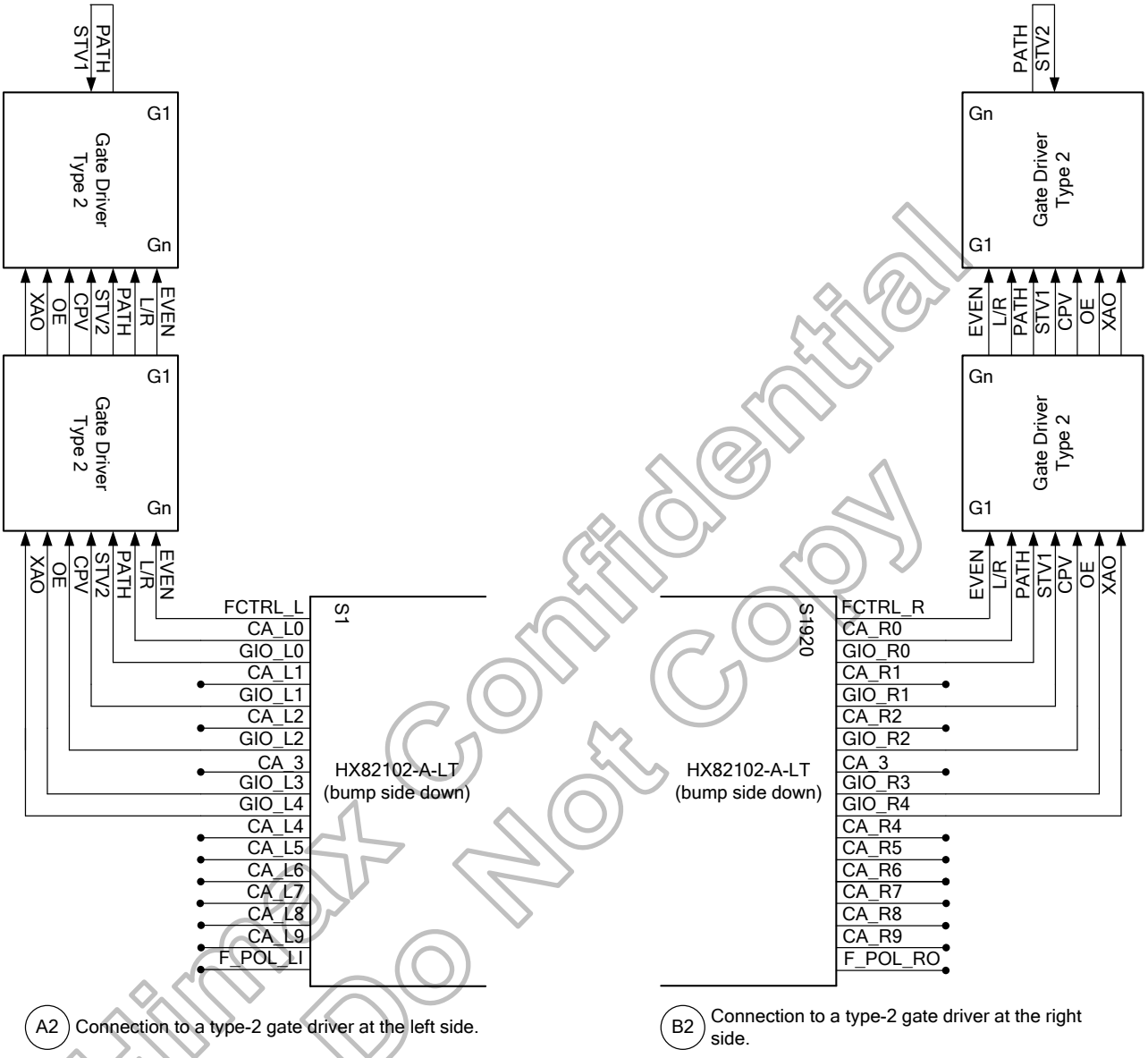

Figure 5.26: Gate control interface for type-2 gate drivers

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5.4.4. Gate driver signal definition

A. When only one source driver is used **(N=1)**, CA_L0/CA_L2/CA_R0/CA_R2 of the chip are used as UD.

	GSQ	GPOS [1:0]	TB	CA_L0 /UD	GIO_L 0	GIO_L 1	CA_L2 /UD	GIO_L 2	GIO_L 3	GIO_L 4	CA_R0 /UD	GIO_R 0	GIO_R 1	CA_R2 /UD	GIO_R 2	GIO_R 3	GIO_R 4
Master (single chip)	0	00	0	0	/XAO	OEV	0	CPV	Input **(HZ)**	STV	1	/XAO	0	1	0	0	0
			1	1	/XAO	OEV	1	CPV	STV	Input **(HZ)**	0	/XAO	0	0	0	0	0
		01	0	0	0	0	0	0	0	0	1	/XAO	OEV	1	CPV	Input **(HZ)**	STV
			1	1	0	0	1	0	0	0	0	/XAO	OEV	0	CPV	STV	Input **(HZ)**
		10	0	0	/XAO	OEV_B	0	CPV_B	Input **(HZ)**	STV_B	1	/XAO	OEV_A	1	CPV_A	Input **(HZ)**	STV_A
			1	1	/XAO	OEV_A	1	CPV_A	STV_A	Input **(HZ)**	0	/XAO	OEV_B	0	CPV_B	STV_B	Input **(HZ)**
		11	0	0	/XAO	OEV	0	CPV	Input **(HZ)**	STV	1	/XAO	OEV	1	CPV	Input **(HZ)**	STV
			1	1	/XAO	OEV	1	CPV	STV	Input **(HZ)**	0	/XAO	OEV	0	CPV	STV	Input **(HZ)**
	1	00	0	0	Input **(HZ)**	STV	0	CPV	OEV	/XAO	1	0	0	1	0	0	/XAO
			1	1	STV	Input **(HZ)**	1	CPV	OEV	/XAO	0	0	0	0	0	0	/XAO
		01	0	0	0	0	0	0	0	0	1	Input **(HZ)**	STV	1	CPV	OEV	/XAO
			1	1	0	0	1	0	0	0	0	STV	Input **(HZ)**	0	CPV	OEV	/XAO
		10	0	0	Input **(HZ)**	STV_B	0	CPV_B	OEV_B	/XAO	1	Input **(HZ)**	STV_A	1	CPV_A	OEV_A	/XAO
			1	1	STV_A	Input **(HZ)**	1	CPV_A	OEV_A	/XAO	0	STV_B	Input **(HZ)**	0	CPV_B	OEV_B	/XAO
		11	0	0	Input **(HZ)**	STV	0	CPV	OEV	/XAO	1	Input **(HZ)**	STV	1	CPV	OEV	/XAO
			1	1	STV	Input **(HZ)**	1	CPV	OEV	/XAO	0	STV	Input **(HZ)**	0	CPV	OEV	/XAO

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B. When source drivers are cascaded **(N>1)**: CA_L0 and CA_L2 of the master chip **(SID=0)** are used as UD. CA_R0 and CA_R2 are used as cascade control.

	GSQ	GPOS [1:0]	TB	CA_L0 /UD	GIO_L 0	GIO_L 1	CA_L2 /UD	GIO_L 2	GIO_L 3	GIO_L 4	CA_R0 /UD	GIO_R 0	GIO_R 1	CA_R2 /UD	GIO_R 2	GIO_R 3	GIO_R 4
Master (cascaded)	0	00	0	0	/XAO	OEV	0	CPV	Input **(HZ)**	STV	CA0	/XAO	0	CA2	0	0	0
			1	1	/XAO	OEV	1	CPV	STV	Input **(HZ)**	CA0	/XAO	0	CA2	0	0	0
		01	0	0	0	0	0	0	0	0	CA0	/XAO	OEV	CA2	CPV	input **(HZ)**	STV
			1	1	0	0	1	0	0	0	CA0	/XAO	OEV	CA2	CPV	STV	Input **(HZ)**
		10	0	0	/XAO	OEV_B	0	CPV_B	Input **(HZ)**	STV_B	CA0	/XAO	OEV_A	CA2	CPV_A	Input **(HZ)**	STV_A
			1	1	/XAO	OEV_A	1	CPV_A	STV_A	Input **(HZ)**	CA0	/XAO	OEV_B	CA2	CPV_B	STV_B	Input **(HZ)**
		11	0	0	/XAO	OEV	0	CPV	Input **(HZ)**	STV	CA0	/XAO	OEV	CA2	CPV	Input **(HZ)**	STV
			1	1	/XAO	OEV	1	CPV	STV	Input **(HZ)**	CA0	/XAO	OEV	CA2	CPV	STV	Input **(HZ)**
	1	00	0	0	Input **(HZ)**	STV	0	CPV	OEV	/XAO	CA0	0	0	CA2	0	0	0
			1	1	STV	Input **(HZ)**	1	CPV	OEV	/XAO	CA0	0	0	CA2	0	0	0
		01	0	0	0	0	0	0	0	0	CA0	Input **(HZ)**	STV	CA2	CPV	OEV	/XAO
			1	1	0	0	1	0	0	0	CA0	STV	Input **(HZ)**	CA2	CPV	OEV	/XAO
		10	0	0	Input **(HZ)**	STV_B	0	CPV_B	OEV_B	/XAO	CA0	Input **(HZ)**	STV_A	CA2	CPV_A	OEV_A	/XAO
			1	1	STV_A	Input **(HZ)**	1	CPV_A	OEV_A	/XAO	CA0	STV_B	Input **(HZ)**	CA2	CPV_B	OEV_B	/XAO
		11	0	0	Input **(HZ)**	STV	0	CPV	OEV	/XAO	CA0	Input **(HZ)**	STV	CA2	CPV	OEV	/XAO
			1	1	STV	Input **(HZ)**	1	CPV	OEV	/XAO	CA0	STV	Input **(HZ)**	CA2	CPV	OEV	/XAO

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For the slave chips except the last one (SID=1 to N-2):

	GSQ	GPOS [1:0]	TB	CA_L0 /UD	GIO_L 0	GIO_L 1	CA_L2 /UD	GIO_L 2	GIO_L 3	GIO_L 4	CA_R0 /UD	GIO_R 0	GIO_R 1	CA_R2 /UD	GIO_R 2	GIO_R 3	GIO_R 4
Slaves except the last (cascaded)	0	00	0	Input (HZ)							CA0	GIO_L0	GIO_L1	CA2	GIO_L2	Input (HZ)	GIO_L4
			1								CA0			CA2		GIO_L3	Input (HZ)
		01	0								CA0			CA2		Input (HZ)	GIO_L4
			1								CA0			CA2		GIO_L3	Input (HZ)
		1X	0								CA0			CA2		Input (HZ)	GIO_L4
			1								CA0			CA2		GIO_L3	Input (HZ)
	1	00	0	Input (HZ)							CA0	Input (HZ)	GIO_L1	CA2	GIO_L2	GIO_L3	GIO_L4
			1								CA0	GIO_L0	Input (HZ)	CA2			
		01	0								CA0	Input (HZ)	GIO_L1	CA2			
			1								CA0	GIO_L0	Input (HZ)	CA2			
		1X	0								CA0	Input (HZ)	GIO_L1	CA2			
			1								CA0	GIO_L0	Input (HZ)	CA2			

CA_R0 and CA_R2 of the last slave chip (SID=N-1) are used as UD:

	GSQ	GPOS [1:0]	TB	CA_L0 /UD	GIO_L 0	GIO_L 1	CA_L2 /UD	GIO_L 2	GIO_L 3	GIO_L 4	CA_R0 /UD	GIO_R 0	GIO_R 1	CA_R2 /UD	GIO_R 2	GIO_R 3	GIO_R 4
The last slave (cascaded)	0	00	0	Input (HZ)							1	GIO_L0	GIO_L1	1	GIO_L2	Input (HZ)	GIO_L4
			1								0			0		GIO_L3	Input (HZ)
		01	0								1			1		Input (HZ)	GIO_L4
			1								0			0		GIO_L3	Input (HZ)
		1X	0								1			1		Input (HZ)	GIO_L4
			1								0			0		GIO_L3	Input (HZ)
	1	00	0	Input (HZ)							1	Input (HZ)	GIO_L1	1	GIO_L2	GIO_L3	GIO_L4
			1								0	GIO_L0	Input (HZ)	0			
		01	0								1	Input (HZ)	GIO_L1	1			
			1								0	GIO_L0	Input (HZ)	0			
		1X	0								1	Input (HZ)	GIO_L1	1			
			1								0	GIO_L0	Input (HZ)	0			

Table 5.5: Gate driver signal definition table

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5.4.5. GIP control interface

The HX82102-A-LT has 20 output pins on each of right/left side for GIP circuit control use as shown below. Each of these output pins can assign signal by register setting **(Page0Fh ~ Page14h)** for satisfy the GIP signal output plan.

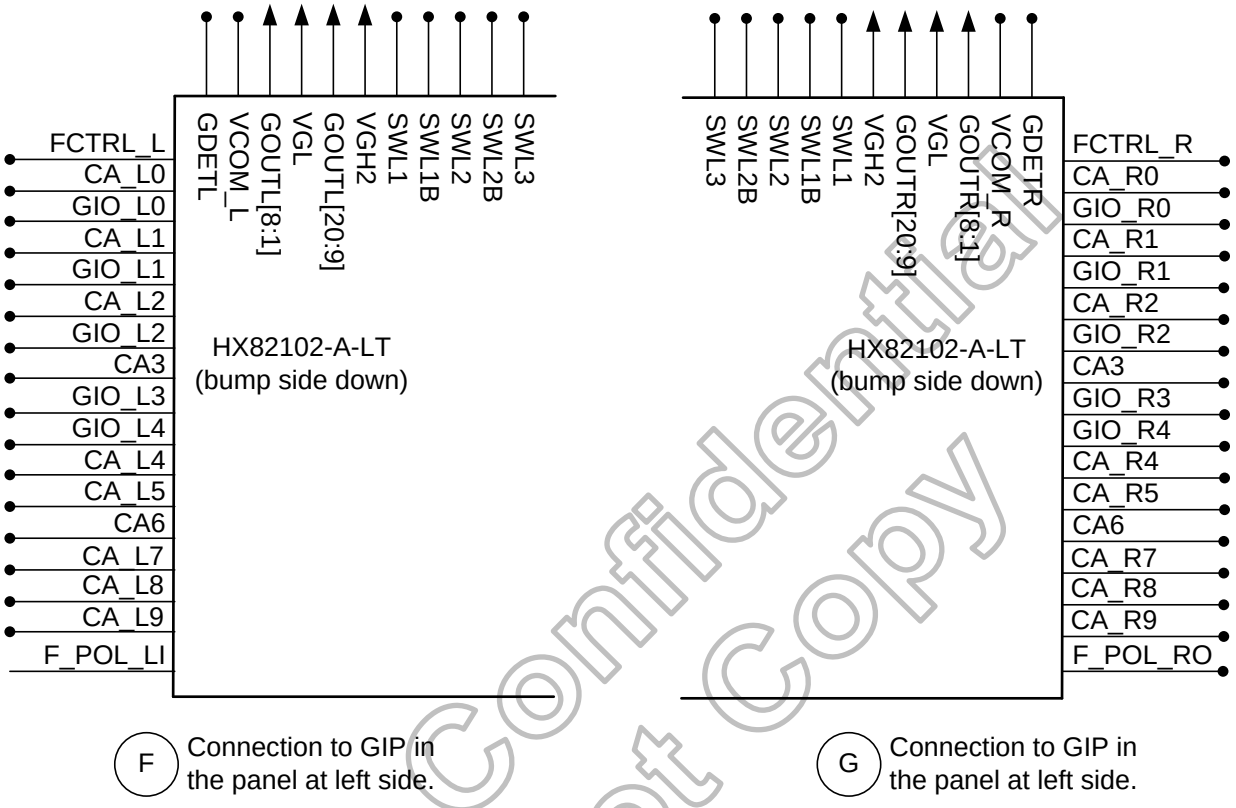

Figure 5.27: GIP control interface

5.4.6. Cascade design: Power application

A. The following voltages are provided by the master chip and should be connected to the slave chip:
   VSP, VSN, VGMPH, VGMPL, VGMNH, VGMNL.
B. The following voltages are provided by the master chip and do not need to connect to slave chip:
   VCOM.
C. The following voltages are provided by each chip with separate capacitors:
   VSDP, VSDN, VCL, VDDD, VDDIF.
D. The following voltages are provided by each chip with common capacitors:
   VSP, VSN, VGMPHI, VGMPLI, VGMNHI, VGMNLI.
E. Note that for the master chip, do not connect gamma voltage inputs VGMPHI / VGMPLI / VGMNHI / VGMNLI to VGMPHO / VGMPLO / VGMNHO / VGMNLO on panel, but connect them through FPC or PCB traces. This helps to reduce difference between gamma voltages of each chip.
F. VCOM can be connected to the panel through VCOM_L and VCOM_R pins of each chip.

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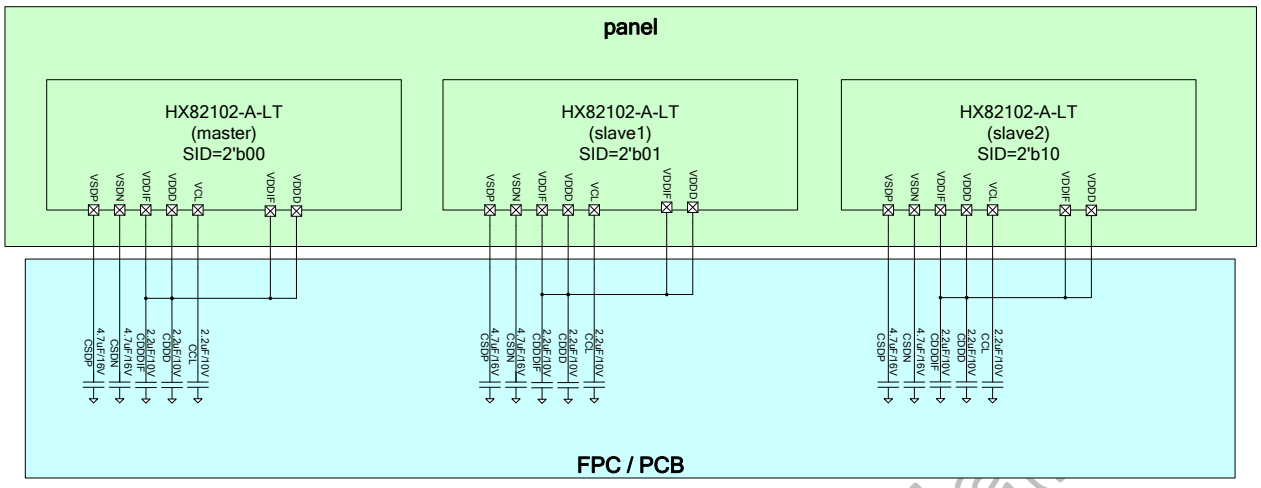

Figure 5.28: Cascade design for regulator outputs

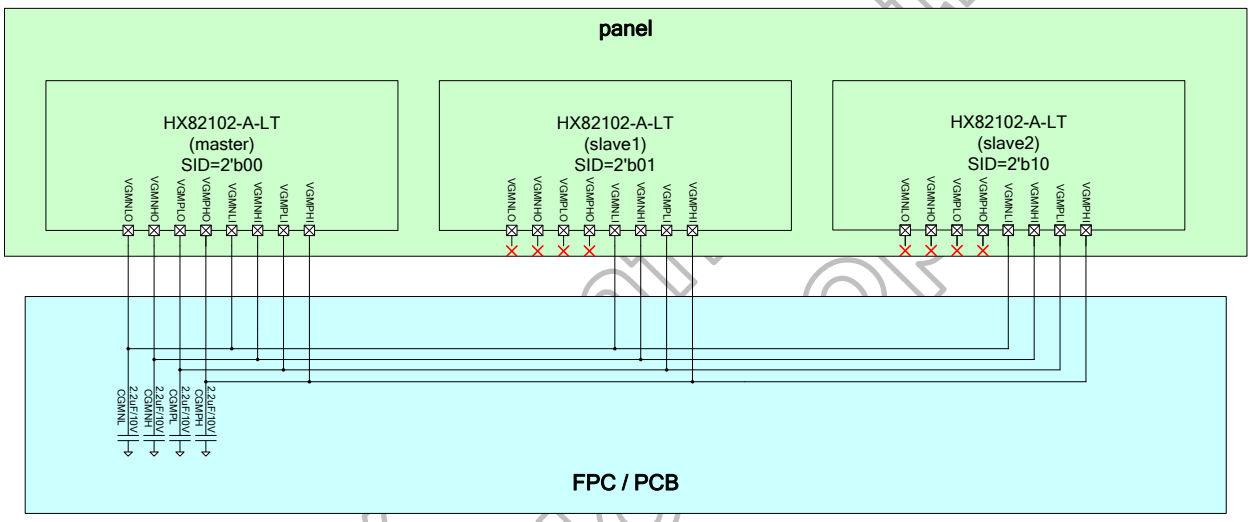

Figure 5.29: Cascade design for gamma reference voltages

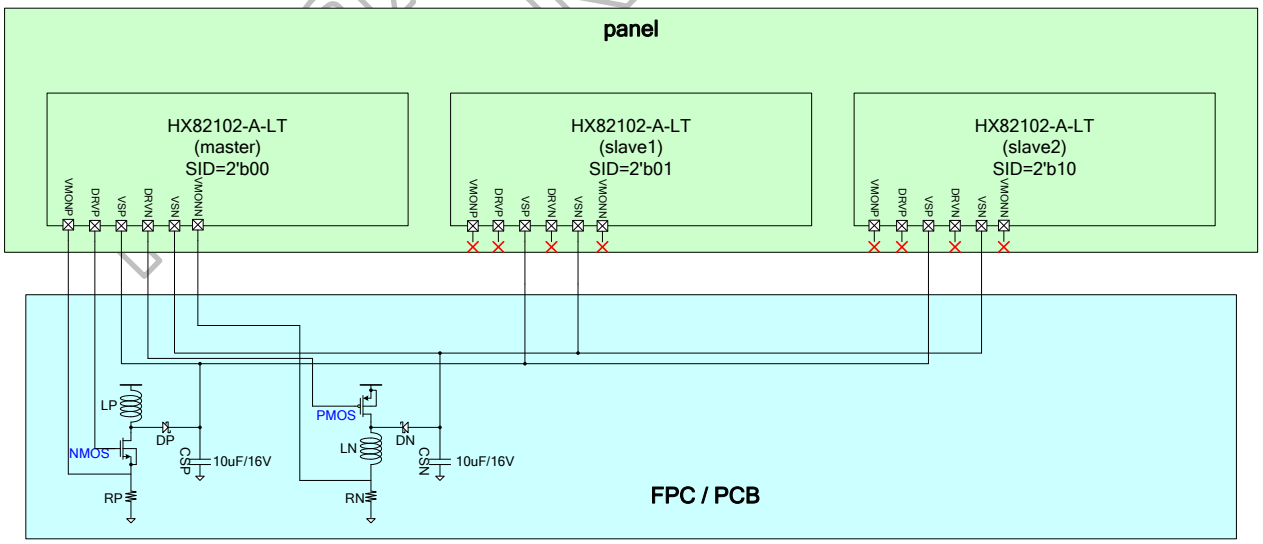

Figure 5.30: Cascade design for PFM

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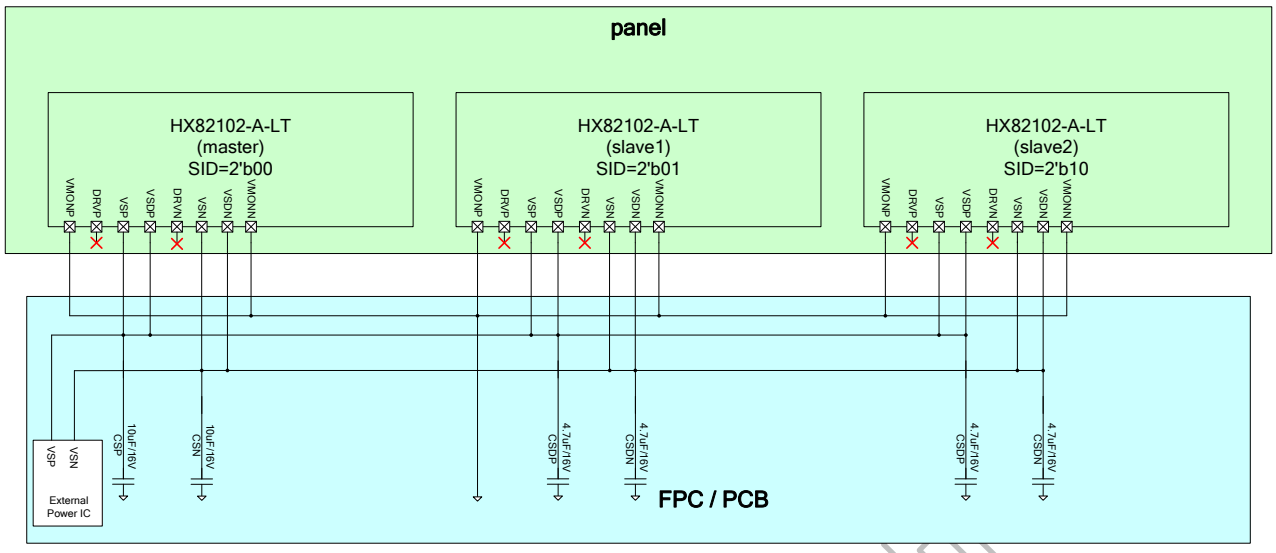

Figure 5.31: Cascade design with external power IC (When EXT_PWR1=H)

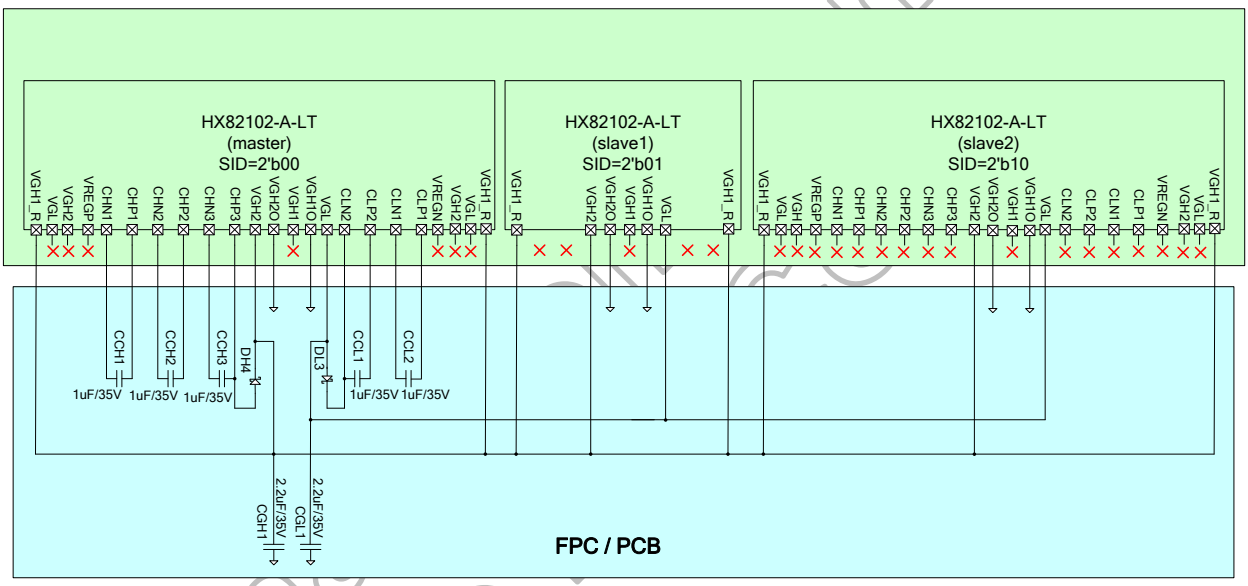

Figure 5.32: Cascade design for charge pumps at Gate driver mode

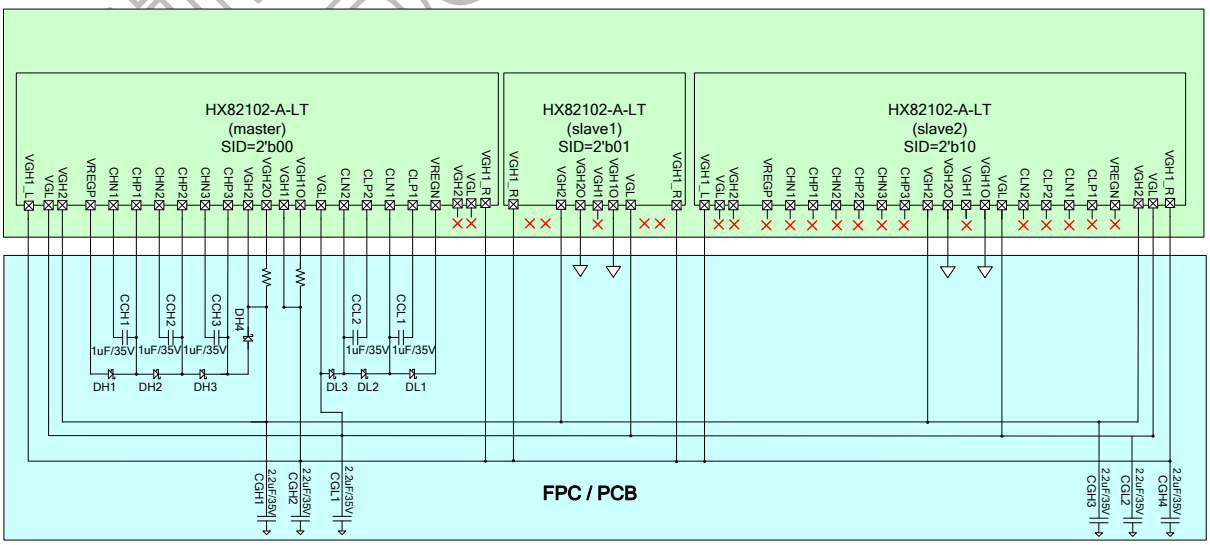

Figure 5.33: Cascade design for charge pumps at IGZO mode

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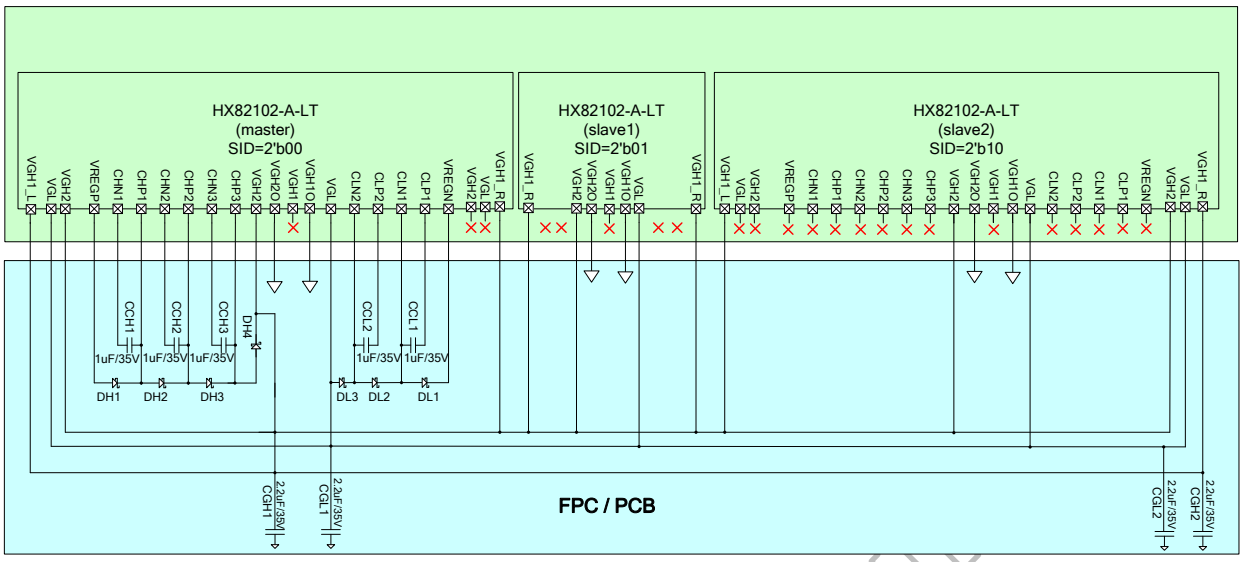

Figure 5.34: Cascade design for charge pumps at GIP mode

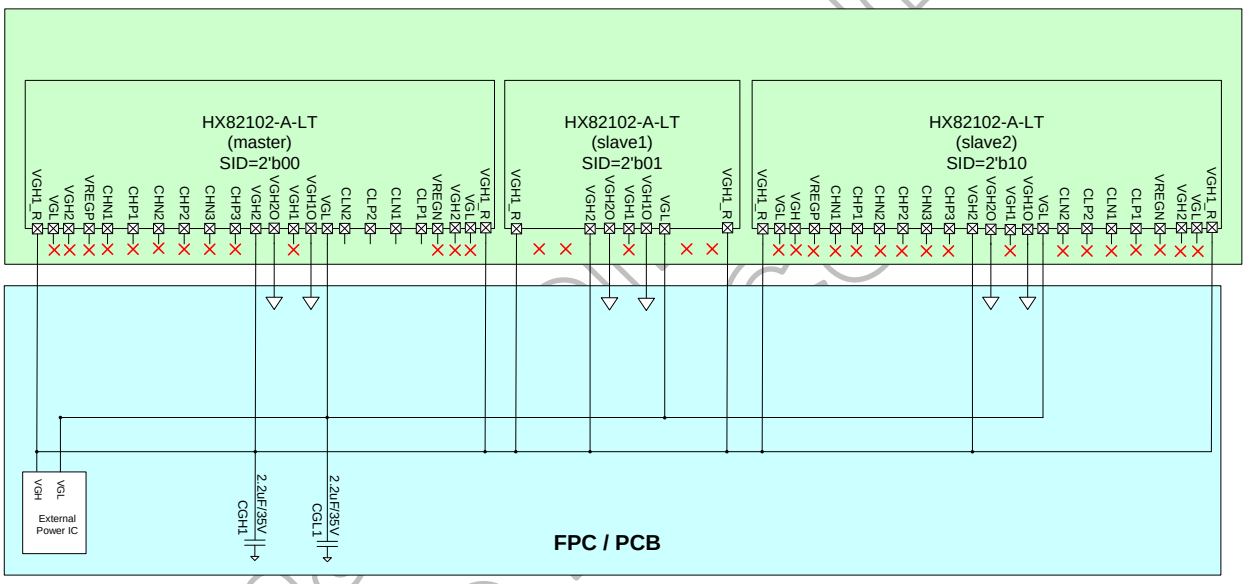

Figure 5.35: Cascade design for charge pumps at Gate driver mode (When EXT_PWR2=H)

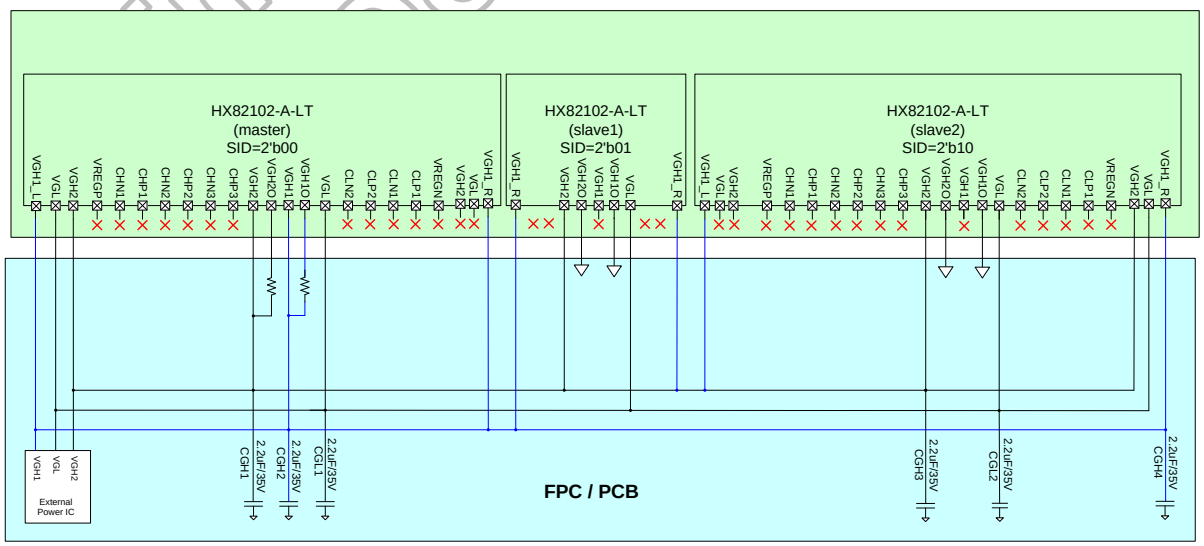

Figure 5.36: Cascade design for charge pumps at IGZO driver mode (When EXT_PWR2=H)

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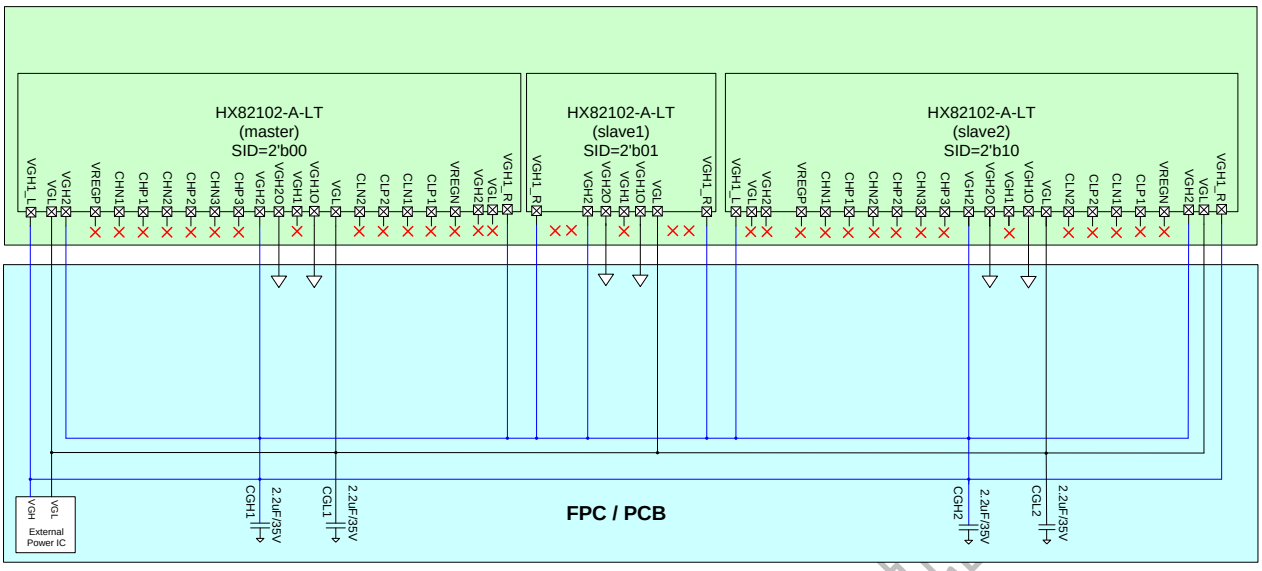

Figure 5.37: Cascade design for charge pumps at GIP driver mode(When EXT_PWR2=H)

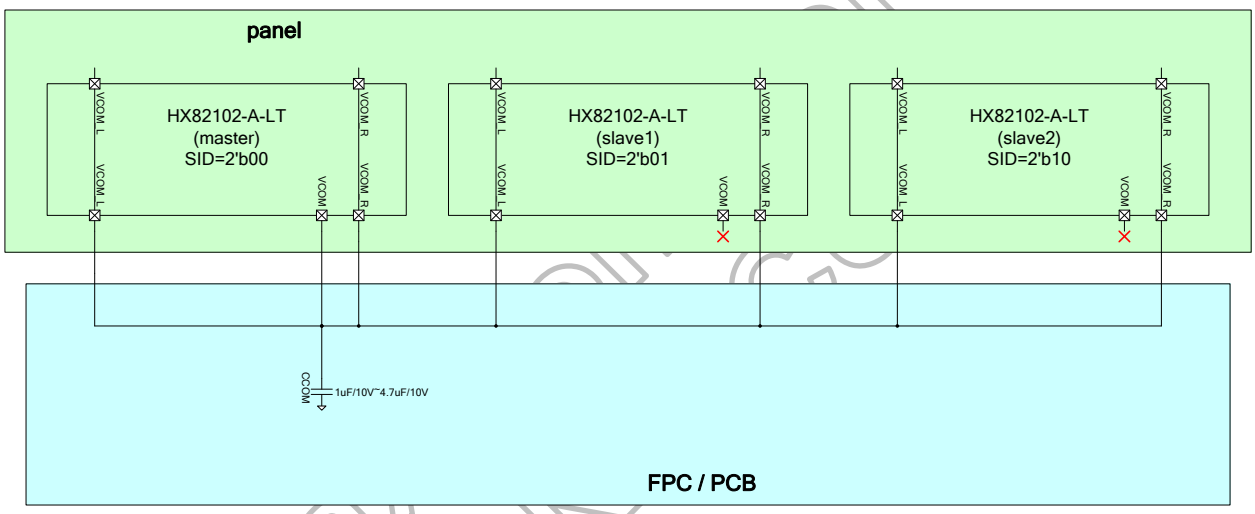

Figure 5.38: Cascade design for VCOM

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5.4.7. Cascade design: RESETB application

A. Add external RC circuit to pin RESETB to start whole chip reset when power up.
B. If RESETB_SLP function not used, and pin RESETB_SLP should be connected to VCC1.

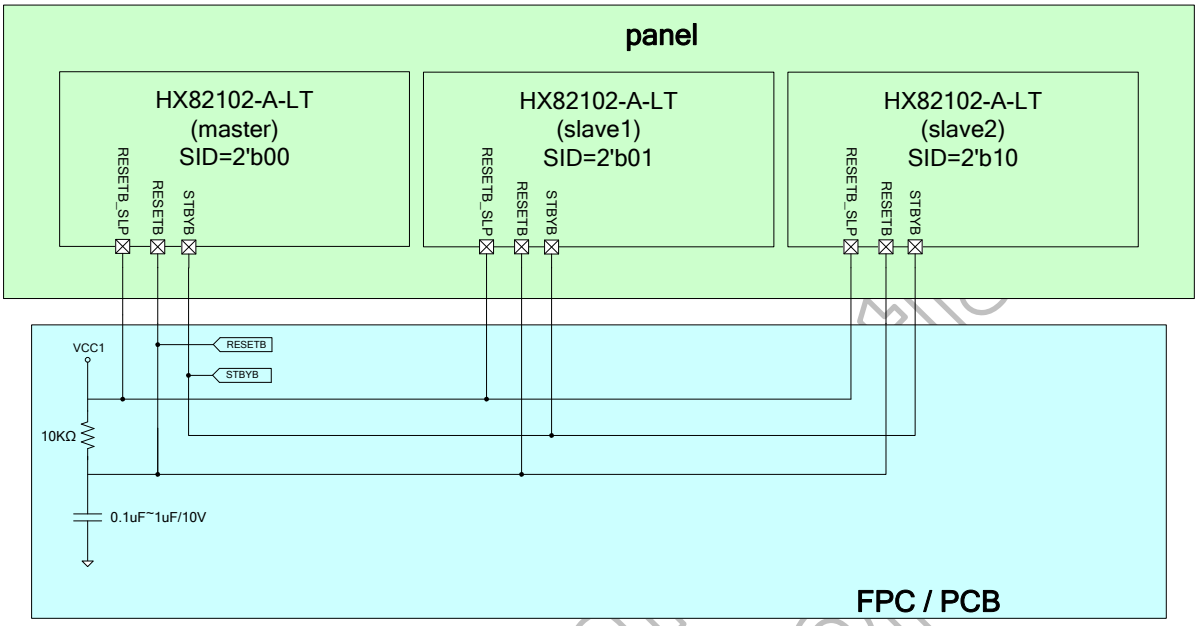

Figure 5.39: Cascade design for RESETB function

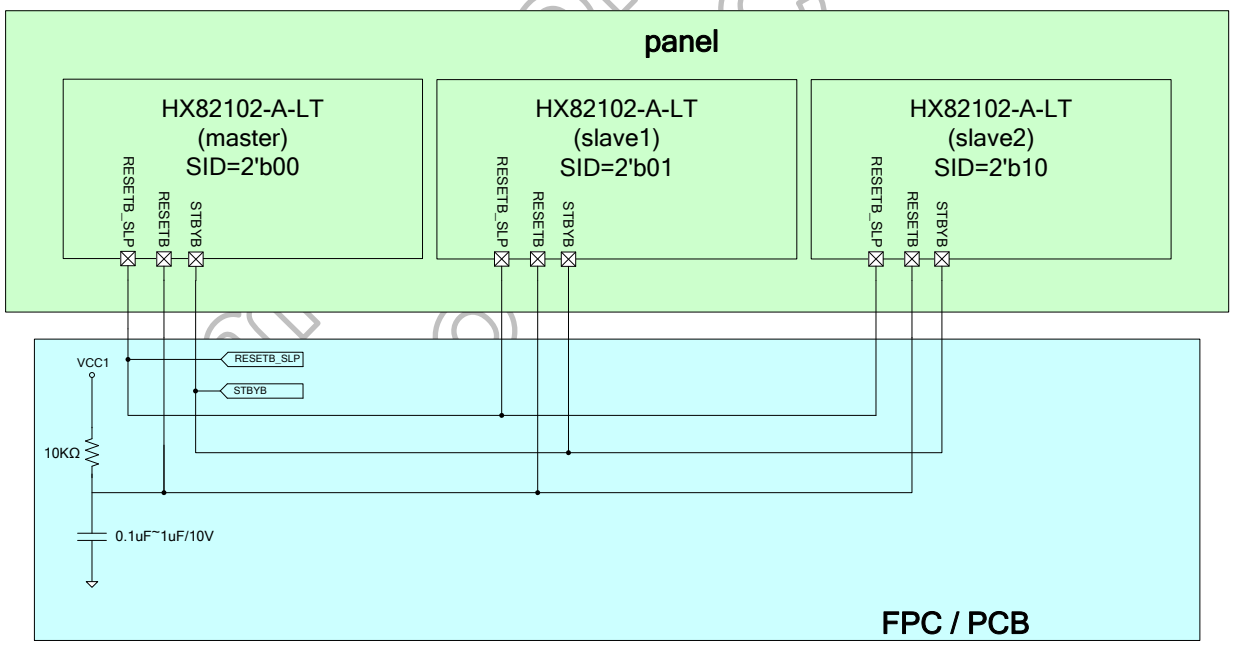

Figure 5.40: Cascade design for RESETB_SLP function

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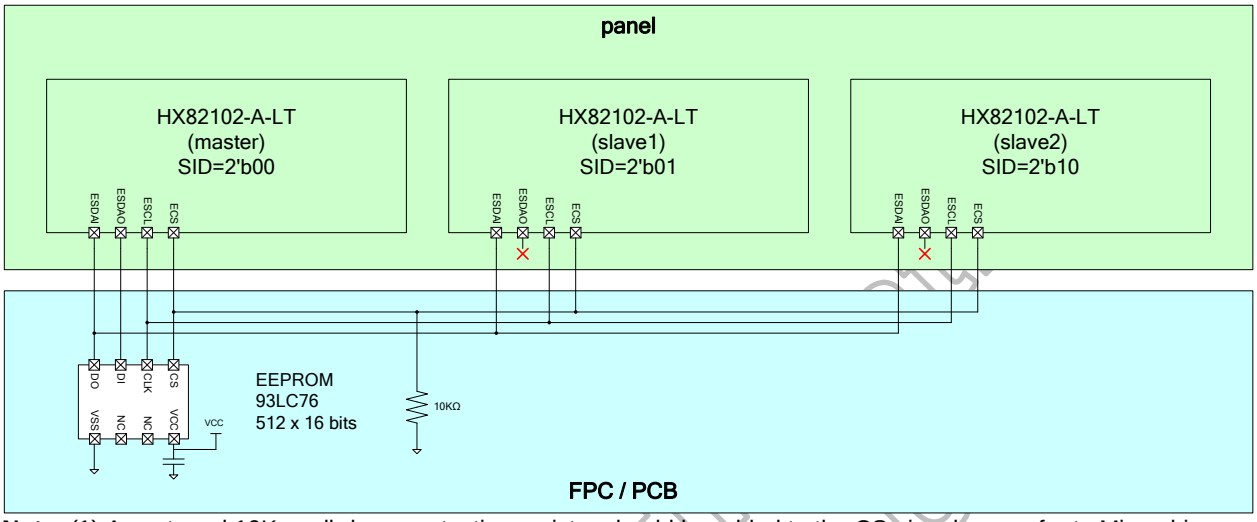
5.4.8. Cascade design: EEPROM application

A. Master and all slave IC set EEPEN=H to enable EEPROM reload setting.
B. HX82102-A-LT supports 8K-bit EEPROM. HX82102-A-LT recommends using Microchip 93LC76 512 x 16-bit.
C. Connect EEPROM CS, CLK, DI, DO to HX82102-A-LT ECS, ESCL, ESDAO, ESDAI



Note: (1) An external 10K_ pull-down protection resistor should be added to the CS pin, please refer to Microchip 93LC76 datasheet for the details.

Figure 5.41: Cascade design for EEPROM application

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5.4.9. Cascade design: External temperature sensor application

A. Master and all slave IC TS_H should be connected together.
B. Master and all slave IC TS_L should be connected together.

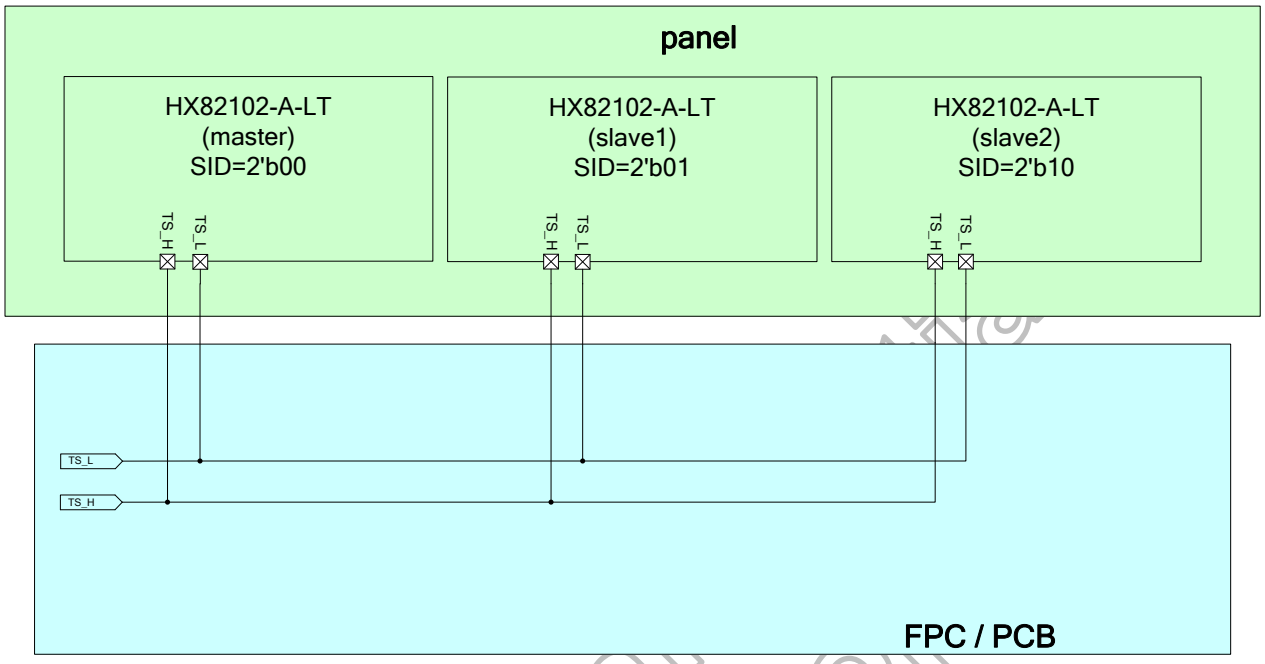

Figure 5.42: Cascade design for external temperature sensor application

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6. Function Description

6.1. Data processing circuit

The input data from external display interface will be fed to the data processing circuit, which contains the functions of contrast **(Gain)** control; brightness **(Offset)** control, and gamma control. See the register descriptions for detail.

The contrast adjustment is done on RGB data with 3 sets of 8-bit registers. The 8-bit register represents gain value in the range of 0.5 ~ 1.496. When output data of the gain multiplication exceeds 255, it will be clamped at 255. Default gain value is 1.0.

The brightness adjustment is done on RGB data with 3 sets of 6-bit registers. The 6-bit register represents offset value in the range of -16 ~ +47.

The digital gamma correction is done by 23-segment piecewise linear interpolation. The 23 segments are defined with 24 register values for level 0, 1, 3, 7, 11, 15, 23, 31, 47, 63, 95, 127, 128, 160, 192, 208, 224, 232, 240, 244, 248, 252, 254 and 255. The gamma correction output is then fed to 8-bit DAC and OP to drive the source lines on the panel.

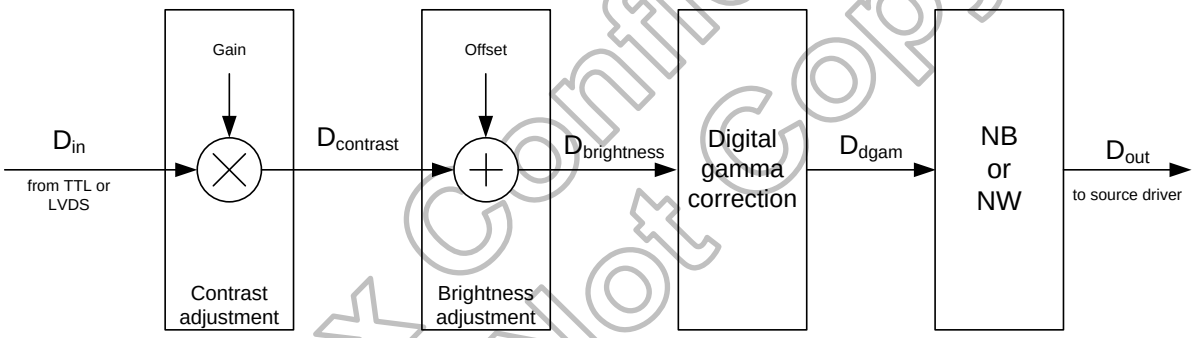

Figure 6.1: Data processing

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6.1.1. Contrast adjustment

Contrast adjustment is done on RGB data separately by multiplying a gain ranging from 0.5 to 1.496. The gain for each color is set with 3 sets of 8-bit registers **(RGC[7:0], GGC[7:0], BGC[7:0])**. If the resulting output data exceeds 255, it will be clamped to 255. Default gain value is 1.0.

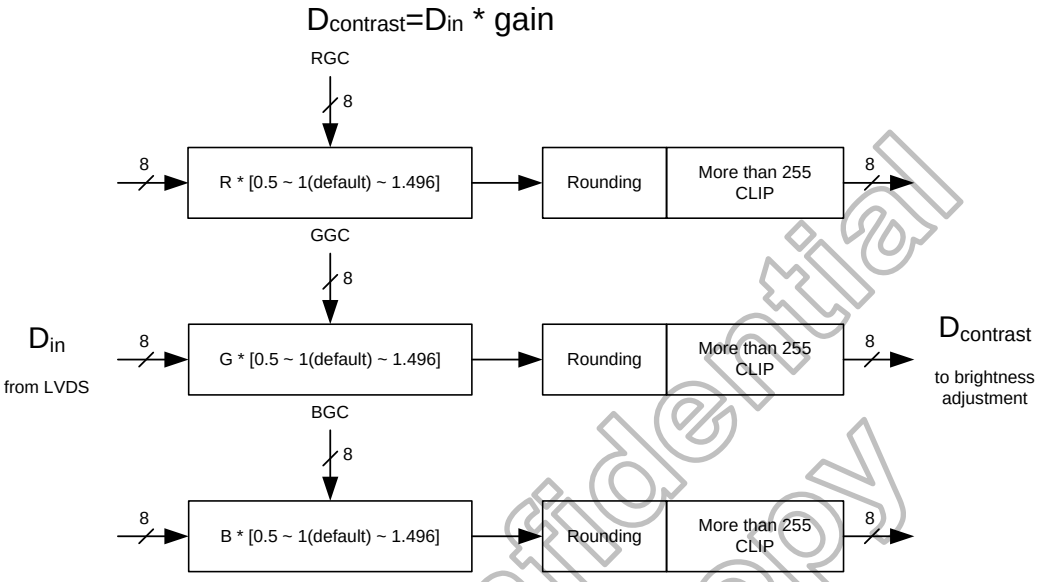

Figure 6.2: Contrast adjustment

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6.1.2. Brightness adjustment

Brightness adjustment is done on RGB data separately by adding an offset ranging from -16 to +47. The offset of each color is set with 3 sets of 6-bit registers **(ROB[5:0], GOB[5:0], BOB[5:0])**. If the resulting output data exceeds the range of 0 to 255, it will be clamped to 0 and 255. Default offset is 0.

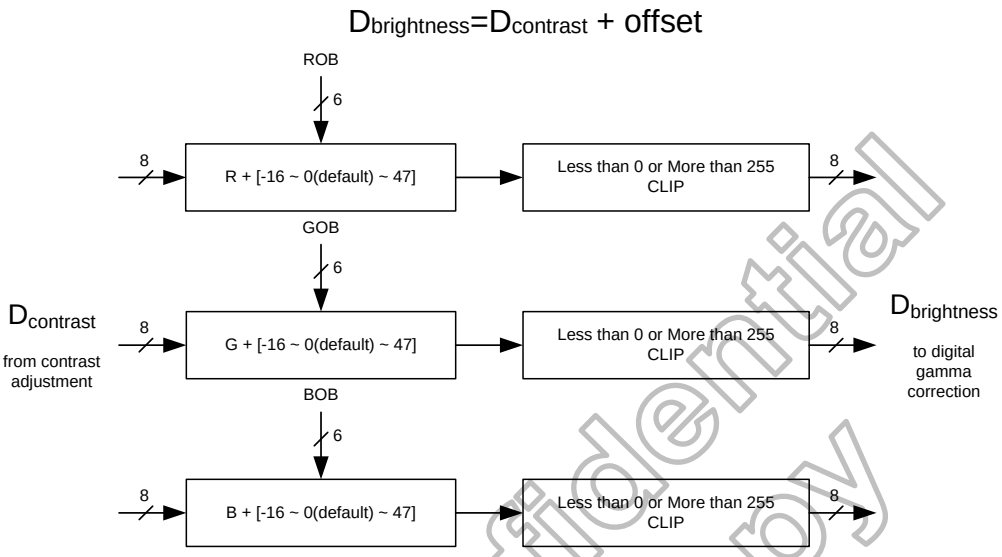

Figure 6.3: Brightness adjustment

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6.1.3. Digital gamma correction

The digital gamma correction is done on RGB data separately with 23-segment piecewise linear interpolation. The 23 segments are defined with 24 register values Y_1~Y_{24} **(in register Page09h ~ Page0Bh)** for level X_1~X_{24} = 0, 1, 3, 7, 11, 15, 23, 31, 47, 63, 95, 127, 128, 160, 192, 208, 224, 232, 240, 244, 248, 252, 254 and 255. Y on X between X_n and X_{n+1} is interpolated with the following equations.

$$Y = Y_n + (Y_{n+1} - Y_n) * (X-X_n) / (X_{n+1}-X_n)$$

The gamma correction output 10-bit data D_{dgam} is then fed to 8-bit DAC and OP to drive the source lines on the panel with dithering.

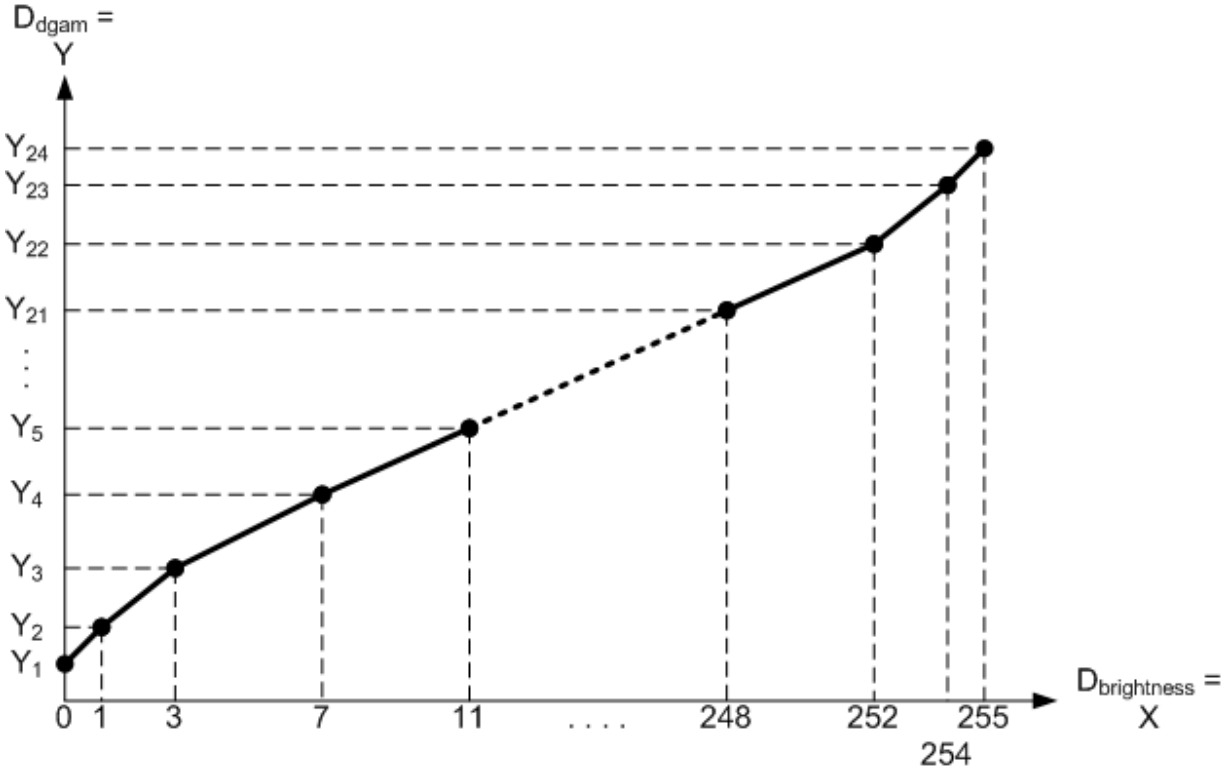

Figure 6.4: Digital gamma correction

6.2. NB/NW selection

The data after digital gamma processing D_{dgam} will go to NB/NW block. It will transfer input data to corresponding correct NB or NW data.

6.3. LCD driver

The LCD driver circuit consists of a 1920-channel source driver **(S[1920:1])** and outputs a liquid crystal drive voltage **(Grayscale voltage)**, which corresponds to the display data. The source lines of the display could be cascaded to support maximum resolution 2880xRGBx1080 with 4 chips.

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6.4. Timing controller

The control circuit generates internal control signals from input VS, HS, or DE signals. The LCD timing generator generates internal control signals for the source and gate driver. The timing generator also generates signals to control the operation timings of display data latching circuit.

6.5. Display interface

The HX82102-A-LT supports different display resolutions with single port LVDS, dual port LVDS.

6.5.1. 8-bit LVDS interface

For 1-port LVDS 8-bit mode with VESA format, only the odd port **(with OLVxxx pins)** is used.

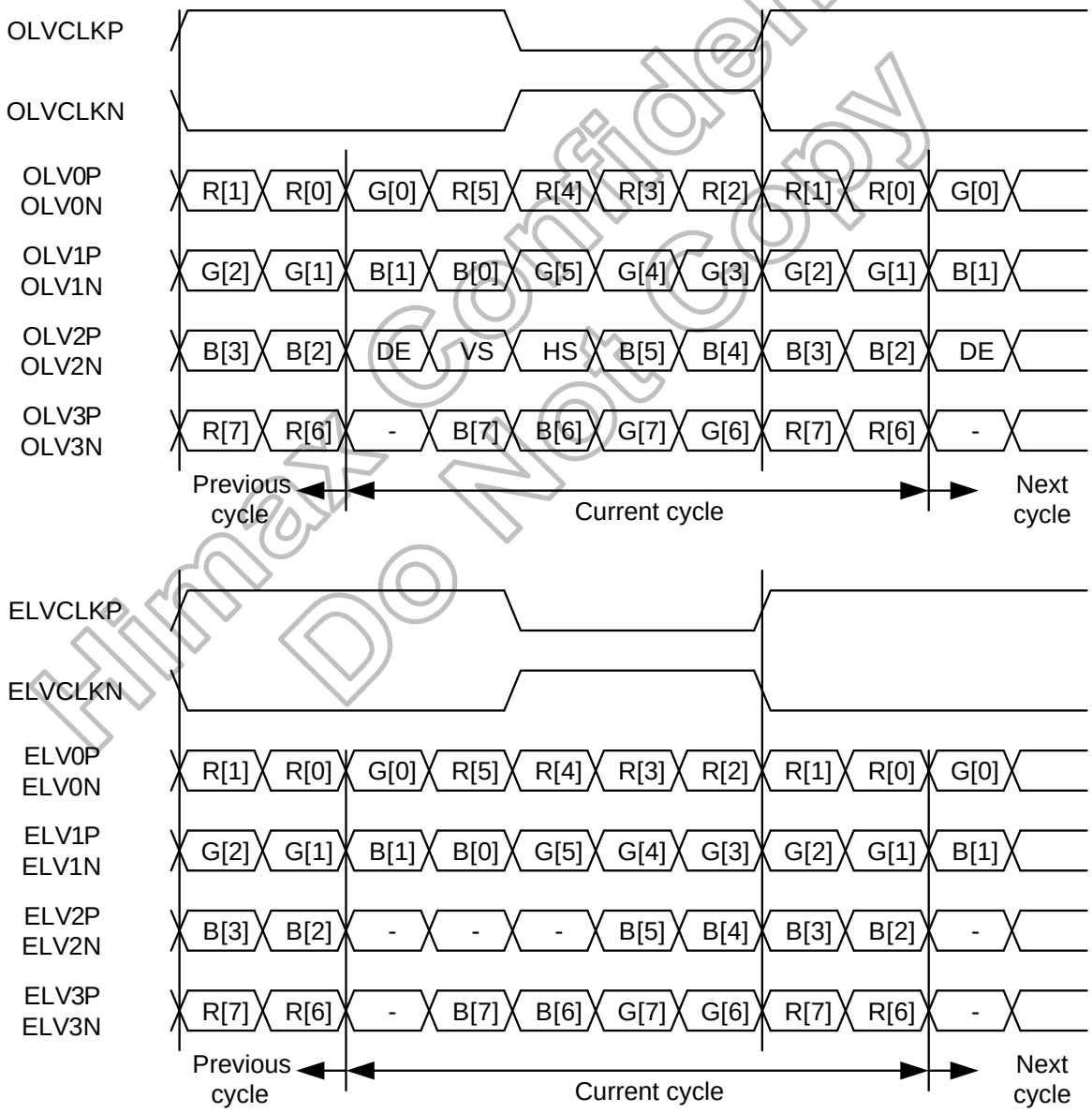

Figure 6.5: 2-port LVDS signals, VESA format (8-bit)

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For 1-port LVDS 8-bit mode with JEIDA format, only the odd port **(with OLVxxx pins)** is used.

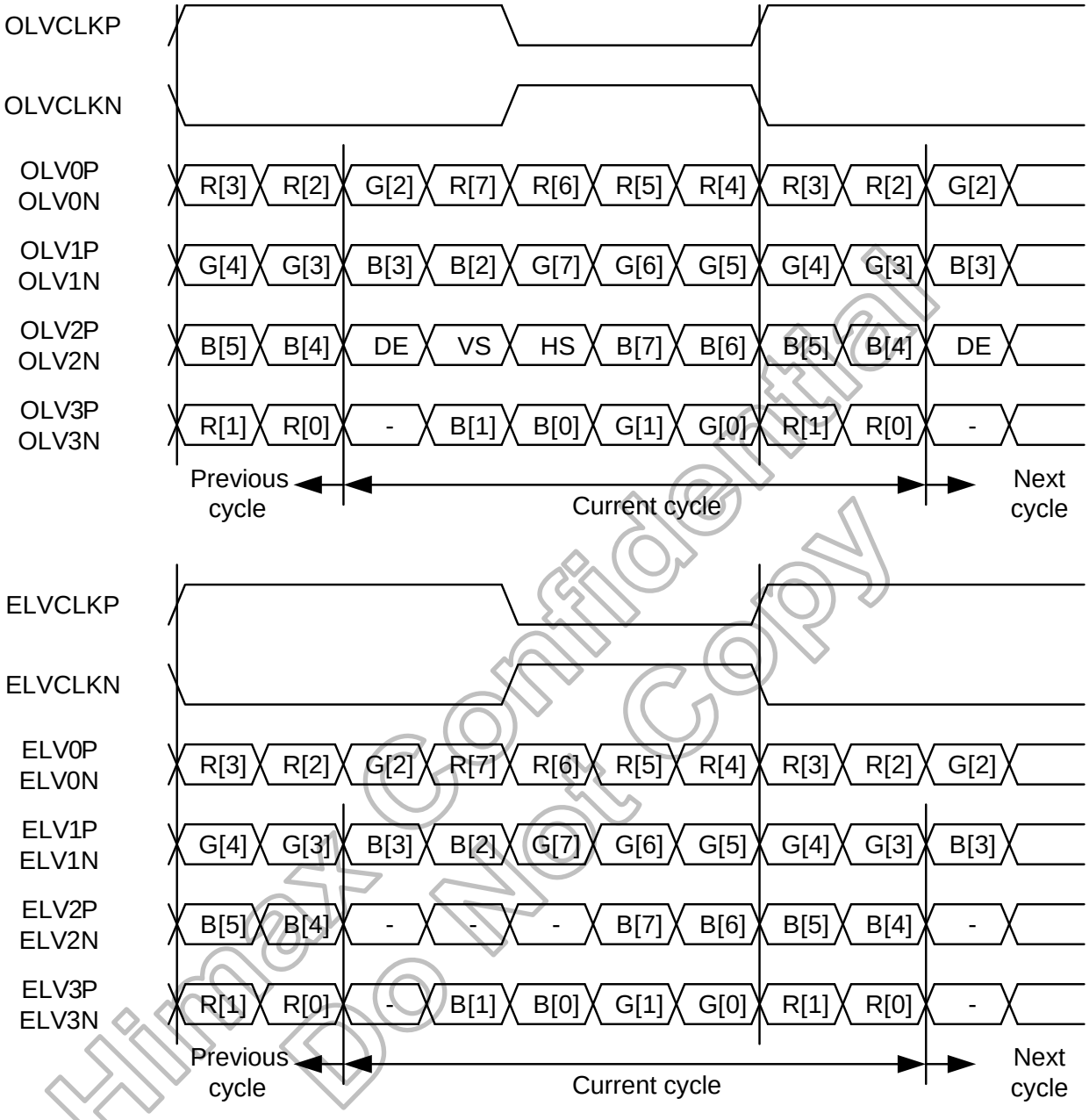

Figure 6.6: 2-port LVDS signals, JEIDA format (8-bit)

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6.5.2. 6-bit LVDS interface

For 1-port LVDS 6-bit mode with VESA format, only the odd port **(with OLVxxx pins)** is used.

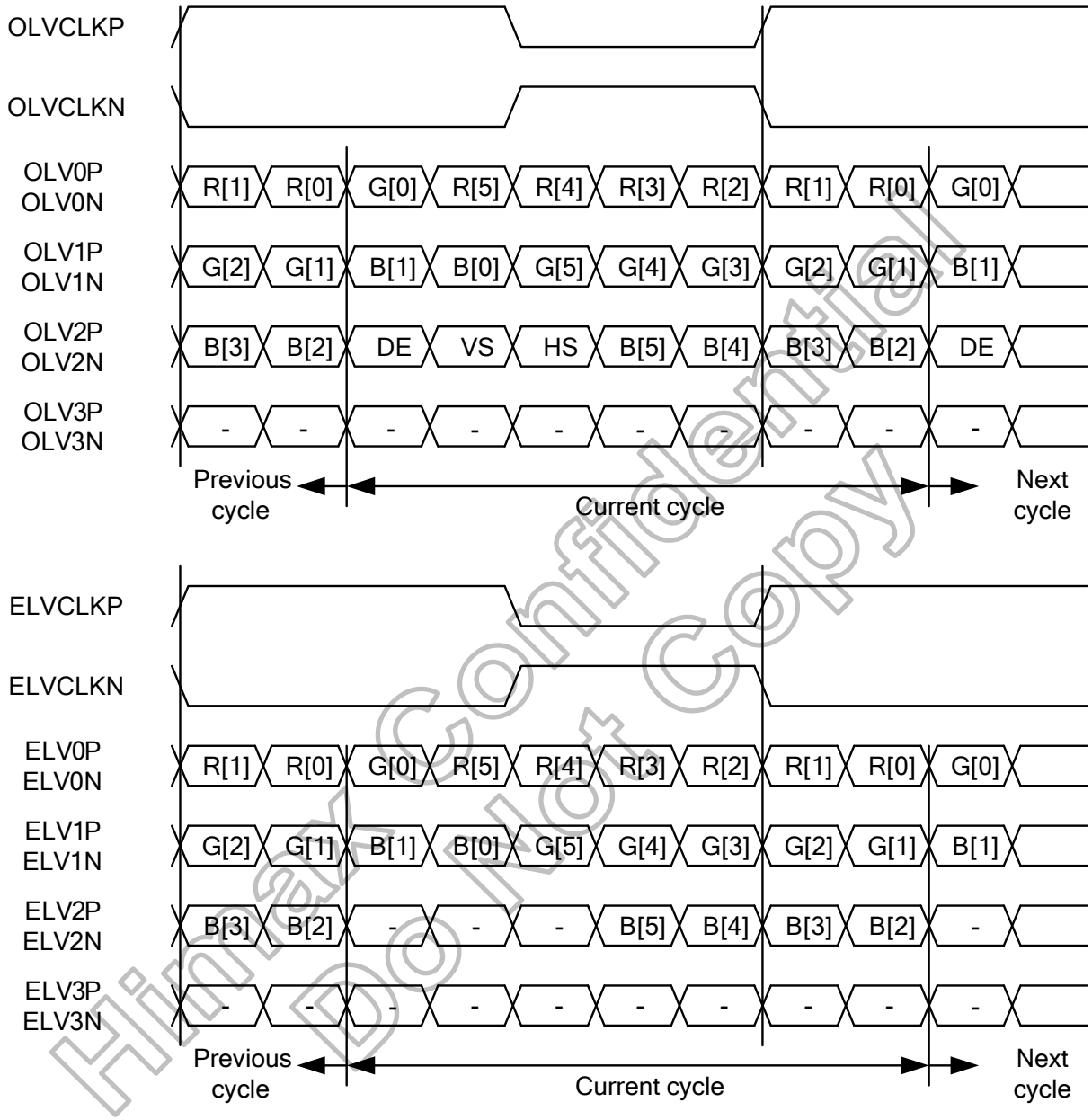

Figure 6.7: 2-port LVDS signals, VESA format (6-bit)

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6.5.3. Parallel RGB with Sync mode at LVDS interface

- **Horizontal**

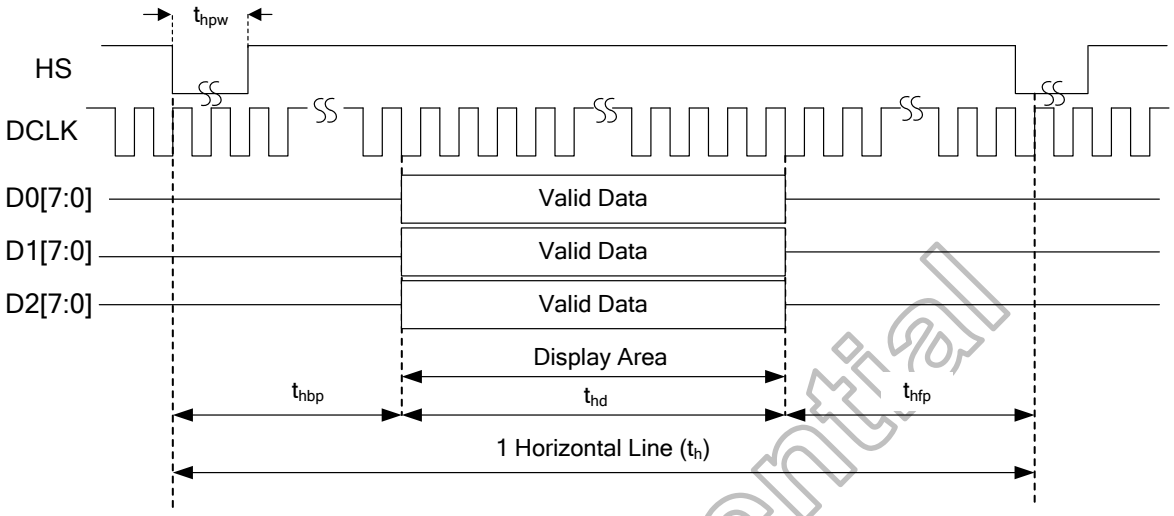

Figure 6.8: Horizontal input timing at Sync mode

- **Vertical**

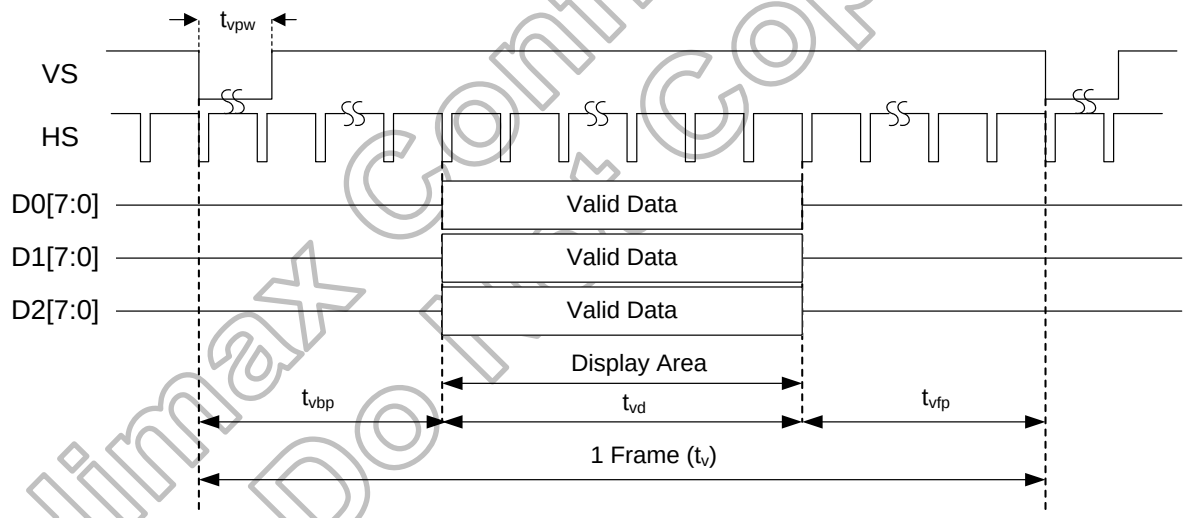

Figure 6.9: Vertical input timing at Sync mode

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Parameter	Symbol	Panel Resolution									Unit
		2560xRGBx960 (Two Port)			1920xRGBx1080 (Two Port)			1920xRGBx720 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	78.82	-	-	67.47	-	-	87.7	-	MHz
Horizontal valid data	t_{hd}		1280			960			1920		DCLK
Hsync pulse Width	t_{hpw}	10	12	-	10	12	-	10	12	-	DCLK
Hsync back porch	t_{hbp}(1)	5	16	-	5	16	-	5	16	-	DCLK
Hsync front porch	t_{hfp}	50	50	-	50	50	-	50	50	-	DCLK
1 horizontal line	t_h(2)	1335	1346	1664	1015	1026	1248	1975	1986	2496	DCLK
Vertical valid data	t_{vd}		960			1080			720		H
Vsync pulse width	t_{vpw}	1	3	-	1	3	-	1	3	-	H
Vsync back porch	t_{vbp}(3)	4	8	-	4	8	-	4	8	-	H
Vsync front porch	t_{vfp}	6	8	-	6	8	-	6	8	-	H
1 vertical field	t_v	970	976	1010	1090	1096	1134	730	736	756	H
Frame rate	FR(4)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1660xRGBx1660 (Two Port)			1560xRGBx720 (One Port)			1540xRGBx720 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	90.1	-	-	71.8	-	-	70.92	-	MHz
Horizontal valid data	t_{hd}		830			1560			1540		DCLK
Hsync pulse Width	t_{hpw}	10	12	-	10	12	-	10	12	-	DCLK
Hsync back porch	t_{hbp}(1)	5	16	-	5	16	-	5	16	-	DCLK
Hsync front porch	t_{hfp}	50	50	-	50	50	-	50	50	-	DCLK
1 horizontal line	t_h(2)	885	896	1079	1615	1626	2028	1595	1606	2002	DCLK
Vertical valid data	t_{vd}		1660			720			720		H
Vsync pulse width	t_{vpw}	1	3	-	1	3	-	1	3	-	H
Vsync back porch	t_{vbp}(3)	4	8	-	4	8	-	4	8	-	H
Vsync front porch	t_{vfp}	6	8	-	6	8	-	6	8	-	H
1 vertical field	t_v	1670	1676	1696	730	736	756	730	736	756	H
Frame rate	FR(4)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1440xRGBx540 (One Port)			1280xRGBx720 (One Port)			1280xRGBx480 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	50.24	-	-	59.44	-	-	40.06	-	MHz
Horizontal valid data	t_{hd}		1440			1280			1280		DCLK
Hsync pulse Width	t_{hpw}	10	12	-	10	12	-	10	12	-	DCLK
Hsync back porch	t_{hbp}(1)	5	16	-	5	16	-	5	16	-	DCLK
Hsync front porch	t_{hfp}	50	50	-	50	50	-	50	50	-	DCLK
1 horizontal line	t_h(2)	1495	1506	1872	1335	1346	1664	1335	1346	1664	DCLK
Vertical valid data	t_{vd}		540			720			480		H
Vsync pulse width	t_{vpw}	1	3	-	1	3	-	1	3	-	H
Vsync back porch	t_{vbp}(3)	4	8	-	4	8	-	4	8	-	H
Vsync front porch	t_{vfp}	6	8	-	6	8	-	6	8	-	H
1 vertical field	t_v	550	556	567	730	736	756	490	496	504	H
Frame rate	FR(4)	-	60	-	-	60	-	-	60	-	Hz

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Parameter	Symbol	Panel Resolution									Unit
		1024xRGBx600 (One Port)			960xRGBx960 (One Port)			800xRGBx480 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	40.29	-	-	60.08	-	-	25.77	-	MHz
Horizontal valid data	t_{hd}		1024			960			800		DCLK
Hsync pulse Width	t_{hpw}	10	12	-	10	12	-	10	12	-	DCLK
Hsync back porch	t_{hbp}(1)	5	16	-	5	16	-	5	16	-	DCLK
Hsync front porch	t_{hfp}	50	50	-	50	50	-	50	50	-	DCLK
1 horizontal line	t_h(2)	1079	1090	1331	1015	1026	1248	855	866	1040	DCLK
Vertical valid data	t_{vd}		600			960			480		H
Vsync pulse width	t_{vpw}	1	3	-	1	3	-	1	3	-	H
Vsync back porch	t_{vbp}(3)	4	8	-	4	8	-	4	8	-	H
Vsync front porch	t_{vfp}	6	8	-	6	8	-	6	8	-	H
1 vertical field	t_v	610	616	720	970	976	1008	490	496	576	H
Frame rate	FR(4)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		720xRGBx720 (One Port)			640xRGBx640 (One Port)			540xRGBx540 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	34.71	-	-	27.79	-	-	20.22	-	MHz
Horizontal valid data	t_{hd}		720			640			540		DCLK
Hsync pulse Width	t_{hpw}	10	12	-	10	12	-	10	12	-	DCLK
Hsync back porch	t_{hbp}(1)	5	16	-	5	16	-	5	16	-	DCLK
Hsync front porch	t_{hfp}	50	50	-	50	50	-	50	50	-	DCLK
1 horizontal line	t_h(2)	775	786	936	695	706	832	595	606	702	DCLK
Vertical valid data	t_{vd}		720			640			540		H
Vsync pulse width	t_{vpw}	1	3	-	1	3	-	1	3	-	H
Vsync back porch	t_{vbp}(3)	4	8	-	4	8	-	4	8	-	H
Vsync front porch	t_{vfp}	6	8	-	6	8	-	6	8	-	H
1 vertical field	t_v	730	736	864	650	656	768	550	556	648	H
Frame rate	FR(4)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution			Unit
		480xRGBx480 (One Port)			
		Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	16.25	-	MHz
Horizontal valid data	t_{hd}		480		DCLK
Hsync pulse Width	t_{hpw}	10	12	-	DCLK
Hsync back porch	t_{hbp}(1)	5	16	-	DCLK
Hsync front porch	t_{hfp}	50	50	-	DCLK
1 horizontal line	t_h(2)	535	546	624	DCLK
Vertical valid data	t_{vd}		480		H
Vsync pulse width	t_{vpw}	1	3	-	H
Vsync back porch	t_{vbp}(3)	4	8	-	H
Vsync front porch	t_{vfp}	6	8	-	H
1 vertical field	t_v	490	496	576	H
Frame rate	FR(4)	-	60	-	Hz

Note: (1) Horizontal back-porch could be adjusted at Sync mode by register R07h of Page00h.
(2) $t_h=t_{hbp} + t_{hfp} + t_{hd}$ and $t_v=t_{vbp} + t_{vfp} + t_{vd}$.
(3) Vertical back-porch could be adjusted at Sync mode by register R06h of Page00h.
(4) FR **(Frame rate)**=F_{DCLK} / t_h / t_v.

Table 6.1: Input timing table at Sync mode

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6.5.4. Parallel RGB with DE only mode at LVDS interface

It just needs DE signal only, when DE only mode enables.

- **Horizontal**

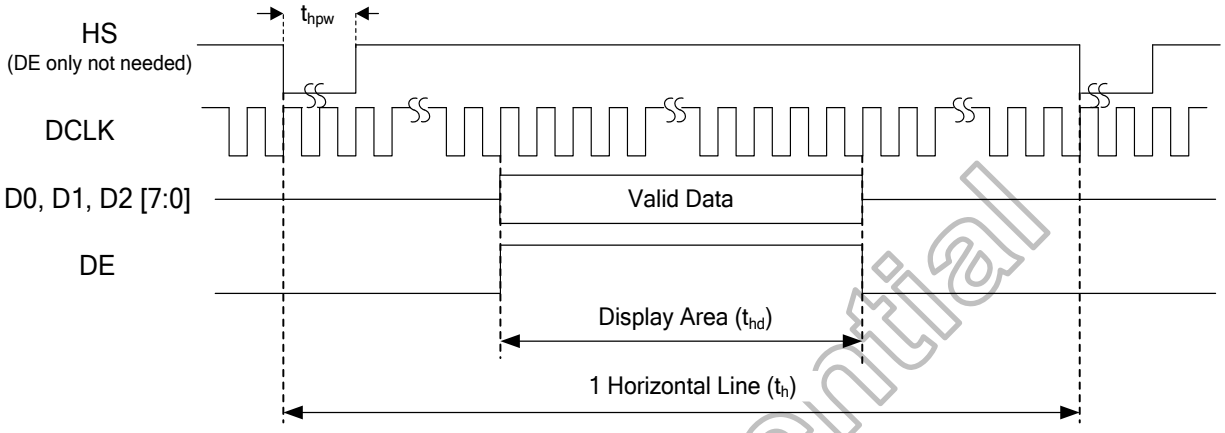


Figure 6.10: Horizontal input timing at DE only mode

- **Vertical**

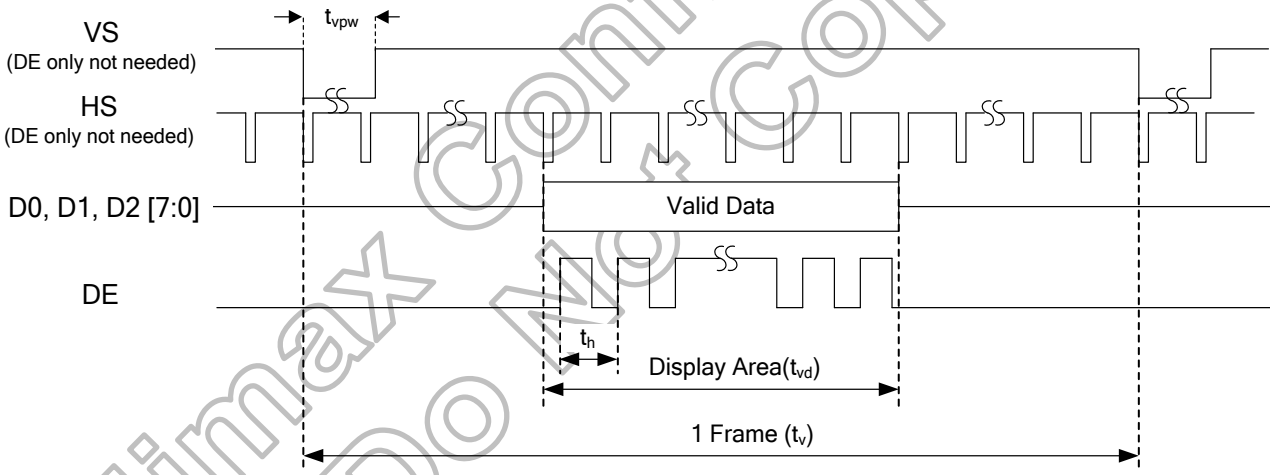
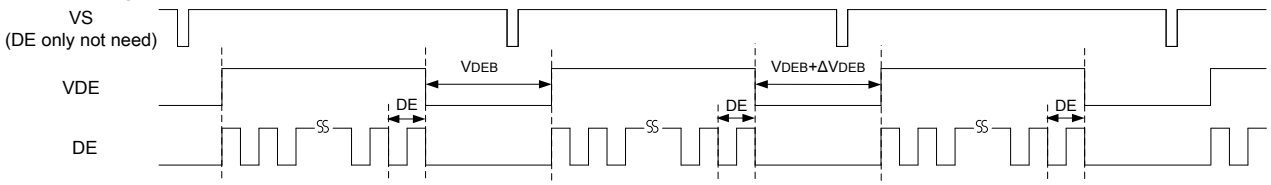


Figure 6.11: Vertical input timing at DE only mode



Note: (1) The variation of vertical blank **(ΔVDEB)** must be less than 50 DCLK with DE only mode when GIP mode **(GDSEL=L)** is used.

Figure 6.12: Vertical variation timing at DE only mode

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Parameter	Symbol	Panel Resolution									Unit
		2560xRGBx960 (Two Port)			1920xRGBx1080 (Two Port)			1920xRGBx720 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	78.82	-	-	67.47	-	-	87.7	-	MHz
Horizontal valid data	t_{hd}		1280			960			1920		DCLK
1 horizontal line	t_h	1335	1346	1664	1015	1026	1248	1975	1986	2496	DCLK
Vertical valid data	t_{vd}		960			1080			720		H
1 vertical field	t_v(1)	970	976	1010	1090	1096	1134	730	736	756	H
Frame rate	FR(2)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1660xRGBx1660 (Two Port)			1560xRGBx720 (One Port)			1540xRGBx720 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	90.1	-	-	71.8	-	-	70.92	-	MHz
Horizontal valid data	t_{hd}		830			1560			1540		DCLK
1 horizontal line	t_h	885	896	1079	1615	1626	2028	1595	1606	2002	DCLK
Vertical valid data	t_{vd}		1660			720			720		H
1 vertical field	t_v(1)	1670	1676	1696	730	736	756	730	736	756	H
Frame rate	FR(2)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1440xRGBx540 (One Port)			1280xRGBx720 (One Port)			1280xRGBx480 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	50.24	-	-	59.44	-	-	40.06	-	MHz
Horizontal valid data	t_{hd}		1560			1440			1280		DCLK
1 horizontal line	t_h	1495	1506	1872	1335	1346	1664	1335	1346	1664	DCLK
Vertical valid data	t_{vd}		540			720			480		H
1 vertical field	t_v(1)	550	556	567	730	736	756	490	496	504	H
Frame rate	FR(2)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1024xRGBx600 (One Port)			960xRGBx960 (One Port)			800xRGBx480 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	40.29	-	-	60.08	-	-	25.77	-	MHz
Horizontal valid data	t_{hd}		1024			960			800		DCLK
1 horizontal line	t_h	1079	1090	1331	1015	1026	1248	855	866	1040	DCLK
Vertical valid data	t_{vd}		600			960			480		H
1 vertical field	t_v(1)	610	616	720	970	976	1008	490	496	576	H
Frame rate	FR(2)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		720xRGBx720 (One Port)			640xRGBx640 (One Port)			540xRGBx540 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	34.71	-	-	27.79	-	-	20.22	-	MHz
Horizontal valid data	t_{hd}		720			640			540		DCLK
1 horizontal line	t_h	775	786	936	695	706	832	595	606	702	DCLK
Vertical valid data	t_{vd}		720			640			540		H
1 vertical field	t_v(1)	730	736	864	650	656	768	550	556	648	H
Frame rate	FR(2)	-	60	-	-	60	-	-	60	-	Hz

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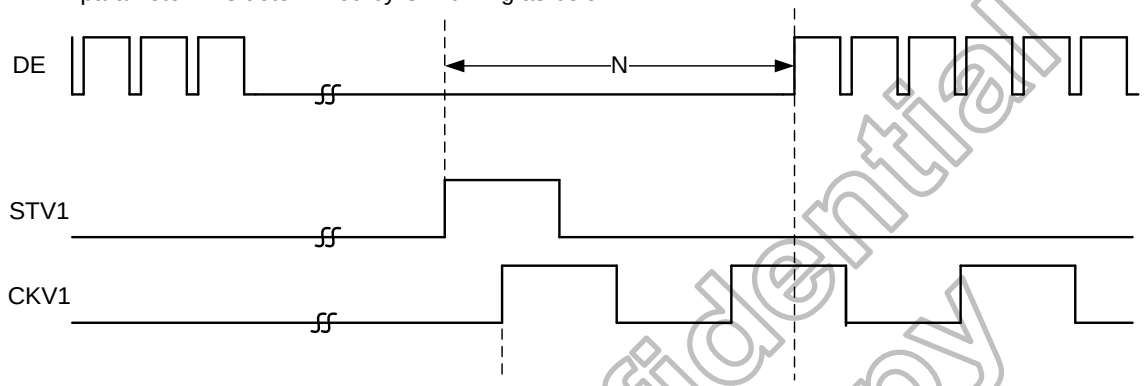
Parameter	Symbol	Panel Resolution 480xRGBx480 (One Port)			Unit
		Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	16.25	-	MHz
Horizontal valid data	t_{hd}		480		DCLK
1 horizontal line	t_h	535	546	624	DCLK
Vertical valid data	t_{vd}		480		H
1 vertical field	t_v(1)	490	496	576	H
Frame rate	FR(2)	-	60	-	Hz

Note: (1) For GIP application **(GDSEL=L)**. 1 vertical field is used that must be more than t_v minimum + (N+3). The parameter N is determined by GIP timing as below.



(2) FR **(Frame rate)**=F_{DCLK} / t_h / t_v.

Table 6.2: Input timing table at DE only mode

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6.6. Power on/off sequence

6.6.1. Power on sequence

A. If VSP and VSN are generated by PFM circuits and PWR_SPEED=1:

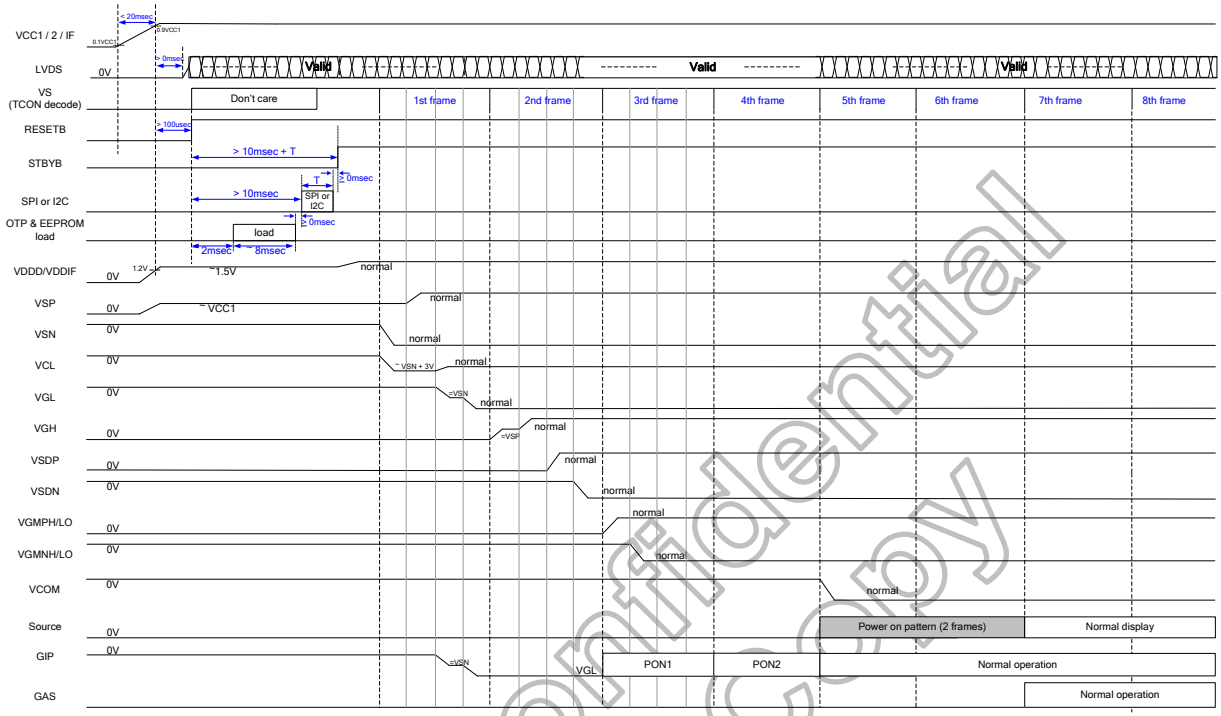

Figure 6.13: Power-on sequence with PFM (PWR_SPEED=1)

B. If VSP and VSN are generated by PFM circuits and PWR_SPEED=0:

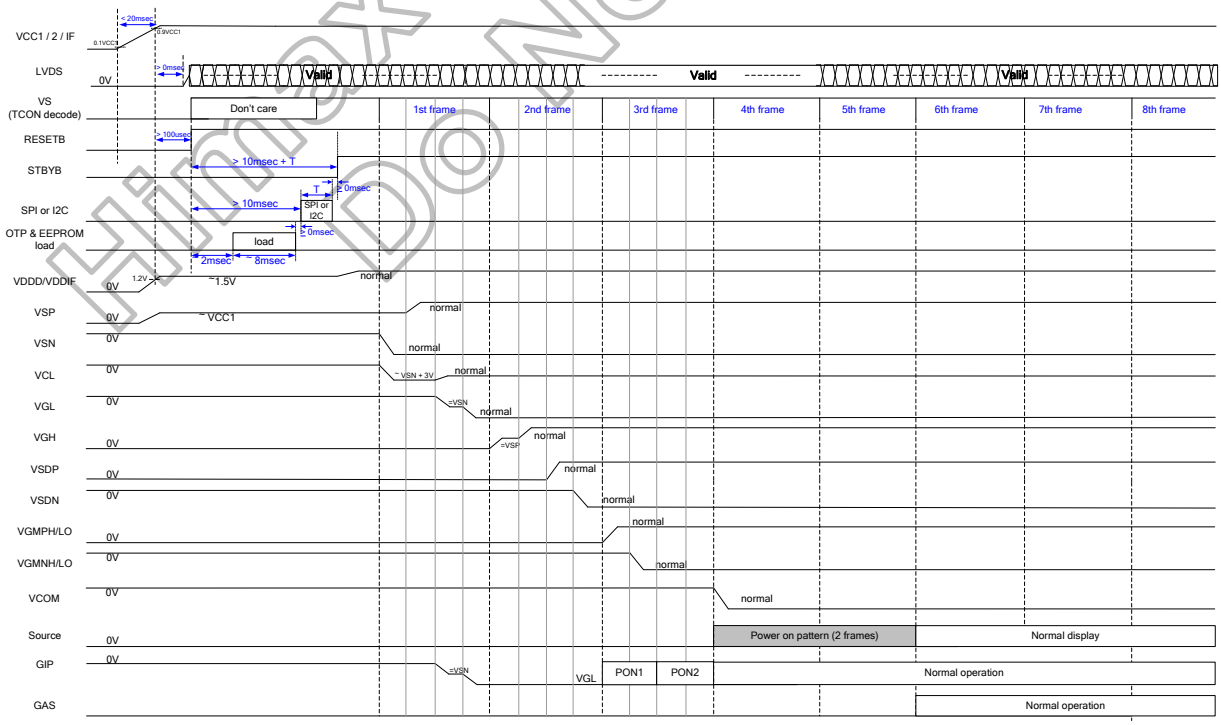

Figure 6.14: Power-on sequence with PFM (PWR_SPEED=0)

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C. VSP=VSDP and VSN=VSDN by external power supply, VGH and VGL generated by internal charge pump circuits **(PWR_SPEED=1)**

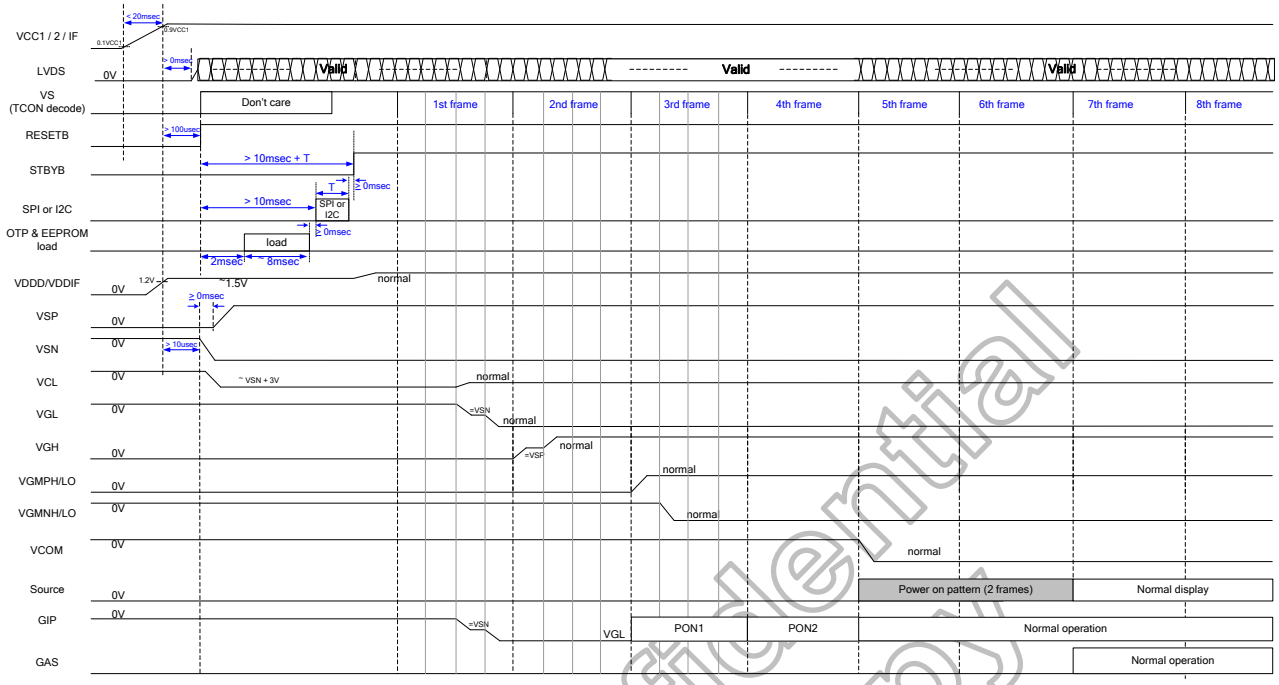

Figure 6.15: Power-on sequence with external VSP/VSN (PWR_SPEED=1)

D. VSP=VSDP and VSN=VSDN by external power supply, VGH and VGL generated by internal charge pump circuits **(PWR_SPEED=0)**

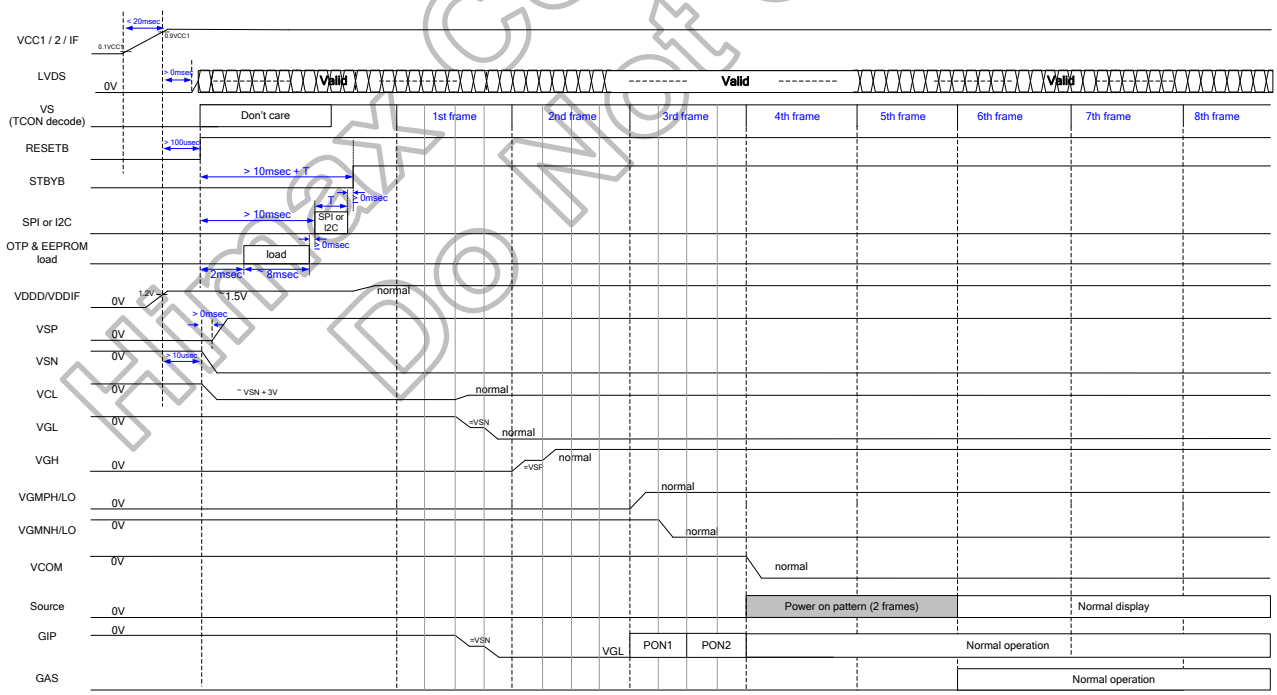

Figure 6.16: Power-on sequence with external VSP/VSN (PWR_SPEED=0)

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E. VSP=VSDP and VSN=VSDN by external power supply, and VGH and VGL by external power supply **(PWR_SPEED=1)**

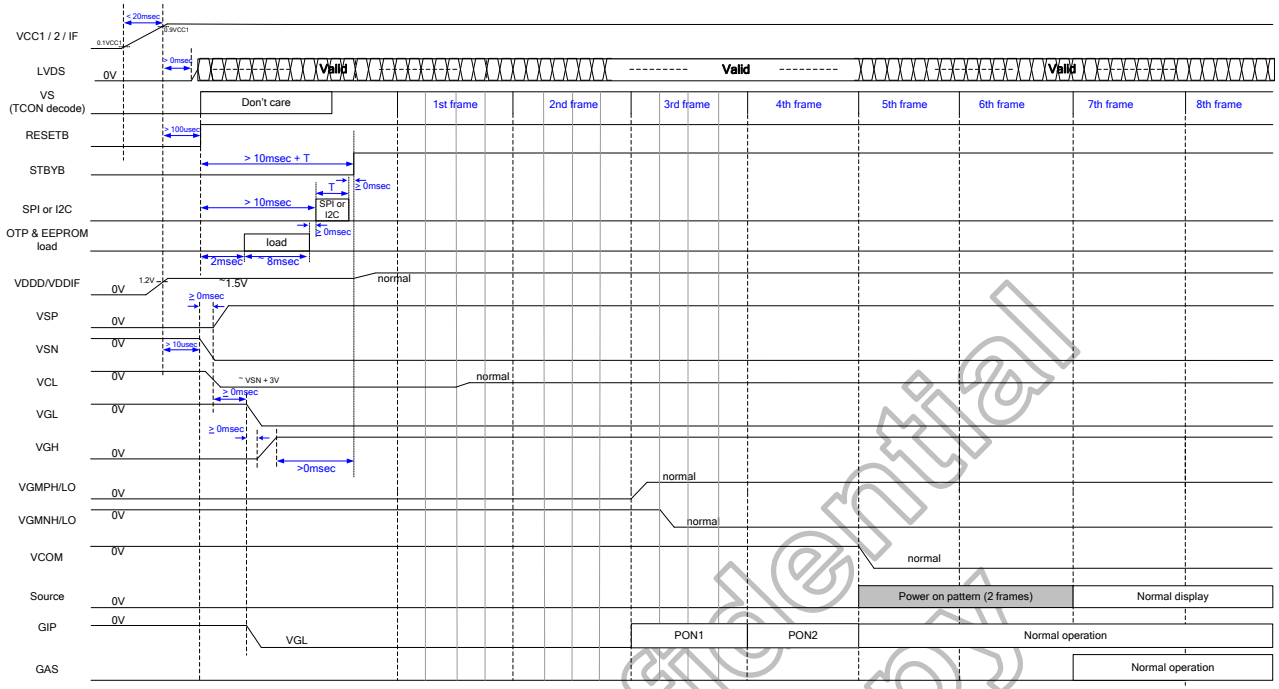

Figure 6.17: Power-on sequence with external VSP/VSN/VGH/VGL (PWR_SPEED=1)

F. VSP=VSDP and VSN=VSDN by external power supply, and VGH and VGL by external power supply **(PWR_SPEED=0)**

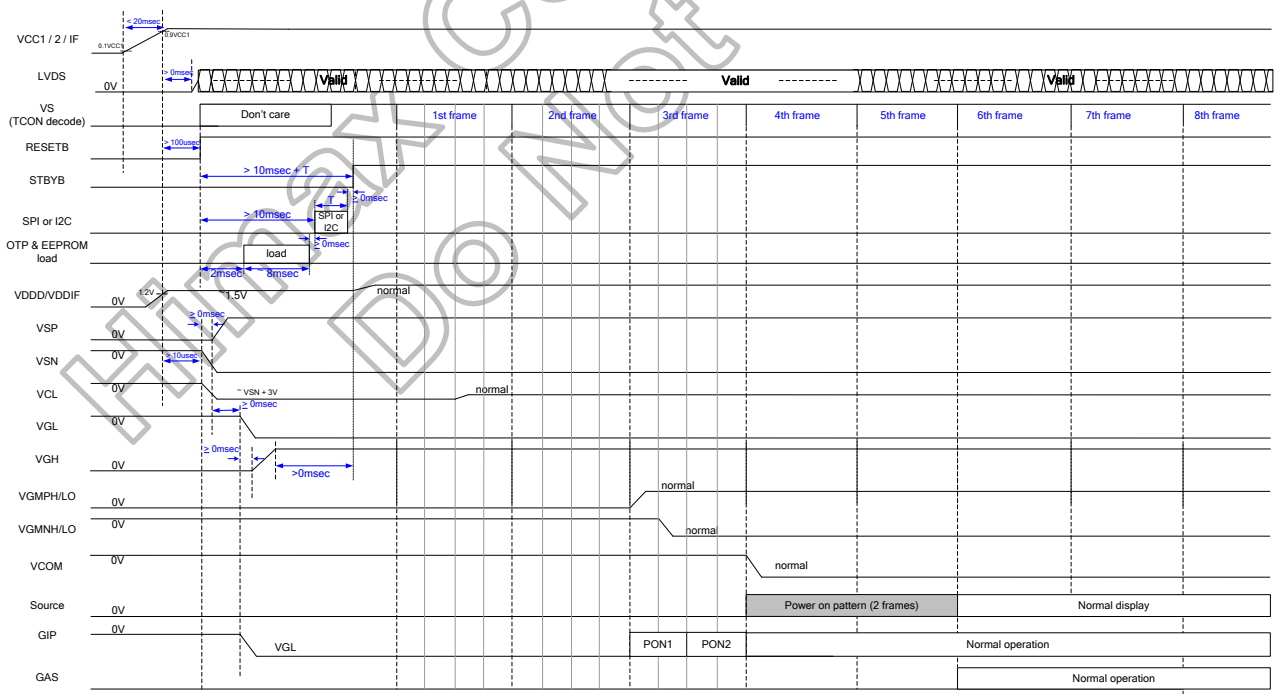

Figure 6.18: Power-on sequence with external VSP/VSN/VGH/VGL (PWR_SPEED=0)

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6.6.2. Power off sequence

A. If VSP and VSN are generated by PFM circuits:

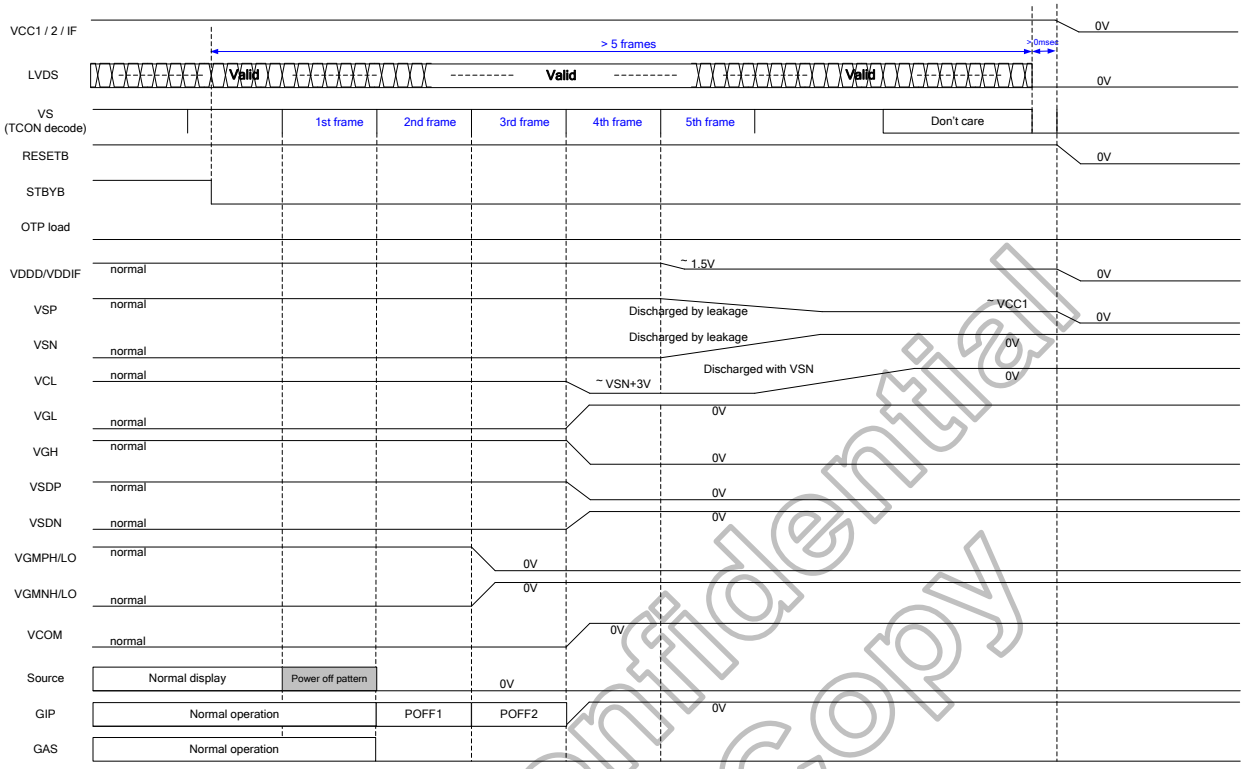

Figure 6.19: Power-off sequence with PFM

B. If VSP=VSDP and VSN=VSDN by external power supply, VGH and VGL generated by internal charge pump circuits:

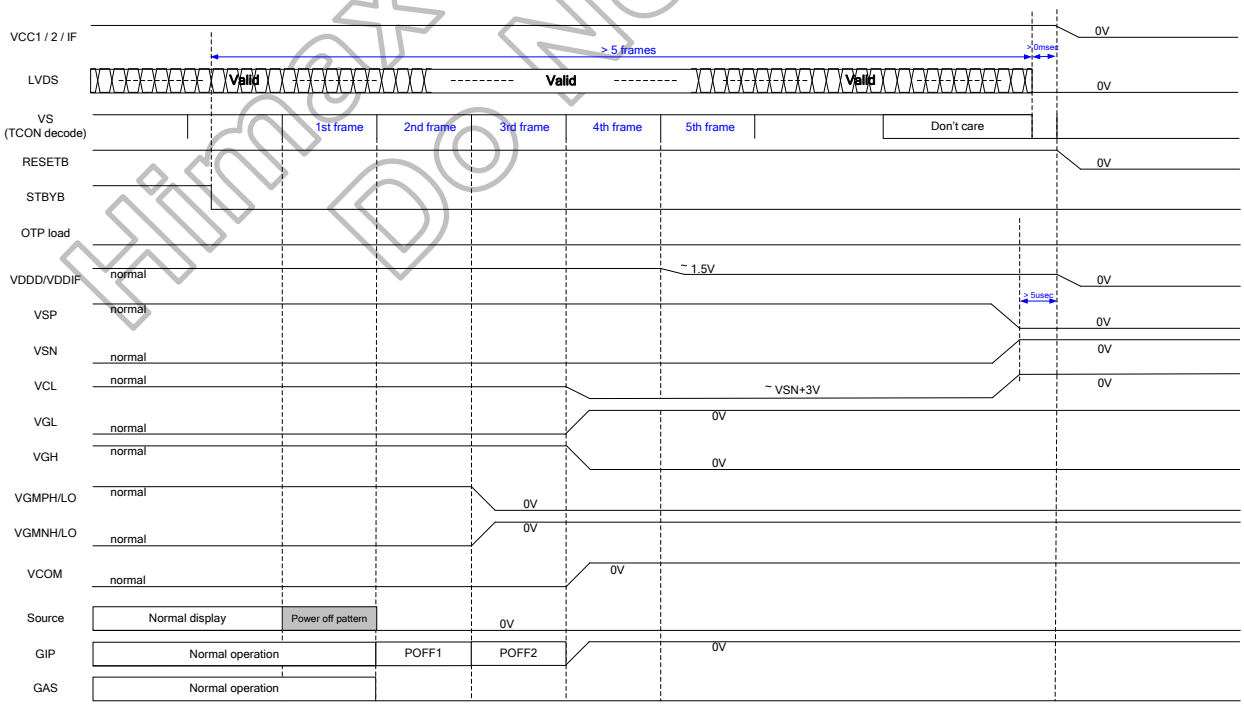

Figure 6.20: Power-off sequence with external VSP/VSN

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C. If VSP=VSDP and VSN=VSDN by external power supply, and VGH and VGL generated by external power supply:

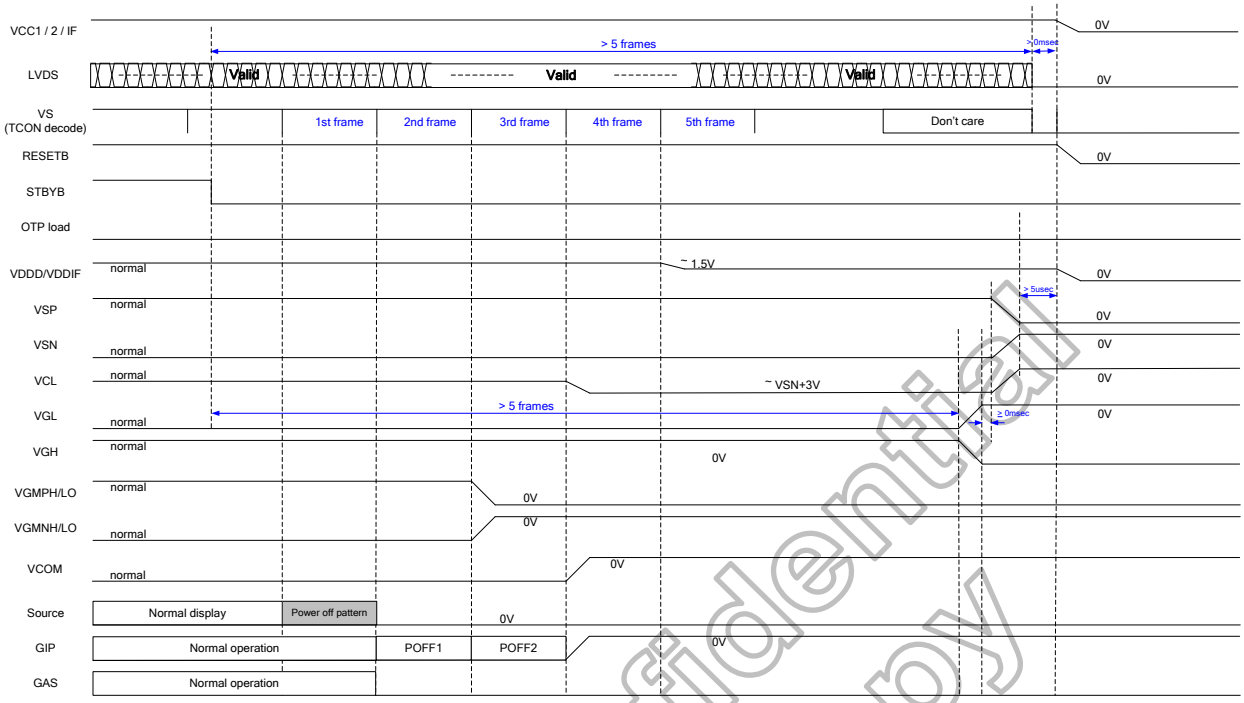

Figure 6.21: Power-off sequence with external VSP/VSN/VGH/VGL

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6.7. PFM setting parameter

In HX82102-A-LT, PFM applies different settings to the power on sequence. Table below is the parameter setting for PFM soft start and normal mode.

	Soft start(1)	Normal
PFM parameter	VSPON_SS1[3:0] VSNON_SS1[3:0] VSPOFF_SS1[3:0] VSNOFF_SS1[3:0] VSPON_SS2[3:0] VSNON_SS2[3:0] VSPOFF_SS2[3:0] VSNOFF_SS2[3:0]	VSPON[4:0] VSNON[4:0] VSPOFF[3:0] VSNOFF[3:0]

Note: (1) VSPON_SS1 / VSPOFF_SS1 **(Page01h R14h)**.
VSNON_SS1 / VSNOFF_SS1 **(Page01h R15h)**.
VSPON_SS2 / VSPOFF_SS2 **(Page01h R0Ah)**.
VSNON_SS2 / VSNOFF_SS2 **(Page01h R0Bh)**.
VSPON / VSPOFF **(Page01h R08h/ Page01h R06h[7])**.
VSNON / VSNOFF **(Page01h R09h/ Page01h R06h[6])**.

Table 6.3: PFM setting parameter

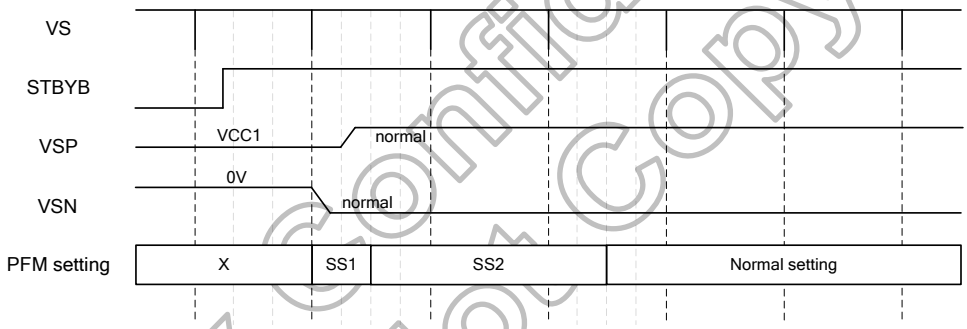

Figure 6.22: PFM power on setting (PFM_SS_SEL=0)

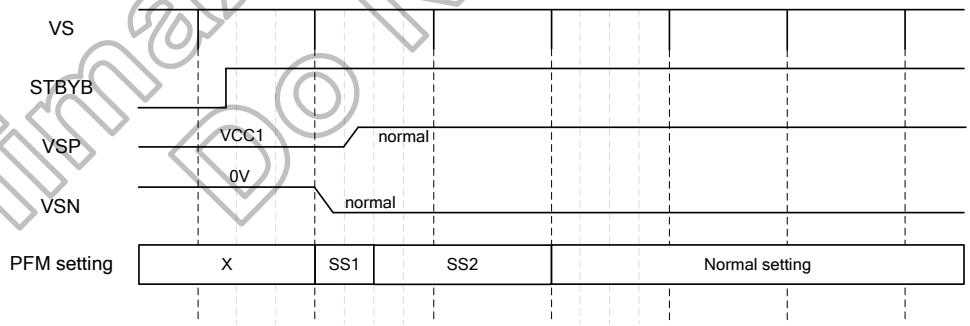

Figure 6.23: PFM power on setting (PFM_SS_SEL=1)

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6.8. TP_SYNC for touch panel synchronization

HX82102-A-LT provides an output TP_SYNC for touch panel synchronization. It can be adjusted by Page03h registers TP_SYNC_SEL[2:0], TP_WIDTH & TP_DLY. The related register let TP_SYNC pin output is HS, VS, VDEN_INT, FAIL_DET, XAO, or Source_SW. VDEN_INT is an internal delayed version of VS, and its width is Vactive. Source_SW is OPA output enable time. TP_DLY is TP_SYNC timing adjustment, and it is effective only when TP_SYNC_SEL[2:0]=3'b011 or 3'b110.

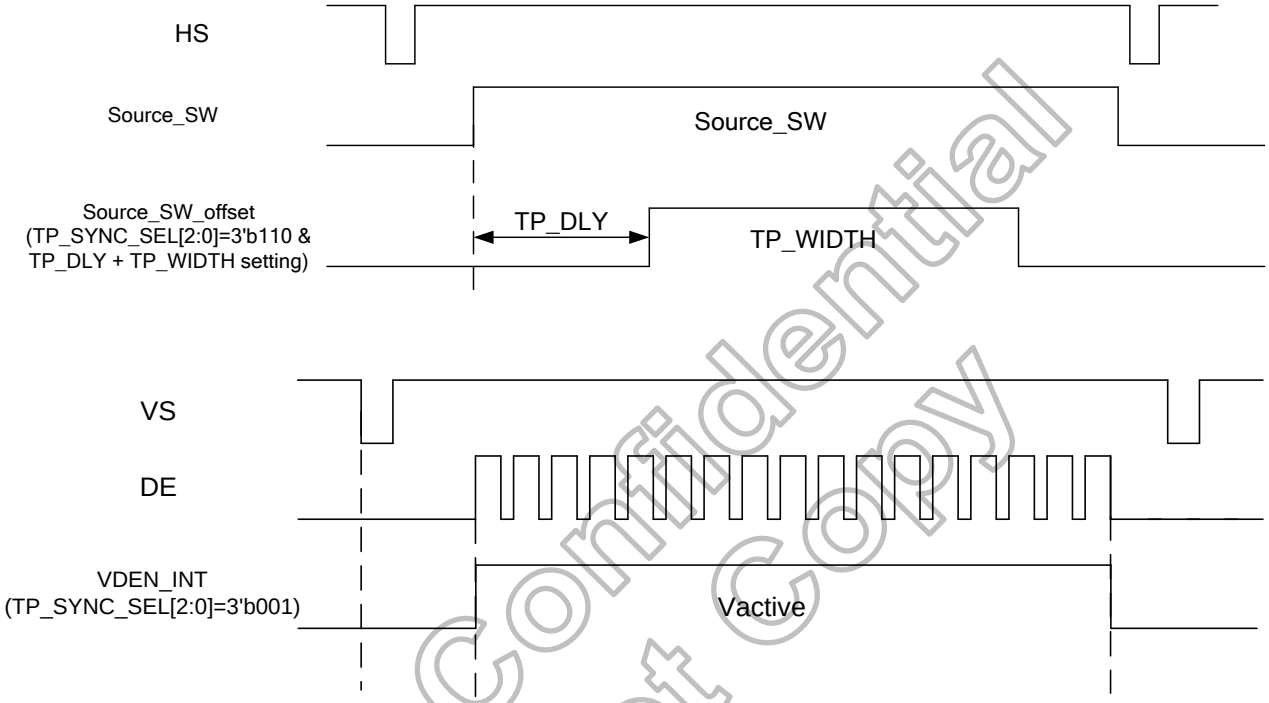

Figure 6.24: TP_SYNC timing adjustment

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6.9. Built-In Self Test function

A BIST **(Built-In Self Test)** pattern generator is embedded in HX82102-A-LT for aging mode. When BISTEN is set to 1 **(by input pin or register)**, HX82102-A-LT will generate the following patterns. When the bit of register PTSEL[15:0] **(Page03h R07h[7:0], R08h[7:0])** to be asserted, means that the corresponding patterns to be selected. The selected patterns will be displayed sequentially and periodically.

If GATEPASS[3:0] **(Page00h R11h[7:4]=5h or HSETPASS[3:0] Page00h R13h[7:4=5h]** is enabled. The frame rate of the display can't guarantee 60Hz at BIST mode.

PTSEL[15:0]	Pattern name	Color	R	G	B
[0]	Full Black	C1	0	0	0
[1]	Full White	C1	255	255	255
[2]	Full Red	C1	255	0	0
[3]	Full Green	C1	0	255	0
[4]	Full Blue	C1	0	0	255
[5]	H Gomi1	C0	255	255	255
		C1	0	0	0
[6]	H Gomi2	C0	0	0	0
		C1	255	255	255
[7]	Cross talk1	C1	128	128	128
		C2	0	0	0
[8]	Cross talk2	C1*(2)	128	128	128
		C2	255	255	255
[9]	Checker board (32x32)	C1	0	0	0
		C2	255	255	255
[10]	Gray Scale 16	C1	0	0	0
		C2	0	0	255
		C3	255	0	0
		C4	255	0	255
		C5	0	255	0
		C6	0	255	255
		C7	255	255	0
		C8	255	255	255
		C9	0	0	0
		C10	36	36	36
		C11	72	72	72
		C12	108	108	108
		C13	144	144	144
		C14	180	180	180
		C15	216	216	216
		C16	255	255	255
[11]	BIST Gray level(1)	C1*(2)	128	128	128
[12]	V Gray scale 256	C1	0~255 increase		
[13]	H Gray scale 256	C1	0~255 increase		
[14]	VCOM trimming	C1	0	0	0
		C2*(2)	128	128	128
[15]	White boarder	C1	255	255	255
		C2	0	0	0

Note: (1) BIST gray level depends on Register Page00h R17h setting value.

Table 6.4: 8-bit mode BIST patterns

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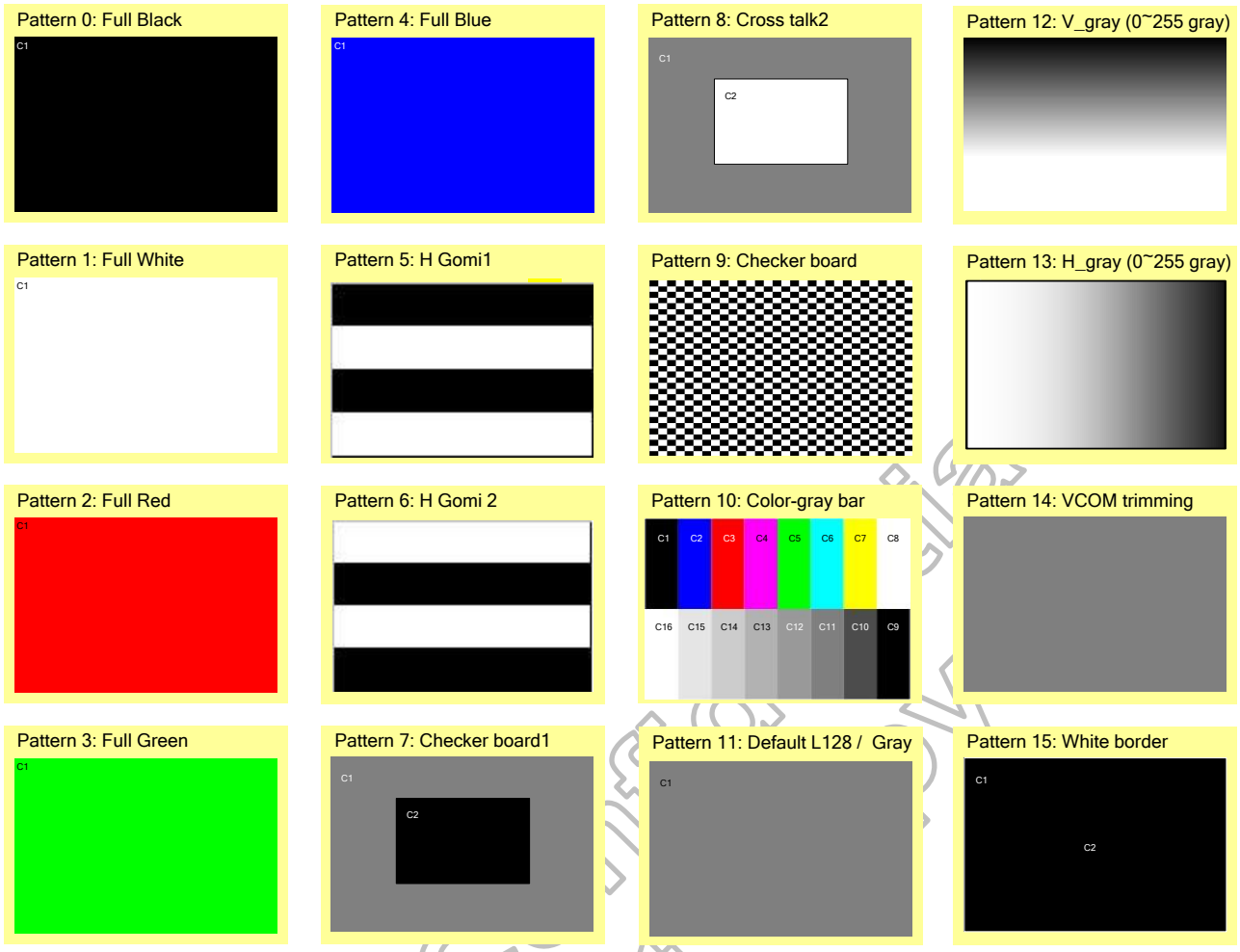
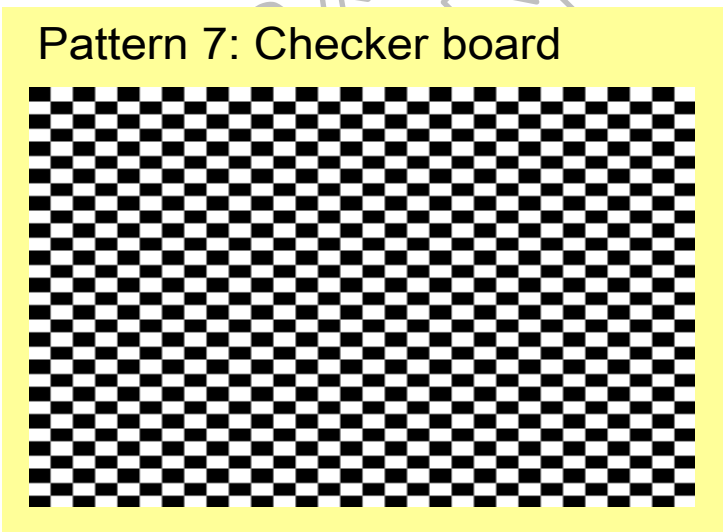
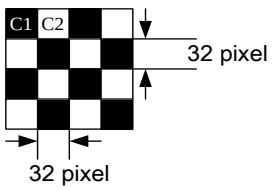


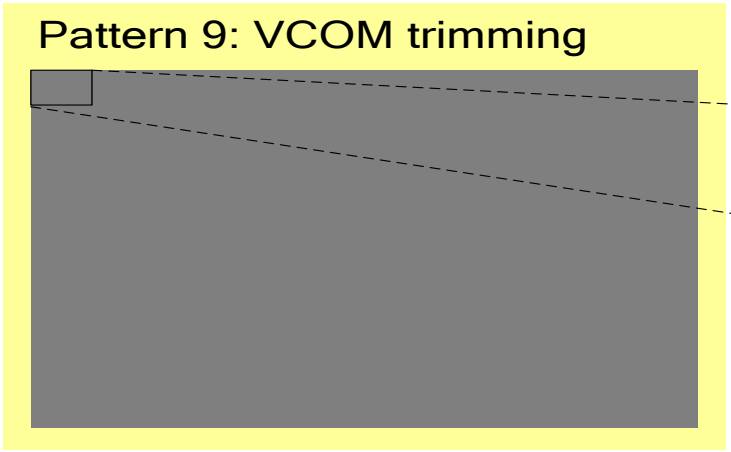
Figure 6.25: BIST patterns

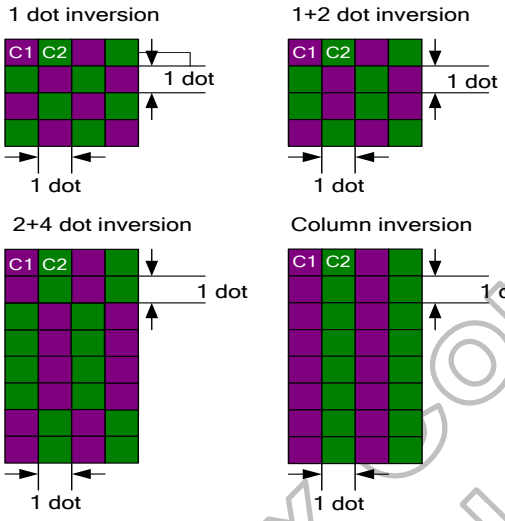
Note: (1) Pattern 7 Checker board pattern is combination of the 32 pixels x 32 pixels black and white block.





(2) Pattern 9 VCOM trimming pattern type is depended on the inversion method.





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6.10. Protection function

6.10.1. GAS function

When power is removed from an electronic device, the image still keeps on the LCD panel for a long time. GAS **(gate all select)** function can speed the process that image disappears.

HX82102-A-LT can detect abnormally low voltage and send GIP signal to the gate by the register setting to discharge residual potential in LCD panel and removes image.

Any one of the following cases with duration larger than 10usec will trigger GAS function.

A. VCC1/2 is lower than 2.4V **(Set by R0Fh[7:5] of Page01h)**
B. VSP is lower than 4V
C. VSN is higher than -4V
D. VGL is higher than VGL x 0.83V **(83%)**

6.10.2. Self protection mode

HX82102-A-LT keeps detecting input signals DE, HS, VS, and DCLK. If any of these signals is missing, HX82102-A-LT will enter self protection mode. In the self protection mode, it would display black or white pattern which could be set in the register. The flow is shown as figure below.

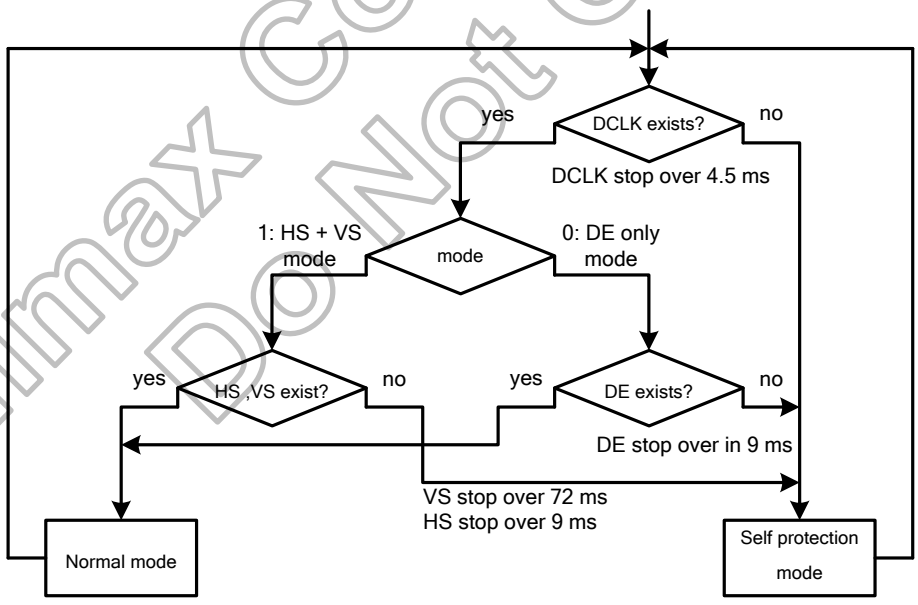

Figure 6.26: Self-protection detection

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6.10.3. CRC

CRC **(cyclic redundancy check)** function is provided to check input RGB data. For each frame, RGB data is calculated with CRC polynomial and initial value. The order of RGB input data can be selected.

The calculated result CRC_SUMO[23:0] is then compared to predicted result CRC_SUMI[23:0]. If calculated result does not match the predicted result, an error flag will be set. Errors are counted and can be checked on CRC_ERRCNT[15:0] register. CRC_SUMO[23:0] can also be read out in selected order.

Note that calculated result of the Nth frame can be read in the (N+1)th frame, predicted result should also be given in the (N+1)th frame, and the error flag is available in the (N+2)th frame.

HX82102-A-LT supports 4 windows for CRC function. CRC_WINx_H1/ CRC_WINx_H2/ CRC_WINx_V1 /RC_WINx_V2 four registers are used to set a window **(x means window number)**. CRC_WINx_H1[11:0] should set to odd numbers, and CRC_WINx_H2[11:0] should be set to even numbers.

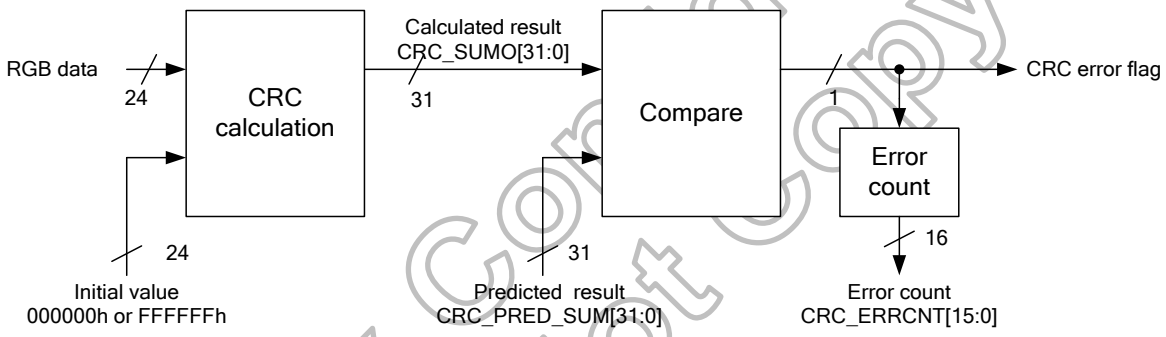

Figure 6.27: CRC function block

CRC type	CRC polynomial
CRC-16	$x^{16}+x^{12}+x^5+1$
CRC-32	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$

Table 6.5: CRC types

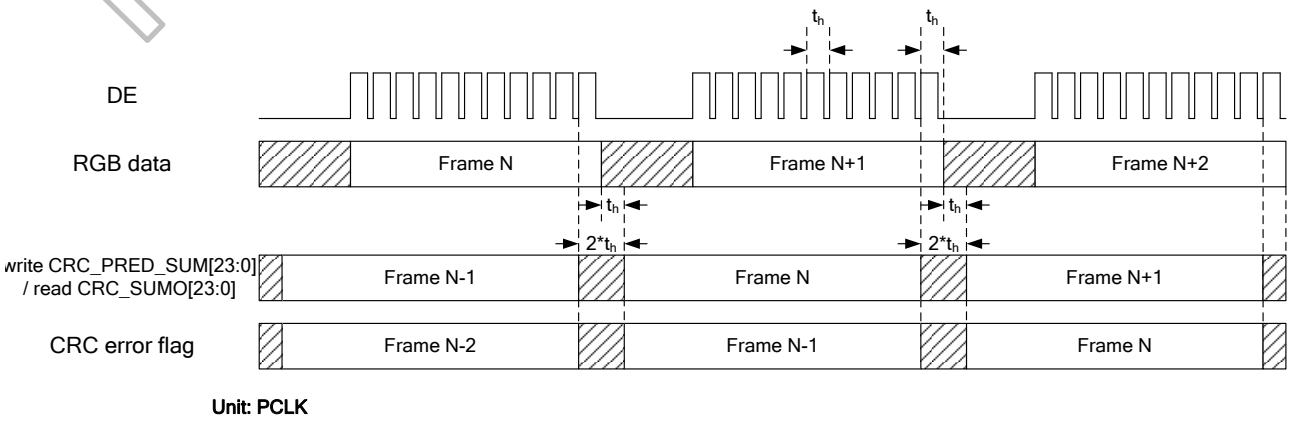

Figure 6.28: CRC timing

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6.10.4. Over current protection

HX82102-A-LT detects the PFM current by monitoring VMONP and VMONN. In any one of the following case, the chip will entry over current protection.

A. DRVP is set to VSS to turn off the external NMOS immediately when VMONP is over its threshold voltage.
B. DRVN is set to VDD to turn off the external PMOS immediately when VMONN is over its threshold voltage.

VMONPS[1:0]: VSP over current detection voltage selection.

VMONPS[1:0]		Function	Note
0	0	0.100V	-
0	1	0.125V	-
1	0	0.150V	Default
1	1	0.175V	-

VMONNS[1:0]: VSN over current detection voltage selection.

VMONNS[1:0]		Function	Note
0	0	0.100V	-
0	1	0.125V	-
1	0	0.150V	Default
1	1	0.175V	-

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6.10.5. Over voltage and low voltage protection

HX82102-A-LT detects the DC/DC voltage for over/low voltage protection function. Display can be inserted black pattern when OVP/LVD trigger period. And it will be reflected to failed detection register and hardware.

Any one of the following cases with duration larger than 8usec will trigger OVP flag.

OVP **(over voltage protection)**:
A. VCC1/2
B. VDDD
C. VSP
D. VSN
E. VGH
F. VGL
G. VCL
H. VCOM
I. VGMPL
J. VGMNL

LVD **(low voltage detection)**:
A. VGH
B. VCL
C. VCOM
D. VSDP
E. VSDN
F. VGMPH
G. VGMNH

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6.11. FAIL detect function

HX82102-A-LT can detect abnormally condition to set the FAIL_DET to low.

Any one of the following cases will trigger the fail detect function to set the FAIL_DET to low. Those follow cases can be enable or disable separate by the register Page04h R02h ~ R06h.

A. OTP values are different with register values after OTP programming.
B. Checksum of EEPROM is wrong after EEPROM reloading.
C. Input signals are detected fail to enter self protection mode.
D. STV signal is detected fail for tradition Gate driver only.
E. Internal source signal output fail.
F. Abnormal low voltages are detected to enter GAS function.
G. Input LVDS signals are unlock.
H. GIP failed detect
I. OVP
J. LVD

The FAIL_DET has two types of output for selection by FAIL_DET_SEL **(Page04h R1h[7])**.The FAIL_DET default output ASIL signal.

ASIL signal output:

FAIL detection item	FAIL_DET output	Note
Normal **(no fail)**	FAIL_DET output STV like.	-
Items A, B, D, E, F, H, I, J	FAIL_DET output low.	-
Items C, G	FAIL_DET output the frequency about 40Hz pulse.	-

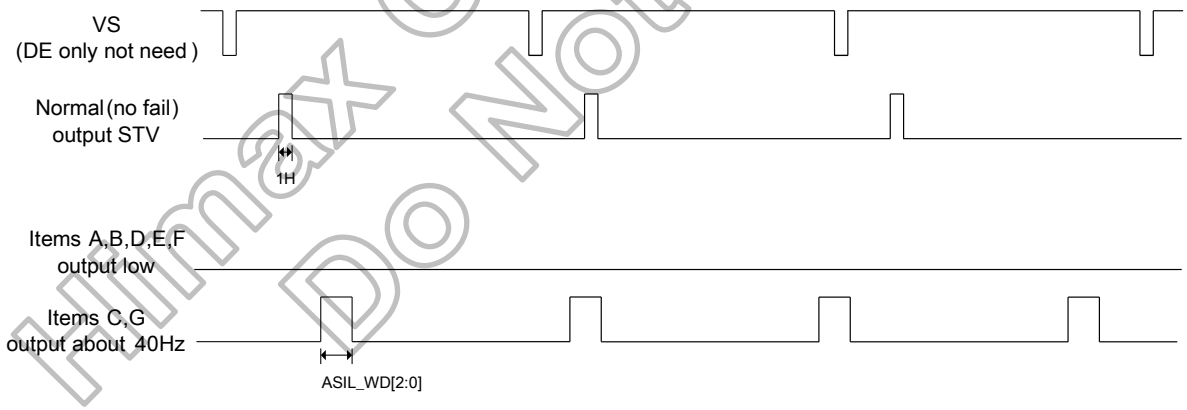

Figure 6.29: FAIL_DET output ASIL signal

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Fail flag output

FAIL detection item	FAIL_DET output	Note
Normal **(no fail)**	FAIL_DET output high.	-
Items A, B, C, D, E, F, G, H, I, J	FAIL_DET output low.	-

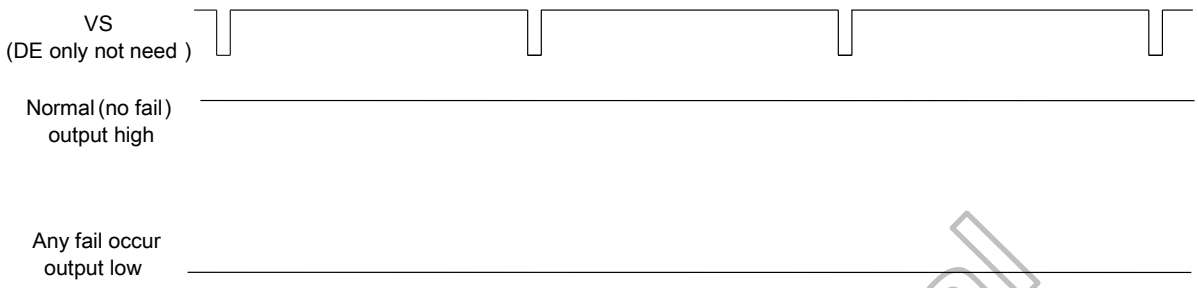

Figure 6.30: FAIL_DET output fail flag

6.12. GATE_NUM_SEL function

GATE_NUM_SEL is a special feature for HX82102-A-LT that can satisfy a variety of vertical resolutions. It can support DE, SYNC and BIST modes. Set GATEPASS[3:0] =5h **(at Page00h R11h[7:4])** to enable the GATE_NUM_SEL, vertical resolution t_{vd} is controlled by GATENUM[11:0] **(at Page00h R10h[7:0] & R11h[3:0])**.

The vertical lines of front end timing must same as GATENUM[11:0] when GATEPASS is enabled.

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6.13. OTP programming sequence

When programming OTP function, the initial value should be written by following steps. The FAIL detection function will detect OTP trimming status.

SIDEN=L, OTP program sequence is executed to all chip. SIDEN=H, OTP program sequence that each chip need to execute independently by SID[1:0] of command.

OTP program sequence is executed to Master IC **(SID[1:0]=LL)** Slave1 IC **(SID[1:0]=LH)** or Slave2 IC **(SID[1:0]=HL)** by OTP_WR1 or OTP_WR2 command.

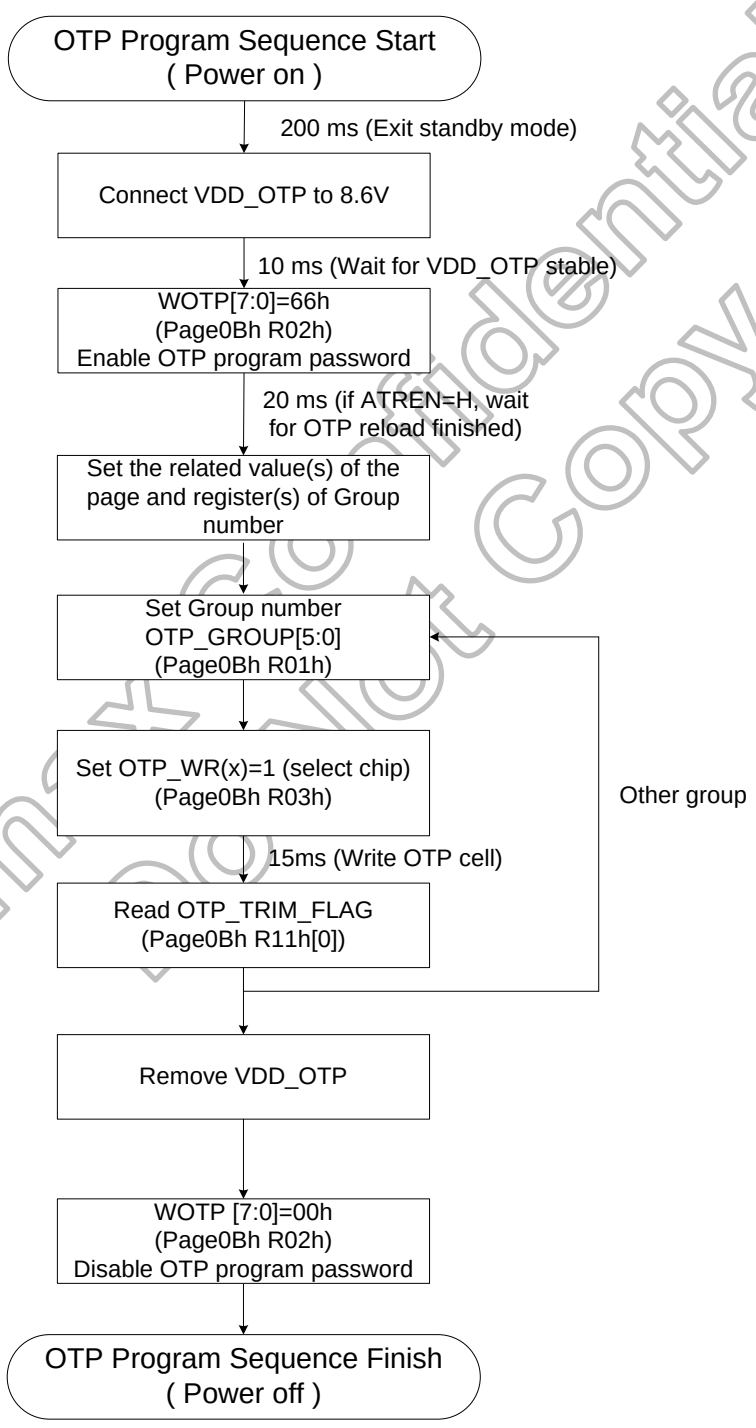

Figure 6.31: OTP program-group flow

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6.14. OTP marginal read

OTP marginal reload provides a critical read condition to filter out “weak programmed” bits. To cover all worse corners, it should be implemented after programming OTP.

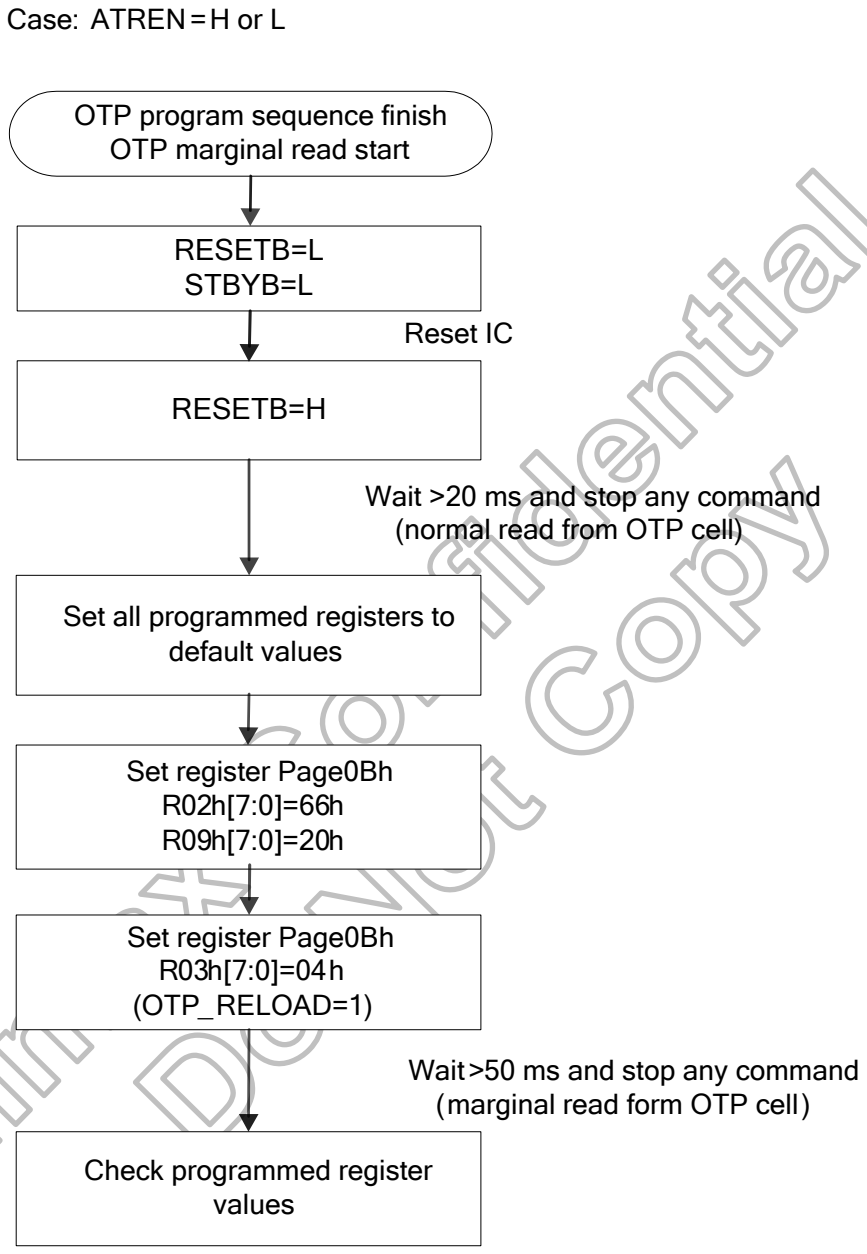

Figure 6.32: OTP marginal read flow

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6.15. SPI Interface

HX82102-A-LT supports 3/4-wire SPI **(serial peripheral interface)** to set internal registers. Setting one command needs 16 SCL clocks. The address and data are transferred from the MSB to LSB edge sequentially at SCL rising edge. Note that ATREN should be set to low when accessing SPI.

A. The first bit R/W selects read/write mode. Setting R/W to 0 selects write mode, and setting R/W to 1 selects read mode.
B. If there are two chips or three chips cascaded, the second and third bits SID[1:0] select chip being active. Note that when SIDEN=L and R/W=1, only read from the master chip.
C. Short the SDAI and SDAO together for 3-wire SPI application.
D. A[4:0] specify the address of the register to be read or written.
E. D[7:0] is the 8-bit data of each register.

SIDEN	R/W	SID[1:0]	Function	Target
L	1	xx	Read	Master
	0	xx	Write	Master and slave
H	1	LL	Read	Master
		LH		Slave1
		HL		Slave2
		HH		Slave3
	0	LL	Write	Master
		LH		Slave1
		HL		Slave2
		HH		Slave3

Table 6.6: SPI timing parameter

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6.15.1. SPI normal read/write mode

In normal write mode, the read/write control bit must be set to 0, and SDAI is address input and data input pin.

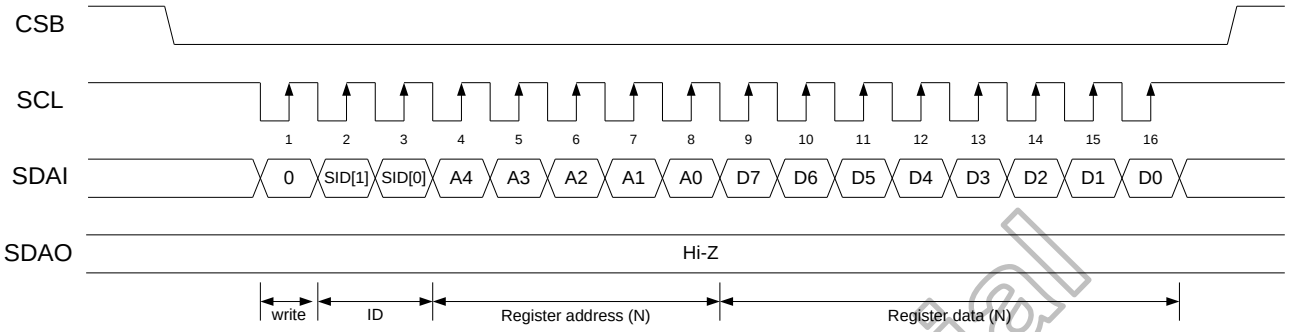

Figure 6.33: SPI signals, normal write mode

In normal read mode, the read/write control bit must be set to 1. The SDAI is address input pin and SDAO is data output pin.

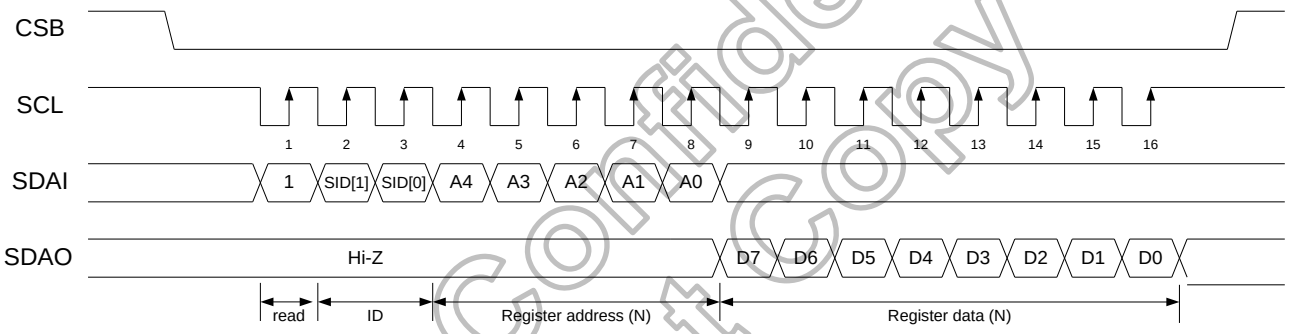

Figure 6.34: SPI signals, normal read mode

6.15.2. SPI burst read/write mode

HX82102-A-LT supports burst mode for writing all registers one time. After choose page want to write, Only the start address is needed, and repeats one set of 8 SCL pulses to access the following registers sequentially.

In burst write mode, the read/write control bit must be set to 0, and SDAI is address input and data input pin.

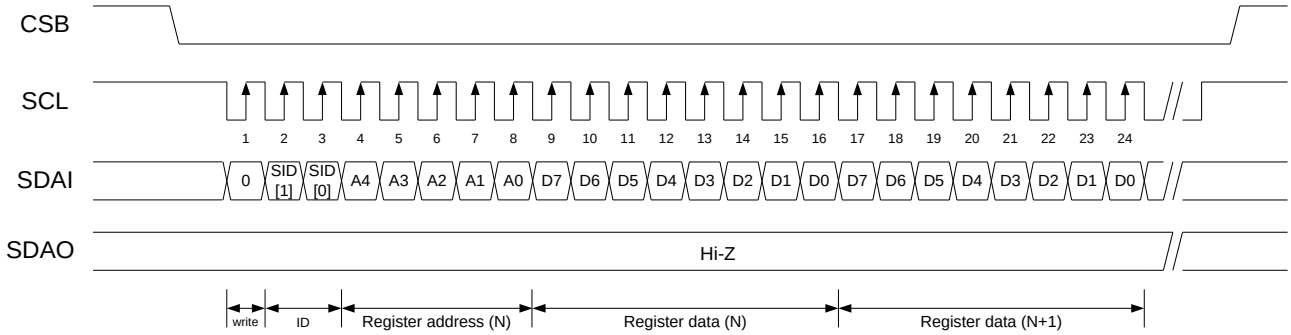

Figure 6.35: SPI signals, burst write mode

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In burst read mode, the read/write control bit must be set to 1. The SDAI is address input pin and SDAO is data output pin.

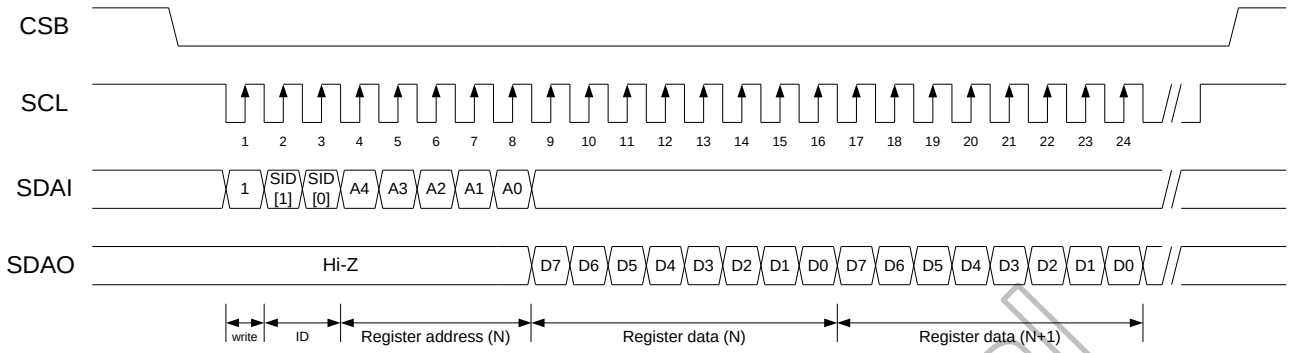

Figure 6.36: SPI signals, burst read mode

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6.16. I2C Interface

HX82102-A-LT supports 2-wire serial interface **(I2C)** to set internal registers.
HX82102-A-LT is a slave and the slave address is fixed 1010010.

A. If there are many chips cascaded, the second and third bits SID[1:0] select chip being active. Note that when SIDEN=L and R/W=1, only read from the master chip.
B. If there are many chips cascaded, when Master chip and slave chips received the slave address from Host, the ACK will response from Master Chip **(SID[1:0]=LL)** only.

SIDEN	R/W	SID[1:0]	Function	Target
L	1	xx	Read	Master
	0	xx	Write	Master and slave
H	1	LL	Read	Master
		LH		Slave1
		HL		Slave2
		HH		Slave3
	0	LL	Write	Master
		LH		Slave1
		HL		Slave2
		HH		Slave3

Table 6.7: I2C timing parameter

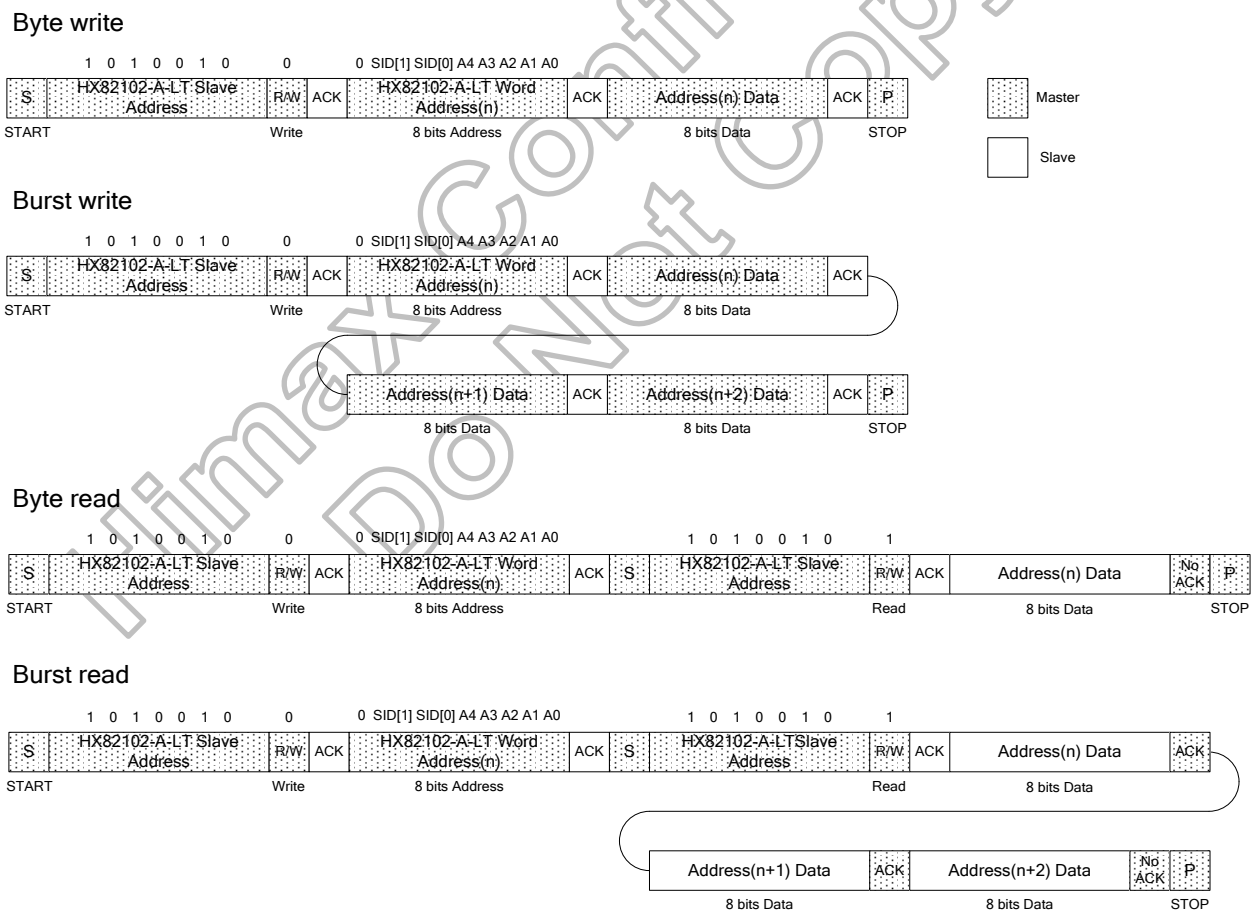

Figure 6.37: I2C R/W format

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6.17. Temperature sensor function

Set TS_H and TS_L to define the low and high temperature region, and each region can set VGMPH/VGMPL/VGMNH/VGMNL/VGH/VGL/VCOM and Analog Gamma Voltage to change the value as the temperature varies.

When TS_GAMMA_EN is set to 1, dynamic settings of analog gamma is enabled. Three sets of analog gamma register values W1, W2 and W3 should be stored in OTP, and the selected set will be loaded from OTP and be effective. Analog gamma settings can be selected by[TS_H:TS_L].

TS_RHL_OPT	TS_GAMMA_EN	TS_VCOM_EN	[TS_H:TS_L]		Effective settings	Note
1	X	X	X	X	By OTP times **(W1->W2->W3)**	Default
0	0	0	X	X		-
0	1	1	L	L	W3	-
			L	H	W2	-
			H	L	W1	-

Table 6.8: Dynamic analog gamma settings

TS_RHL_OPT	TS_GAMMA_EN	[TS_H:TS_L]		Effective settings	Note
1	X	X	X	VGMPHS[4:0]/ VGMPLS[3:0]/ VGMNHS[4:0]/VGMNLS[3:0]	Default
0	0	X	X		-
0	1	L	L		-
		L	H	VGMPHS_LT[4:0]/ VGMPLS_LT[3:0]/ VGMNHS_LT[4:0]/ VGMNLS_LT[3:0]	-
		H	L	VGMPHS_HT[4:0]/ VGMPLS_HT[3:0]/ VGMNHS_HT[4:0]/ VGMNLS_HT[3:0]	-

Table 6.9: Dynamic gamma reference settings

TS_RHL_OPT	TS_VCOM_EN	[TS_H:TS_L]		Effective settings	Note
1	X	X	X	VCOMS[8:0]	Default
0	0	X	X		-
0	1	L	L		-
		L	H	VCOMS_LT[8:0]	-
		H	L	VCOMS_HT[8:0]	-

Table 6.10: Dynamic VCOM settings

TS_RHL_OPT	TS_VGHL_EN	[TS_H:TS_L]		Effective settings	Note
1	X	X	X	VGHS[6:0], VGLS[5:0]	Default
0	0	X	X	VGHS[6:0], VGLS[5:0]	-
0	1	L	L	VGHS[6:0], VGLS[5:0]	-
		L	H	VGHS_LT[6:0], VGLS_LT[5:0]	-
		H	L	VGHS_HT[6:0], VGLS_HT[5:0]	-

Table 6.11: Dynamic VGH and VGL settings

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6.18. Multiple frame polarity control and INTLB

Suppose a “P frame” is defined as the first source output starting with positive polarity, and an “N frame” is defined as starting with negative polarity. Normally frame polarity is changed by frame, that is odd frames are P frames and even frames are N frames.

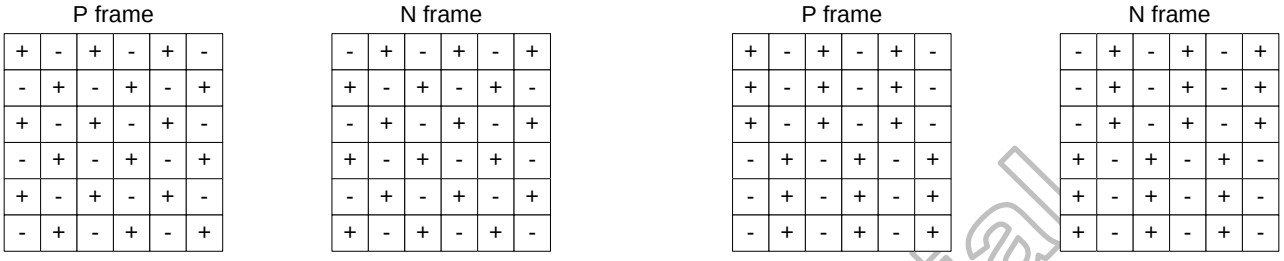

Figure 6.38: Definition of frame polarity

It is able to be inversed periodically for 2^K frames by setting POL_INV_FRM[3:0] to K, maximum period is 4096 frames. VCOM value VCOMS[7:0] is added an offset VCOMSOFS[7:0] ranging from -127 to +127.

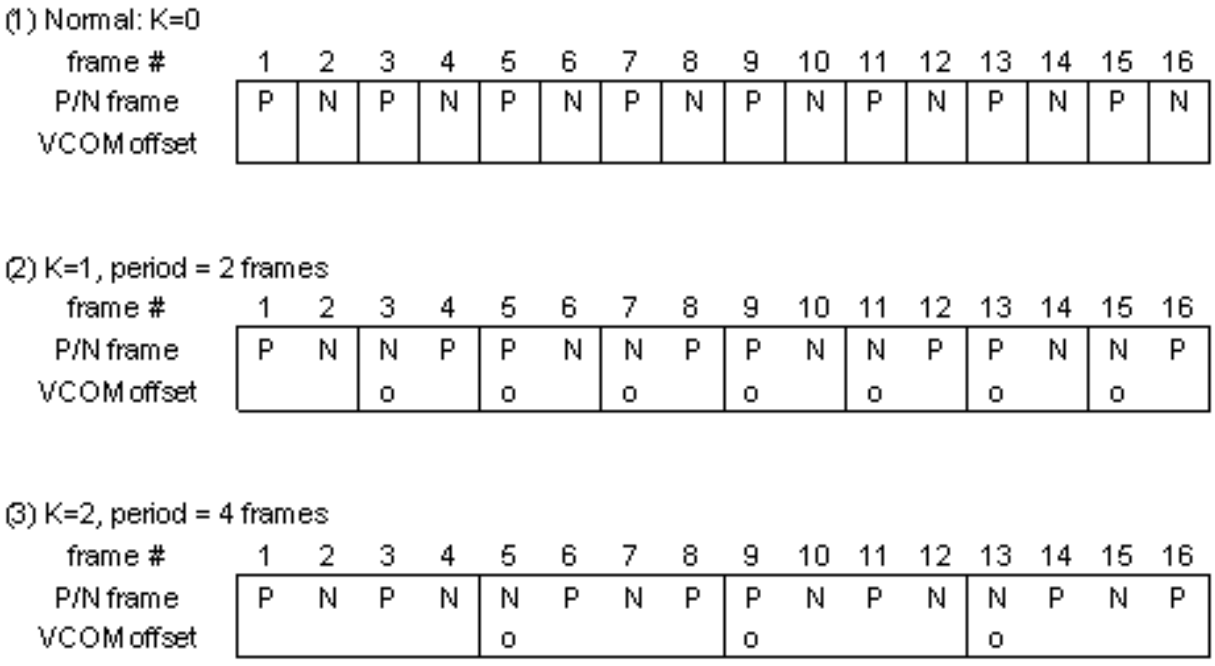

Figure 6.39: Multiple frame polarity control

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7. Gamma Correction Function

7.1. Analog gamma structure

For positive polarity, three voltages VGMPH/M/LO are generated as gamma reference, where VGMPMO is equal to 0.5*(VGMPHO+VGMPLO). They are connected to VGMPH/M/LI and used to generate all gamma reference voltages. GSH0/2/4/8/14/22/30/47/79/111/143/175/207/224/232/240/246/251/253/255, and all grayscale voltages are GSH[0:255].

For negative polarity, the structure is exactly the same to positive gamma circuit.

7.1.1. Equation for gamma code

The reference voltages can be set by registers, as described in the following table.

Setting for positive gamma voltage

Gamma code	Register	Reference voltage
GSH0	T_VP0_[4:0]	VGMPL + (1/512)*(VP0_[4:0]*2)*(VGMPH – VGMPL)
GSH2	T_VP2_[5:0]	VGMPL + (1/512)*(VP2_[5:0]*2 + 2)*(VGMPH – VGMPL)
GSH4	T_VP4_[5:0]	VGMPL + (1/512)*(VP4_[5:0]*2 + 10)*(VGMPH – VGMPL)
GSH8	T_VP8_[5:0]	VGMPL + (1/512)*(VP8_[5:0]*2 + 28)*(VGMPH – VGMPL)
GSH14	T_VP14_[5:0]	VGMPL + (1/512)*(VP14_[5:0]*2 + 53)*(VGMPH – VGMPL)
GSH22	T_VP22_[5:0]	GSH14 + (1/250)*(VP22_[5:0] + 5)*(GSH240 – GSH14)
GSH30	T_VP30_[5:0]	GSH14 + (1/250)*(VP30_[5:0] + 13)*(GSH240 – GSH14)
GSH47	T_VP47_[5:0]	GSH14 + (1/250)*(VP47_[5:0] + 27)*(GSH240 – GSH14)
GSH79	T_VP79_[5:0]	GSH14 + (1/250)*(VP79_[5:0] + 47)*(GSH240 – GSH14)
GSH111	T_VP111_[5:0]	GSH14 + (1/250)*(VP111_[5:0] + 67)*(GSH240 – GSH14)
GSH143	T_VP143_[5:0]	GSH14 + (1/250)*(VP143_[5:0] + 87)*(GSH240 – GSH14)
GSH175	T_VP175_[5:0]	GSH14 + (1/250)*(VP175_[5:0] + 123)*(GSH240 – GSH14)
GSH207	T_VP207_[5:0]	GSH14 + (1/250)*(VP207_[5:0] + 163)*(GSH240 – GSH14)
GSH224	T_VP224_[5:0]	GSH14 + (1/250)*(VP224_[5:0] + 183)*(GSH240 – GSH14)
GSH232	T_VP232_[5:0]	GSH14 + (1/250)*(VP232_[5:0] + 186)*(GSH240 – GSH14)
GSH240	T_VP240_[5:0]	VGMPL + (1/512)*(VP240_[5:0]*2 + 334)*(VGMPH – VGMPL)
GSH246	T_VP246_[5:0]	VGMPL + (1/512)*(VP246_[5:0]*2 + 376)*(VGMPH – VGMPL)
GSH251	T_VP251_[5:0]	VGMPL + (1/512)*(VP251_[5:0]*2 + 380)*(VGMPH – VGMPL)
GSH253	T_VP253_[5:0]	VGMPL + (1/512)*(VP253_[5:0]*2 + 384)*(VGMPH – VGMPL)
GSH255	T_VP255_[4:0]	VGMPL + (1/512)*(VP255_[4:0]*2 + 450)*(VGMPH – VGMPL)

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Setting for negative gamma voltage

Gamma code	Register	Reference voltage
GSL0	T_VN0_[4:0]	VGMNL + (1/512)*(VN0_[4:0]*2)*(VGMNH – VGMNL)
GSL2	T_VN2_[5:0]	VGMNL + (1/512)*(VN2_[5:0]*2 + 2)*(VGMNH – VGMNL)
GSL4	T_VN4_[5:0]	VGMNL + (1/512)*(VN4_[5:0]*2 + 10)*(VGMNH – VGMNL)
GSL8	T_VN8_[5:0]	VGMNL + (1/512)*(VN8_[5:0]*2 + 28)*(VGMNH – VGMNL)
GSL14	T_VN14_[5:0]	VGMNL + (1/512)*(VN14_[5:0]*2 + 53)*(VGMNH – VGMNL)
GSL22	T_VN22_[5:0]	GSL14 + (1/250)*(VN22_[5:0] + 5)*(GSL240 – GSL14)
GSL30	T_VN30_[5:0]	GSL14 + (1/250)*(VN30_[5:0] + 13)*(GSL240 – GSL14)
GSL47	T_VN47_[5:0]	GSL14 + (1/250)*(VN47_[5:0] + 27)*(GSL240 – GSL14)
GSL79	T_VN79_[5:0]	GSL14 + (1/250)*(VN79_[5:0] + 47)*(GSL240 – GSL14)
GSL111	T_VN111_[5:0]	GSL14 + (1/250)*(VN111_[5:0] + 67)*(GSL240 – GSL14)
GSL143	T_VN143_[5:0]	GSL14 + (1/250)*(VN143_[5:0] + 87)*(GSL240 – GSL14)
GSL175	T_VN175_[5:0]	GSL14 + (1/250)*(VN175_[5:0] + 123)*(GSL240 – GSL14)
GSL207	T_VN207_[5:0]	GSL14 + (1/250)*(VN207_[5:0] + 163)*(GSL240 – GSL14)
GSL224	T_VN224_[5:0]	GSL14 + (1/250)*(VN224_[5:0] + 183)*(GSL240 – GSL14)
GSL232	T_VN232_[5:0]	GSL14 + (1/250)*(VN232_[5:0] + 186)*(GSL240 – GSL14)
GSL240	T_VN240_[5:0]	VGMNL + (1/512)*(VN240_[5:0]*2 + 334)*(VGMNH – VGMNL)
GSL246	T_VN246_[5:0]	VGMNL + (1/512)*(VN246_[5:0]*2 + 376)*(VGMNH – VGMNL)
GSL251	T_VN251_[5:0]	VGMNL + (1/512)*(VN251_[5:0]*2 + 380)*(VGMNH – VGMNL)
GSL253	T_VN253_[5:0]	VGMNL + (1/512)*(VN253_[5:0]*2 + 384)*(VGMNH – VGMNL)
GSL255	T_VN255_[4:0]	VGMNL + (1/512)*(VN255_[4:0]*2 + 450)*(VGMNH – VGMNL)

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7.1.2. Resistor ratio for gamma code

Resistor ratio in the resistor chain 3 of both positive and negative gamma circuits is described in the following table. The resistor RGMA[k] is between GSH[k] and GSH[k-1], or GSL[k] and GSL[k-1].

Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio
RGMA[255]	17R	RGMA[223]	4.333R	RGMA[191]	2.813R	RGMA[159]	2.188R
RGMA[254]	16R	RGMA[222]	4.333R	RGMA[190]	2.813R	RGMA[158]	2.188R
RGMA[253]	14.5R	RGMA[221]	4.333R	RGMA[189]	2.813R	RGMA[157]	2.188R
RGMA[252]	13R	RGMA[220]	4.333R	RGMA[188]	2.813R	RGMA[156]	2.188R
RGMA[251]	13R	RGMA[219]	4.063R	RGMA[187]	2.75R	RGMA[155]	2.125R
RGMA[250]	12R	RGMA[218]	4.063R	RGMA[186]	2.75R	RGMA[154]	2.125R
RGMA[249]	12R	RGMA[217]	4.063R	RGMA[185]	2.75R	RGMA[153]	2.125R
RGMA[248]	11R	RGMA[216]	4.063R	RGMA[184]	2.75R	RGMA[152]	2.125R
RGMA[247]	11R	RGMA[215]	3.813R	RGMA[183]	2.625R	RGMA[151]	2.063R
RGMA[246]	10R	RGMA[214]	3.813R	RGMA[182]	2.625R	RGMA[150]	2.063R
RGMA[245]	10R	RGMA[213]	3.813R	RGMA[181]	2.625R	RGMA[149]	2.063R
RGMA[244]	9R	RGMA[212]	3.813R	RGMA[180]	2.625R	RGMA[148]	2.063R
RGMA[243]	9R	RGMA[211]	3.5R	RGMA[179]	2.5R	RGMA[147]	2R
RGMA[242]	8R	RGMA[210]	3.5R	RGMA[178]	2.5R	RGMA[146]	2R
RGMA[241]	8R	RGMA[209]	3.5R	RGMA[177]	2.5R	RGMA[145]	2R
RGMA[240]	7R	RGMA[208]	3.5R	RGMA[176]	2.5R	RGMA[144]	2R
RGMA[239]	7R	RGMA[207]	3.5R	RGMA[175]	2.5R	RGMA[143]	2R
RGMA[238]	6.5R	RGMA[206]	3.5R	RGMA[174]	2.5R	RGMA[142]	2R
RGMA[237]	6R	RGMA[205]	3.5R	RGMA[173]	2.5R	RGMA[141]	2R
RGMA[236]	5.75R	RGMA[204]	3.5R	RGMA[172]	2.5R	RGMA[140]	2R
RGMA[235]	5.5R	RGMA[203]	3.313R	RGMA[171]	2.375R	RGMA[139]	1.938R
RGMA[234]	5.25R	RGMA[202]	3.313R	RGMA[170]	2.375R	RGMA[138]	1.938R
RGMA[233]	5R	RGMA[201]	3.313R	RGMA[169]	2.375R	RGMA[137]	1.938R
RGMA[232]	4.75R	RGMA[200]	3.313R	RGMA[168]	2.375R	RGMA[136]	1.938R
RGMA[231]	4.75R	RGMA[199]	3.063R	RGMA[167]	2.313R	RGMA[135]	1.938R
RGMA[230]	4.75R	RGMA[198]	3.063R	RGMA[166]	2.313R	RGMA[134]	1.938R
RGMA[229]	4.75R	RGMA[197]	3.063R	RGMA[165]	2.313R	RGMA[133]	1.938R
RGMA[228]	4.5R	RGMA[196]	3.063R	RGMA[164]	2.313R	RGMA[132]	1.938R
RGMA[227]	4.5R	RGMA[195]	2.938R	RGMA[163]	2.25R	RGMA[131]	1.915R
RGMA[226]	4.5R	RGMA[194]	2.938R	RGMA[162]	2.25R	RGMA[130]	1.915R
RGMA[225]	4.5R	RGMA[193]	2.938R	RGMA[161]	2.25R	RGMA[129]	1.915R
RGMA[224]	4.66R	RGMA[192]	2.938R	RGMA[160]	2.25R	RGMA[128]	1.915R

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Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio
RGMA[127]	1.915R	RGMA[95]	1.875R	RGMA[63]	2.313R	RGMA[31]	3.75R
RGMA[126]	1.915R	RGMA[94]	1.875R	RGMA[62]	2.313R	RGMA[30]	4.2R
RGMA[125]	1.915R	RGMA[93]	1.875R	RGMA[61]	2.313R	RGMA[29]	4.33R
RGMA[124]	1.915R	RGMA[92]	1.875R	RGMA[60]	2.313R	RGMA[28]	4.5R
RGMA[123]	1.875R	RGMA[91]	1.875R	RGMA[59]	2.438R	RGMA[27]	4.66R
RGMA[122]	1.875R	RGMA[90]	1.875R	RGMA[58]	2.438R	RGMA[26]	4.75R
RGMA[121]	1.875R	RGMA[89]	1.875R	RGMA[57]	2.438R	RGMA[25]	5R
RGMA[120]	1.875R	RGMA[88]	1.875R	RGMA[56]	2.438R	RGMA[24]	5.1R
RGMA[119]	1.875R	RGMA[87]	1.875R	RGMA[55]	2.563R	RGMA[23]	5.2R
RGMA[118]	1.875R	RGMA[86]	1.875R	RGMA[54]	2.563R	RGMA[22]	5.5R
RGMA[117]	1.875R	RGMA[85]	1.875R	RGMA[53]	2.563R	RGMA[21]	5.8R
RGMA[116]	1.875R	RGMA[84]	1.875R	RGMA[52]	2.563R	RGMA[20]	6R
RGMA[115]	1.875R	RGMA[83]	1.875R	RGMA[51]	2.75R	RGMA[19]	6.2R
RGMA[114]	1.875R	RGMA[82]	1.875R	RGMA[50]	2.75R	RGMA[18]	6.33R
RGMA[113]	1.875R	RGMA[81]	1.875R	RGMA[49]	2.75R	RGMA[17]	6.5R
RGMA[112]	1.875R	RGMA[80]	1.875R	RGMA[48]	2.75R	RGMA[16]	6.75R
RGMA[111]	1.875R	RGMA[79]	2R	RGMA[47]	2.875R	RGMA[15]	7.125R
RGMA[110]	1.875R	RGMA[78]	2R	RGMA[46]	2.875R	RGMA[14]	8R
RGMA[109]	1.875R	RGMA[77]	2R	RGMA[45]	2.875R	RGMA[13]	8.25R
RGMA[108]	1.875R	RGMA[76]	2R	RGMA[44]	2.875R	RGMA[12]	8.75R
RGMA[107]	1.875R	RGMA[75]	2.063R	RGMA[43]	3.063R	RGMA[11]	9.5R
RGMA[106]	1.875R	RGMA[74]	2.063R	RGMA[42]	3.063R	RGMA[10]	10.25R
RGMA[105]	1.875R	RGMA[73]	2.063R	RGMA[41]	3.063R	RGMA[9]	10.5R
RGMA[104]	1.875R	RGMA[72]	2.063R	RGMA[40]	3.063R	RGMA[8]	12R
RGMA[103]	1.875R	RGMA[71]	2.125R	RGMA[39]	3.313R	RGMA[7]	13R
RGMA[102]	1.875R	RGMA[70]	2.125R	RGMA[38]	3.313R	RGMA[6]	14R
RGMA[101]	1.875R	RGMA[69]	2.125R	RGMA[37]	3.313R	RGMA[5]	13R
RGMA[100]	1.875R	RGMA[68]	2.125R	RGMA[36]	3.313R	RGMA[4]	11R
RGMA[99]	1.875R	RGMA[67]	2.208R	RGMA[35]	3.5R	RGMA[3]	10R
RGMA[98]	1.875R	RGMA[66]	2.208R	RGMA[34]	3.5R	RGMA[2]	9R
RGMA[97]	1.875R	RGMA[65]	2.208R	RGMA[33]	3.5R	RGMA[1]	8R
RGMA[96]	1.875R	RGMA[64]	2.208R	RGMA[32]	3.5R	-	-

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8. Register Function

8.1. Register table

8.1.1. Register table: Page00h (Normal function setting)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	0Ch	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7]	GOA_ENB	Gate type selection.	Group1 **(2 times)**
		R/W	[6:4]	PTS[2:0]	Panel type selection.	
		R/W	[3:2]	ZZS[1:0]	Zig-Zag type selection.	
		R/W	[1:0]	GSEL[1:0]	Dual Gate on sequence select	
02h	71h	R/W	[7:6]	TR[1:0]	Interface selection	
		R/W	[5]	DINT	Input data 6-bit or 8-bit selection.	
		R/W	[4]	MODE	Sync or DE mode selection.	
		R/W	[3]	HSP	HS polarity.	
		R/W	[2]	VSP	VS polarity.	
		R/W	[1]	CLOCKP	Clock latch data edge for TTL mode.	
		R/W	[0]	NB	Normally white/black selection.	
03h	00h	R/W	[7]	RL	Horizontal scan direction.	
		R/W	[6]	TB	Vertical scan direction.	
		R/W	[5:4]	INV[1:0]	Inversion algorithm selection.	
		R/W	[3:0]	RS[3:0]	Resolution selection.	
04h	04h	R/W	[7]	RB_INV	R data and B data exchange.	
		R/W	[6]	DGAMEN	Digital Gamma function enable.	
		R/W	[5:4]	GPOS[1:0]	Tradition Gate driver location.	
		R/W	[3:2]	SD_GND_V[1:0]	Source output state in vertical blanking.	
		R/W	[1]	PON	White/Black pattern selection at power on sequence.	
		R/W	[0]	POFF	White/Black pattern selection at power off sequence.	
05h	C5h	R/W	[7]	GASEN	GAS function enable.	
		R/W	[6]	SPFEN	Self-protection mode enables.	
		R/W	[5]	SPFSEL	White/Black pattern selection in self-protection mode.	
		R/W	[4]	BISTEN	BIST mode enable.	
		R/W	[3:2]	SD_CLK_SEL[1:0]	GIP/Source clock selection.	
		R/W	[1:0]	BIST_FNUM[1:0]	BIST pattern refresh frame setting	
06h	08h	R/W	[7:0]	VSTS[7:0]	Vertical back porch adjustment.	Group 2 **(2 times)**
07h	10h	R/W	[7:0]	HSTS[7:0]	Horizontal back porch adjustment.	
08h	C9h	R/W	[7]	PWR_SPEED	Speed power on enable.	
		R/W	[6]	TS_RHL_OPT	VGMPHS,VGMNHS,VGMPLS,VGMNLS,VGHS, VGLS,VCOM,AGAM select by TS or OTP flag.	
		R/W	[5:0]	OEW[5:0]	Timing for gate driver control.	
09h	86h	R/W	[7]	-	Reserved.	
		R/W	[6]	-	Reserved.	
		R/W	[5:0]	GEQW[5:0]	Time for pre-charging source output to ground.	
0Ah	8Fh	R/W	[7:6]	PCR[1:0]	Source SW divided selection.	
		R/W	[5:0]	EQ0W[5:0]	Time for pre-charging source output to ground.	
0Bh	30h	R/W	[7]	-	Reserved.	
		R/W	[6:4]	BC[2:0]	Source driver bias current selection.	
		R/W	[3:2]	POCSD[1:0]	Source output offset cancelling selection.	
		R/W	[1:0]	POCGM[1:0]	Gamma offset cancelling selection.	
0Ch	80h	R/W	[7]	-	Reserved.	
		R/W	[6:4]	CAS_DEL_OPT[2:0]	Cascade delay signal.	
		R/W	[3]	RGATE	Dual gate interlace GATE swap.	
		R/W	[2]	GM_SWAP	Gate line and color filter mapping selection.	
		R/W	[1]	DUAL_F	Dual gate frame inversion.	
		R/W	[0]	TP_SYNC_VBLK	TPSYNC output in vertical blanking.	
0Dh	80h	R/W	[7:6]	OSC_BISTS[1:0]	Source/GIP clock selection in BIST mode.	
		R/W	[5:4]	BISTS_CLK_SEL[1:0]	OSC_BISTS division.	
		R/W	[3:0]	BIST_VFP[3:0]	BIST mode vertical back porch adjustment.	

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Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
0Eh	10h	R/W	[7:6]	-	Reserved.	Group 3 **(2 times)**
		R/W	[5:0]	ROB[5:0]	Offset of Red data.	
0Fh	10h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	GOB[5:0]	Offset of Green data.	
10h	10h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	BOB[5:0]	Offset of Blue data.	
11h	80h	R/W	[7:0]	RGC[7:0]	Gain of Red data.	
12h	80h	R/W	[7:0]	GGC[7:0]	Gain of Green data.	
13h	80h	R/W	[7:0]	BGC[7:0]	Gain of Blue data.	
14h	68h	R/W	[7:0]	GATENUM[7:0]	Vertical resolution setting when manual selection is enabled. VRES=GATENUM[11:0] * 1	Group 4 **(2 times)**
15h	A1h	R/W	[7:4]	GATEPASS[3:0]	Password for manual vertical resolution selection.	
		R/W	[3:0]	GATENUM[11:8]	Vertical resolution setting when manual selection is enabled. VRES=GATENUM[11:0] * 1	
16h	00h	R/W	[7:0]	HSETNUM[7:0]	Horizontal resolution setting when manual selection is enabled. HRES=HSETNUM[10:0]	
17h	A5h	R/W	[3:0]	HSETPASS[3:0]	Password for manual horizontal resolution Selection	
		R/W	[7:0]	HSETNUM[11:8]	Horizontal resolution setting when manual selection is enabled. HRES=HSETNUM[10:0]	
18h	00h	R/W	[7:0]	BIST_H_OFFSET[7:0]	BIST mode H_width offset.	
19h	0Fh	R/W	[7]	-	Reserved.	
		R/W	[6]	BIST_OSC_SEL_EN	Oscillator frequency selection for BIST.	
		R/W	[5:0]	H_OSCLK_SEL[5:0]	Oscillator selection for BIST mode.	
1Bh	32h	R/W	[7:0]	-	Reserved.	Group 5 **(2 times)**
1Ch	00h	R/W	[7:4]	POL_INV_FRM[3:0]	Polarity change sequence method selection.	
		R/W	[3]	EQ0_MODE	EQ0 mode selection.	
		R/W	[2]	-	Reserved.	
		R/W	[1:0]	PRE_SCAN[1:0]	Tradition Gate driver pre-scan mode selection.	
1Dh	80h	R/W	[7:0]	BIST_GRAY[7:0]	BIST mode gray scale pattern setting.	
1Eh	80h	R/W	[7:0]	DMY_DATA[7:0]	Source dummy data select for Zig-Zag type panel.	

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8.1.2. Register table: Page01h (Power control function setting)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	0Ch	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	3Ah	R/W	[7]	-	Reserved.	Group 6 **(2 times)**
		R/W	[6]	PFMFREN	PFM frequency randomizer.	
		R/W	[5]	VSPEN	VSP enable.	
		R/W	[4]	VSNEN	VSN enable.	
		R/W	[3:2]	DRVPD[1:0]	DRVP buffer size selection.	
		R/W	[1:0]	DRVND[1:0]	DRVN buffer size selection.	
02h	94h	R/W	[7:6]	VMONPS[1:0]	VSP over current protect selection.	
		R/W	[5]	OCPEN	PFM over current detect enable.	
		R/W	[4:0]	VSPS[4:0]	VSP voltage selection.	
03h	94h	R/W	[7:6]	VMONNS[1:0]	VSN over current protect selection.	
		R/W	[5]	VCOM_OTP	VCOMS setting selection.	
		R/W	[4:0]	VSNS[4:0]	VSN voltage selection.	
04h	1Ch	R/W	[7]	-	Reserved.	
		R/W	[6:0]	VGHS[6:0]	VGH voltage selection.	
05h	0Ch	R/W	[7]	-	Reserved.	
		R/W	[6]	VGLXS	VGL boosting mode selection.	
		R/W	[5:0]	VGLS[5:0]	VGL voltage selection.	
06h	14h	R/W	[7]	VSPON[4]	Pulse width of high state of DRVP.	
		R/W	[6]	VSNON[4]	Pulse width of high state of DRVN.	
		R/W	[5]	POFF_GAS_EN	XAO active during power off function disable.	
		R/W	[4:0]	VSDPS[4:0]	Select VSDP level.	
07h	D4h	R/W	[7]	-	Reserved.	
		R/W	[6]	-	Reserved.	
		R/W	[5]	CAS_VGHL_OPT	VGH/VGL power on sequence delay between slave and master.	
		R/W	[4:0]	VSDNS[4:0]	Select VSDN level.	
08h	55h	R/W	[3:0]	VSPON[3:0]	PFM turn on duty of DRVP.	
		R/W	[3:0]	VSPOFF[3:0]	PFM turn off duty of DRVP.	
09h	55h	R/W	[3:0]	VSNON[3:0]	PFM turn on duty of DRVN.	
		R/W	[3:0]	VSNOFF[3:0]	PFM turn off duty of DRVN.	
0Ah	4Fh	R/W	[3:0]	VSPON_SS2[3:0]	PFM turn on duty of DRVP at soft start of power on sequence.	
		R/W	[3:0]	VSPOFF_SS2[3:0]	PFM turn off duty of DRVP at soft start of power on sequence.	
0Bh	8Ah	R/W	[3:0]	VSNON_SS2[3:0]	PFM turn on duty of DRVN at soft start of power on sequence.	
		R/W	[3:0]	VSNOFF_SS2[3:0]	PFM turn off duty of DRVN at soft start of power on sequence.	
0Ch	B1h	R/W	[7]	GAS_VCC_EN	GAS detector VCI level selection.	
		R/W	[6:5]	VGHXS[1:0]	Select VGH boosting mode.	
		R/W	[4]	VCOMEN	Enable VCOM regulator.	
		R/W	[3]	S_VCL_ENB	Slave chip VCL regulator enable.	
		R/W	[2]	M_VCL_ENB	Master chip VCL regulator enable.	
		R/W	[1:0]	VCOMD[1:0]	Select VCOM driving capability.	
0Dh	E3h	R/W	[7]	VGHL_LIMIT	Auto setting for (VGH + |VGL| < 32).	
		R/W	[6]	VGHEN	VGH charge pump circuit enable.	
		R/W	[5]	VGLEN	VGL charge pump circuit enable.	
		R/W	[4]	-	Reserved.	
		R/W	[3]	PFM_SS_SEL	PFM soft start duration selection.	
		R/W	[2]	POL_TOG_VBLK	POL keep toggle at vertical blanking.	
		R/W	[1:0]	FCP[1:0]	VGH and VGL charge pump frequency setting.	
0Eh	FAh	R/W	[7]	GAS_VGL_EN	GAS detector VGL level select.	
		R/W	[6]	SCPEN	Enable SCP detector.	
		R/W	[5]	VGMREGEN	VGMPH/M/LO, VGMNH/M/LO regulators enable signal.	
		R/W	[4:0]	VGMPHS[4:0]	select VGMPHO level.	
0Fh	5Ah	R/W	[7:5]	GASVCIS[2:0]	VCI GAS voltage.	
		R/W	[4:0]	VGMNHS[4:0]	Select VGMNHO level.	
10h	11h	R/W	[3:0]	VGMPLS[3:0]	Select VGMPLO level.	

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Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
		R/W	[3:0]	VGMNLS[3:0]	Select VGMNLO level.	
11h	AAh	R/W	[7:6]	DCHG2R[1:0]	VGH2 dis-charge resistance selection.	
		R/W	[5:4]	DCHG2ON[1:0]	Enable DCHG2R function in normal off and GAS off.	
		R/W	[3:2]	DCHG1R[1:0]	VGH1 dis-charge resistance selection.	
		R/W	[1:0]	DCHG1ON[1:0]	Enable DCHG1R function in normal off and GAS off.	
12h	54h	R/W	[7]	POFF_BLACK_OPT	Power off 2 black frames.	
		R/W	[6]	POFF_BLACK_NUM	Power off black frame numbers: 0/1 frame.	
		R/W	[5:4]	PON_BLACK_NUM[1:0]	Power on black frame numbers: 0/1/2 frames.	
		R/W	[3]	HT_POL_OPT	POL inversion change at HT.	
		R/W	[2:0]	VCLS[2:0]	Select VCL level, **(range: -2.125V ~ -3V)** default=-2.75V.	
13h	00h	R/W	[7]	GD_OEV_OFF	Tradition Gate OEV keep Low.	
		R/W	[6]	-	Reserved.	
		R/W	[5]	LTPS_GIP_PWR_OPT	GIP power on keep VGL.	
		R/W	[4]	LOAD_OPT	Panel Loading option.	
		R/W	[3:2]	-	Reserved.	
		R/W	[1:0]	TFVBAT1[1:0]	Abnormal off sequence, GIP VGH1 output setting period.	
14h	1Fh	R/W	[3:0]	VSPON_SS1[3:0]	PFM turn on duty of DRVP at soft start of power on sequence.	
		R/W	[3:0]	VSPOFF_SS1[3:0]	PFM turn off duty of DRVP at soft start of power on sequence.	
15h	2Fh	R/W	[3:0]	VSNON_SS1[3:0]	PFM turn on duty of DRVN at soft start of power on sequence.	
		R/W	[3:0]	VSNOFF_SS1[3:0]	PFM turn off duty of DRVN at soft start of power on sequence.	
16h	05h	R/W	[7:0]	-	Reserved.	
17h	00h	R/W	[7:0]	-	Reserved.	
18h	FFh	R/W	[7:0]	PTSEL[15:8]	BIST pattern selection.	
19h	FFh	R/W	[7:0]	PTSEL[7:0]	BIST pattern selection.	
1Ah	01h	R/W	[7:1]	-	Reserved.	Group 7 **(3 times)**
		R/W	[0]	OFF_VCOM[8]	Panel off sequence, VCOMDC voltage setting.	
1Bh	5Ch	R/W	[7:0]	OFF_VCOM[7:0]	Panel off sequence, VCOMDC voltage setting.	
1Ch	00h	R/W	[7:0]	VCOM_OFST[7:0]	VCOM of first frame for pol_inv_frame feature.	
1Dh	01h	R/W	[7:1]	-	Reserved.	Group 8 **(10 times)**
		R/W	[0]	VCOMS[8]	Select VCOM level.	
1Eh	5Ch	R/W	[7:0]	VCOMS[7:0]	Select VCOM level.	

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8.1.3. Register table: Page02h (Positive analog gamma, PAGM)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	0Ch	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7:5]	-	Reserved.	Group 9 **(3 times)**
		R/W	[4:0]	T_VP0[4:0]	Positive gamma reference GSH0 selection.	
02h	04h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP2[5:0]	Positive gamma reference GSH2 selection.	
03h	08h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP4[5:0]	Positive gamma reference GSH4 selection.	
4h	18h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP8[5:0]	Positive gamma reference GSH8 selection.	
5h	23h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP14[5:0]	Positive gamma reference GSH14 selection.	
6h	12h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP22[5:0]	Positive gamma reference GSH22 selection.	
7h	11h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP30[5:0]	Positive gamma reference GSH30 selection.	
8h	17h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP47[5:0]	Positive gamma reference GSH47 selection.	
9h	20h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP79[5:0]	Positive gamma reference GSH79 selection.	
0Ah	23h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP111[5:0]	Positive gamma reference GSH113 selection.	
0Bh	26h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP143[5:0]	Positive gamma reference GSH143 selection.	
0Ch	2Bh	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP175[5:0]	Positive gamma reference GSH175 selection.	
0Dh	25h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP207[5:0]	Positive gamma reference GSH207 selection.	
0Eh	25h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP224[5:0]	Positive gamma reference GSH224 selection.	
0Fh	35h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP232[5:0]	Positive gamma reference GSH232 selection.	
10h	30h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP240[5:0]	Positive gamma reference GSH240 selection.	
11h	24h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP246[5:0]	Positive gamma reference GSH246 selection.	
12h	31h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP251[5:0]	Positive gamma reference GSH251 selection.	
13h	38h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VP253[5:0]	Positive gamma reference GSH253 selection.	
14h	1Eh	R/W	[7:5]	-	Reserved.	
		R/W	[4:0]	T_VP255[4:0]	Positive gamma reference GSH255 selection.	
15h	00h	R/W	[7:0]	P_checksum[7:0]	SUM[R01:R14] **(only for OTP)**.	

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8.1.4. Register table: Page03h (Negative analog gamma, NAGM)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	0Ch	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7:5]	-	Reserved.	Group 10 **(3 times)**
		R/W	[4:0]	T_VN0[4:0]	Positive gamma reference GSL0 selection.	
02h	04h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN2[5:0]	Positive gamma reference GSL2 selection.	
03h	08h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN4[5:0]	Positive gamma reference GSL4 selection.	
4h	18h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN8[5:0]	Positive gamma reference GSL8 selection.	
5h	23h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN14[5:0]	Positive gamma reference GSL14 selection.	
6h	12h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN22[5:0]	Positive gamma reference GSL22 selection.	
7h	11h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN30[5:0]	Positive gamma reference GSL30 selection.	
8h	17h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN47[5:0]	Positive gamma reference GSL47 selection.	
9h	20h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN79[5:0]	Positive gamma reference GSL79 selection.	
0Ah	23h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN111[5:0]	Positive gamma reference GSL113 selection.	
0Bh	26h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN143[5:0]	Positive gamma reference GSL143 selection.	
0Ch	2Bh	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN175[5:0]	Positive gamma reference GSL175 selection.	
0Dh	25h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN207[5:0]	Positive gamma reference GSL207 selection.	
0Eh	25h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN224[5:0]	Positive gamma reference GSL224 selection.	
0Fh	35h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN232[5:0]	Positive gamma reference GSL232 selection.	
10h	30h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN240[5:0]	Positive gamma reference GSL240 selection.	
11h	24h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN246[5:0]	Positive gamma reference GSL246 selection.	
12h	31h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN251[5:0]	Positive gamma reference GSL251 selection.	
13h	38h	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	T_VN253[5:0]	Positive gamma reference GSL253 selection.	
14h	1Eh	R/W	[7:5]	-	Reserved.	
		R/W	[4:0]	T_VN255[4:0]	Positive gamma reference GSL255 selection.	
15h	00h	R/W	[7:0]	N_checksum[7:0]	SUM[R01:R14] **(only for OTP)**.	

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8.1.5. Register table: Page04h (Fail flag function setting)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	0Ch	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	84h	R/W	[7]	FAIL_DET_SEL	FAIL_DET output selection.	Group 11 **(2 times)**
		R/W	[6]	FAIL_DET_INV	FAIL_DET output inverse.	
		R/W	[5]	ASIL_PRIOR_SEL	ASIL priority selection.	
		R/W	[4]	ASIL_NOSIG_SEL	ASIL detect function selection.	
		R/W	[3]	ASIL_INV	ASIL output signal inverse.	
		R/W	[2:0]	ASIL_WD[2:0]	ASIL output pulse width selection.	
02h	3fh	R/W	[7:6]	-	Reserved.	
		R/W	[5]	SD_DET_EN	Source_R/L block self detect function enable.	
		R/W	[4]	PON_FDET_EN	Power on fail detect test enable.	
		R/W	[3]	CRC4_FAIL_ENB	CRC4 windows4 fail flag enable.	
		R/W	[2]	CRC3_FAIL_ENB	CRC3 windows3 fail flag enable.	
		R/W	[1]	CRC2_FAIL_ENB	CRC2 windows2 fail flag enable.	
		R/W	[0]	CRC1_FAIL_ENB	CRC1 windows1 fail flag enable.	
03h	00h	R/W	[7]	PFM_NG_ENB	PFM NG fail flag enable.	
		R/W	[6]	OTP_TRIM_FAIL_ENB	OTP program fail flag enable.	
		R/W	[5]	EEPROM_FAIL_ENB	EEPROM reload fail flag enable.	
		R/W	[4]	NOVIDEO_FAIL_ENB	No vedio ail mode fail flag enable.	
		R/W	[3]	GATE_FAIL_ENB	Tradition gate signal fail flag enable.	
		R/W	[2]	SOURCE_FAIL_ENB	Internal source circuit fail flag enable.	
		R/W	[1]	OTP_FULL_FAIL_ENB	GAS function fail flag enable.	
		R/W	[0]	LVDS_FAIL_ENB	LVDS lock fail flag enable.	
04h	9Dh	R/W	[7]	GAS_VGL_ENB	Low VGL signal to fail_flag enable.	
		R/W	[6]	GAS_PFM_FAIL_ENB	Low VSP/VSN signal to fail flag enable.	
		R/W	[5]	GAS_VCC_FAIL_ENB	Low VCC signal to fail flag enable.	
		R/W	[4]	SLV_VCOM_DET_ENB	Slave VCOM fail_detect enable.	
		R/W	[3]	OTP_CKSUM_FAIL2_ENB	OTP P/N gamma table checksum fail flag to FAIL_DET pin enable.	
		R/W	[2]	OTP_CHKSUM_FAIL_ENB	OTP table checksum fail flag to FAIL_DET pin enable.	
		R/W	[1]	OTP_RL_FAIL_ENB	OTP reload fail_flag to FAIL_DET pin enable.	
		R/W	[0]	SLV_GAM_DET_ENB	Slave VGM fail_detect enable.	
05h	00h	R/W	[7]	OVP_VCC_ENB	VCC detect and output to fail_flag enable.	
		R/W	[6]	OVP_VSP_ENB	VSP detect and output to fail_flag enable.	
		R/W	[5]	OVP_VSN_ENB	VSN detect and output to fail_flag enable.	
		R/W	[4]	OVP_VGH_ENB	VGH detect and output to fail_flag enable.	
		R/W	[3]	OVP_VGL_ENB	VGL detect and output to fail_flag enable.	
		R/W	[2]	OVP_VCOM_ENB	VCOM detect and output to fail_flag enable.	
		R/W	[1]	LVD_VGH_ENB	Low VGH detect and output to fail_flag enable.	
		R/W	[0]	LVD_VCOM_ENB	Low VCOM detect and output to fail_flag enable.	
06h	00h	R/W	[7]	OVP_VGMPL_ENB	VGMPL detect and output to fail_flag enable.	
		R/W	[6]	OVP_VGMNL_ENB	VGMNL detect and output to fail_flag enable.	
		R/W	[5]	OVP_VDDD_ENB	VDDD detect and output to fail_flag enable.	
		R/W	[4]	OVP_VCL_ENB	VCL detect and output to fail_flag enable.	
		R/W	[3]	LVD_VGMPH_ENB	Low VGMPH detect and output to fail_flag enable.	
		R/W	[2]	LVD_VGMNH_ENB	Low VGMNH detect and output to fail_flag enable.	
		R/W	[1]	LVD_VSDPN_ENB	Low VSDP/VSDN detect and output to fail_flag enable.	
		R/W	[0]	LVD_VCL_ENB	Low VCL detect and output to fail_flag enable.	
07h	08h	R/W	[7:4]	-	Reserved.	
		R/W	[3]	PFM_NG_ACT	Behavior of PFM NG fail selection.	
		R/W	[2]	OTP_TRIM_FAIL_ACT	Behavior of OTP_TRIM fail selection.	
		R/W	[1]	EEPROM_OTP_FAIL_ACT	Behavior of EEPROM_OTP fail selection.	
		R/W	[0]	GATE_SD_FAIL_ACT	Behavior of GATE_SD fail selection.	
08h	0Ah	R/W	[7:6]	CRC_FAIL_ACT[1:0]	Behavior of CRC fail selection.	
		R/W	[5:4]	GAS_VGL_FAIL_ACT[1:0]	Behavior of GAS_VGL fail selection.	
		R/W	[3:2]	GAS_PFM_FAIL_ACT[1:0]	Behavior of GAS_PFM fail selection.	
		R/W	[1:0]	GAS_VCC_FAIL_ACT[1:0]	Behavior of GAS_VCC fail selection.	

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Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
09h	00h	R/W	[7:5]	-	Reserved.	
		R/W	[4]	VGMA_PWR_NG_ACT	Behavior of GMA related voltage fail selection.	
		R/W	[3]	VCOM_NG_ACT	Behavior of VCOM voltage fail selection.	
		R/W	[2]	OVP_PWR_ACT	Behavior of DC/DC voltage over fail selection.	
		R/W	[1]	LVD_PWR_ACT	Behavior of VGH/VSDN voltage low fail selection.	
		R/W	[0]	LVD_VCL_ACT	Behavior of VCL voltage low fail selection.	
0Ah	00h	R/W	[7:0]	-	Reserved.	
0Bh	D0h	R/W	[7]	PFM_DET_EN	PFM_NG detect enable.	
		R/W	[6]	PFM_DET_OPT	PFM_NG fail-detect time selection.	
		R/W	[5]	PFM_REDET_OPT	PFM stop time after PFM_NG fail-detect trigger.	
		R/W	[4]	DPFM_OSC_SEL	DPFM clock frequency selection.	
		R/W	[3:0]	-	Reserved.	
0Ch	00h	R/W	[7]	CROSS_TALK_GRAY	BIST cross_talk_gray selection.	
		R/W	[6]	FLICK_GRAY	BIST flick_gray selection.	
		R/W	[5:4]	GIP_MX_TAB_SEL[1:0]	GIP MUX table selection.	
		R/W	[3]	-	Reserved.	
		R/W	[2]	GAS_OTP_SELB	Exit gas need do otp /eeprom reload.	
		R/W	[1]	RESET_SLP_OPT	RESET_SLP active.	
		R/W	[0]	ZZS_FORCE_POL_ENB	Zigzag panel inversion selection.	
0Dh	F0h	R/W	[7:6]	ENDRVN[1:0]	Negative polarity, channel OP PMOS driving ability control signal.	
		R/W	[5:4]	ENDRVP[1:0]	Positive polarity, channel OP PMOS driving ability control signal.	
		R/W	[3:0]	-	Reserved.	
0Eh	FFh	R/W	[7:0]	PON_FAIL_EN1[7:0]	Power on fail test enable.	
0Fh	0Fh	R/W	[7:0]	PON_FAIL_EN2[7:0]	Power on fail test enable.	
10h	40h	R/W	[7:0]	TP_DLY[7:0]	set HS falling to TP_SYNC rising period, range: (1~256)*4 **(unit: SD_CLK_SEL)**.	
11h	40h	R/W	[7:0]	TP_WIDTH[7:0]	set TP_SYNC H_width, range: (1~256)*4 **(unit: SD_CLK_SEL)**.	
12h	6eh	R/W	[7]	TP_SYNC_INV	TPSYNC output inverse.	
		R/W	[6:4]	TP_SYNC1_SEL[2:0]	TPSYNC1 output selection.	
		R/W	[3]	TP_WIDTH_ENB	TPSYNC output enable when SD driving.	
		R/W	[2:0]	TP_SYNC2_SEL[2:0]	TPSYNC2 output selection.	
13h	57h	R/W	[7:6]	GIP_RL_EN_S3[1:0]	GIP R/L pin enable for SID[1:0]=HH **(Slave3)**.	
		R/W	[5:4]	GIP_RL_EN_S2[1:0]	GIP R/L pin enable for SID[1:0]=HL **(Slave2)**.	
		R/W	[3:2]	GIP_RL_EN_S1[1:0]	GIP R/L pin enable for SID[1:0]=LH **(Slave1)**.	
		R/W	[1:0]	GIP_RL_EN_M[1:0]	GIP R/L pin enable for SID[1:0]=LL **(master)**.	
14h	00h	R/W	[7:4]	L_GIP_VGH_SEL[19:16]	Left side GIP PIN VGH power select for GAS state.	
		R/W	[3:0]	R_GIP_VGH_SEL[19:16]	Right side GIP PIN VGH power select for GAS state.	
15h	00h	R/W	[7:0]	L_GIP_VGH_SEL[15:8]	Left side GIP PIN VGH power select for GAS state.	
16h	00h	R/W	[7:0]	L_GIP_VGH_SEL[7:0]	Left side GIP PIN VGH power select for GAS state.	
17h	00h	R/W	[7:0]	R_GIP_VGH_SEL[15:8]	Right side GIP PIN VGH power select for GAS state.	
18h	00h	R/W	[7:0]	R_GIP_VGH_SEL[7:0]	Right side GIP PIN VGH power select for GAS state.	

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8.1.6. Register table: Page05h (GIP function)

Please refer to application note for GIP function.
(OTP group 12, and can be programmed 2 times.)

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8.1.7. Register table: Page06h (Digital gamma correction for Red color)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7:0]	DGMA1R[7:0]	Digital gamma reference Y1[7:0]: Red.	Group 13 **(1 time)**
02h	04h	R/W	[7:0]	DGMA2R[7:0]	Digital gamma reference Y2[7:0]: Red.	
03h	0Ch	R/W	[7:0]	DGMA3R[7:0]	Digital gamma reference Y3[7:0]: Red.	
04h	1Ch	R/W	[7:0]	DGMA4R[7:0]	Digital gamma reference Y4[7:0]: Red.	
05h	2Ch	R/W	[7:0]	DGMA5R[7:0]	Digital gamma reference Y5[7:0]: Red.	
06h	3Ch	R/W	[7:0]	DGMA6R[7:0]	Digital gamma reference Y6[7:0]: Red.	
07h	5Ch	R/W	[7:0]	DGMA7R[7:0]	Digital gamma reference Y7[7:0]: Red.	
08h	7Ch	R/W	[7:0]	DGMA8R[7:0]	Digital gamma reference Y8[7:0]: Red.	
09h	BCh	R/W	[7:0]	DGMA9R[7:0]	Digital gamma reference Y9[7:0]: Red.	
0Ah	FCh	R/W	[7:0]	DGMA10R[7:0]	Digital gamma reference Y10[7:0]: Red.	
0Bh	7Ch	R/W	[7:0]	DGMA11R[7:0]	Digital gamma reference Y11[7:0]: Red.	
0Ch	FCh	R/W	[7:0]	DGMA12R[7:0]	Digital gamma reference Y12[7:0]: Red.	
0Dh	00h	R/W	[7:0]	DGMA13R[7:0]	Digital gamma reference Y13[7:0]: Red.	
0Eh	80h	R/W	[7:0]	DGMA14R[7:0]	Digital gamma reference Y14[7:0]: Red.	
0Fh	00h	R/W	[7:0]	DGMA15R[7:0]	Digital gamma reference Y15[7:0]: Red.	
10h	40h	R/W	[7:0]	DGMA16R[7:0]	Digital gamma reference Y16[7:0]: Red.	
11h	80h	R/W	[7:0]	DGMA17R[7:0]	Digital gamma reference Y17[7:0]: Red.	
12h	A0h	R/W	[7:0]	DGMA18R[7:0]	Digital gamma reference Y18[7:0]: Red.	
13h	C0h	R/W	[7:0]	DGMA19R[7:0]	Digital gamma reference Y19[7:0]: Red.	
14h	D0h	R/W	[7:0]	DGMA20R[7:0]	Digital gamma reference Y20[7:0]: Red.	
15h	E0h	R/W	[7:0]	DGMA21R[7:0]	Digital gamma reference Y21[7:0]: Red.	
16h	F0h	R/W	[7:0]	DGMA22R[7:0]	Digital gamma reference Y22[7:0]: Red.	
17h	F8h	R/W	[7:0]	DGMA23R[7:0]	Digital gamma reference Y23[7:0]: Red.	
18h	FCh	R/W	[7:0]	DGMA24R[7:0]	Digital gamma reference Y24[7:0]: Red.	
19h	00h	R/W	[7:6]	DGMA1R[9:8]	Digital gamma reference Y1[9:8]: Red.	
			[5:4]	DGMA2R[9:8]	Digital gamma reference Y2[9:8]: Red.	
			[3:2]	DGMA3R[9:8]	Digital gamma reference Y3[9:8]: Red.	
			[1:0]	DGMA4R[9:8]	Digital gamma reference Y4[9:8]: Red.	
1Ah	00h	R/W	[7:6]	DGMA5R[9:8]	Digital gamma reference Y5[9:8]: Red.	
			[5:4]	DGMA6R[9:8]	Digital gamma reference Y6[9:8]: Red.	
			[3:2]	DGMA7R[9:8]	Digital gamma reference Y7[9:8]: Red.	
			[1:0]	DGMA8R[9:8]	Digital gamma reference Y8[9:8]: Red.	
1Bh	05h	R/W	[7:6]	DGMA9R[9:8]	Digital gamma reference Y9[9:8]: Red.	
			[5:4]	DGMA10R[9:8]	Digital gamma reference Y10[9:8]: Red.	
			[3:2]	DGMA11R[9:8]	Digital gamma reference Y11[9:8]: Red.	
			[1:0]	DGMA12R[9:8]	Digital gamma reference Y12[9:8]: Red.	
1Ch	AFh	R/W	[7:6]	DGMA13R[9:8]	Digital gamma reference Y13[9:8]: Red.	
			[5:4]	DGMA14R[9:8]	Digital gamma reference Y14[9:8]: Red.	
			[3:2]	DGMA15R[9:8]	Digital gamma reference Y15[9:8]: Red.	
			[1:0]	DGMA16R[9:8]	Digital gamma reference Y16[9:8]: Red.	
1Dh	FFh	R/W	[7:6]	DGMA17R[9:8]	Digital gamma reference Y17[9:8]: Red.	
			[5:4]	DGMA18R[9:8]	Digital gamma reference Y18[9:8]: Red.	
			[3:2]	DGMA19R[9:8]	Digital gamma reference Y19[9:8]: Red.	
			[1:0]	DGMA20R[9:8]	Digital gamma reference Y20[9:8]: Red.	
1Eh	FFh	R/W	[7:6]	DGMA21R[9:8]	Digital gamma reference Y21[9:8]: Red.	
			[5:4]	DGMA22R[9:8]	Digital gamma reference Y22[9:8]: Red.	
			[3:2]	DGMA23R[9:8]	Digital gamma reference Y23[9:8]: Red.	
			[1:0]	DGMA24R[9:8]	Digital gamma reference Y24[9:8]: Red.	

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8.1.8. Register table: Page07h (Digital gamma correction for Green color)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7:0]	DGMA1G[7:0]	Digital gamma reference Y1[7:0]: Green.	Group 14 (1 time)
02h	04h	R/W	[7:0]	DGMA2G[7:0]	Digital gamma reference Y2[7:0]: Green.	
03h	0Ch	R/W	[7:0]	DGMA3G[7:0]	Digital gamma reference Y3[7:0]: Green.	
04h	1Ch	R/W	[7:0]	DGMA4G[7:0]	Digital gamma reference Y4[7:0]: Green.	
05h	2Ch	R/W	[7:0]	DGMA5G[7:0]	Digital gamma reference Y5[7:0]: Green.	
06h	3Ch	R/W	[7:0]	DGMA6G[7:0]	Digital gamma reference Y6[7:0]: Green.	
07h	5Ch	R/W	[7:0]	DGMA7G[7:0]	Digital gamma reference Y7[7:0]: Green.	
08h	7Ch	R/W	[7:0]	DGMA8G[7:0]	Digital gamma reference Y8[7:0]: Green.	
09h	BCh	R/W	[7:0]	DGMA9G[7:0]	Digital gamma reference Y9[7:0]: Green.	
0Ah	FCh	R/W	[7:0]	DGMA10G[7:0]	Digital gamma reference Y10[7:0]: Green.	
0Bh	7Ch	R/W	[7:0]	DGMA11G[7:0]	Digital gamma reference Y11[7:0]: Green.	
0Ch	FCh	R/W	[7:0]	DGMA12G[7:0]	Digital gamma reference Y12[7:0]: Green.	
0Dh	00h	R/W	[7:0]	DGMA13G[7:0]	Digital gamma reference Y13[7:0]: Green	
0Eh	80h	R/W	[7:0]	DGMA14G[7:0]	Digital gamma reference Y14[7:0]: Green.	
0Fh	00h	R/W	[7:0]	DGMA15G[7:0]	Digital gamma reference Y15[7:0]: Green.	
10h	40h	R/W	[7:0]	DGMA16G[7:0]	Digital gamma reference Y16[7:0]: Green	
11h	80h	R/W	[7:0]	DGMA17G[7:0]	Digital gamma reference Y17[7:0]: Green.	
12h	A0h	R/W	[7:0]	DGMA18G[7:0]	Digital gamma reference Y18[7:0]: Green.	
13h	C0h	R/W	[7:0]	DGMA19G[7:0]	Digital gamma reference Y19[7:0]: Green.	
14h	D0h	R/W	[7:0]	DGMA20G[7:0]	Digital gamma reference Y20[7:0]: Green.	
15h	E0h	R/W	[7:0]	DGMA21G[7:0]	Digital gamma reference Y21[7:0]: Green.	
16h	F0h	R/W	[7:0]	DGMA22G[7:0]	Digital gamma reference Y22[7:0]: Green.	
17h	F8h	R/W	[7:0]	DGMA23G[7:0]	Digital gamma reference Y23[7:0]: Green.	
18h	FCh	R/W	[7:0]	DGMA24G[7:0]	Digital gamma reference Y24[7:0]: Green.	
19h	00h	R/W	[7:6]	DGMA1G[9:8]	Digital gamma reference Y1[9:8]: Green.	
			[5:4]	DGMA2G[9:8]	Digital gamma reference Y2[9:8]: Green.	
			[3:2]	DGMA3G[9:8]	Digital gamma reference Y3[9:8]: Green.	
			[1:0]	DGMA4G[9:8]	Digital gamma reference Y4[9:8]: Green.	
1Ah	00h	R/W	[7:6]	DGMA5G[9:8]	Digital gamma reference Y5[9:8]: Green.	
			[5:4]	DGMA6G[9:8]	Digital gamma reference Y6[9:8]: Green.	
			[3:2]	DGMA7G[9:8]	Digital gamma reference Y7[9:8]: Green.	
			[1:0]	DGMA8G[9:8]	Digital gamma reference Y8[9:8]: Green.	
1Bh	05h	R/W	[7:6]	DGMA9G[9:8]	Digital gamma reference Y9[9:8]: Green.	
			[5:4]	DGMA10G[9:8]	Digital gamma reference Y10[9:8]: Green.	
			[3:2]	DGMA11G[9:8]	Digital gamma reference Y11[9:8]: Green.	
			[1:0]	DGMA12G[9:8]	Digital gamma reference Y12[9:8]: Green.	
1Ch	AFh	R/W	[7:6]	DGMA13G[9:8]	Digital gamma reference Y13[9:8]: Green.	
			[5:4]	DGMA14G[9:8]	Digital gamma reference Y14[9:8]: Green.	
			[3:2]	DGMA15G[9:8]	Digital gamma reference Y15[9:8]: Green.	
			[1:0]	DGMA16G[9:8]	Digital gamma reference Y16[9:8]: Green.	
1Dh	FFh	R/W	[7:6]	DGMA17G[9:8]	Digital gamma reference Y17[9:8]: Green.	
			[5:4]	DGMA18G[9:8]	Digital gamma reference Y18[9:8]: Green.	
			[3:2]	DGMA19G[9:8]	Digital gamma reference Y19[9:8]: Green.	
			[1:0]	DGMA20G[9:8]	Digital gamma reference Y20[9:8]: Green.	
1Eh	FFh	R/W	[7:6]	DGMA21G[9:8]	Digital gamma reference Y21[9:8]: Green.	
			[5:4]	DGMA22G[9:8]	Digital gamma reference Y22[9:8]: Green.	
			[3:2]	DGMA23G[9:8]	Digital gamma reference Y23[9:8]: Green.	
			[1:0]	DGMA24G[9:8]	Digital gamma reference Y24[9:8]: Green.	

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8.1.9. Register table: Page08h (Digital gamma correction for Blue color)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group
00h	1Bh	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7:0]	DGMA1B[7:0]	Digital gamma reference Y1[7:0]: Blue.	Group 15 **(1 time)**
02h	04h	R/W	[7:0]	DGMA2B[7:0]	Digital gamma reference Y2[7:0]: Blue.	
03h	0Ch	R/W	[7:0]	DGMA3B[7:0]	Digital gamma reference Y3[7:0]: Blue.	
04h	1Ch	R/W	[7:0]	DGMA4B[7:0]	Digital gamma reference Y4[7:0]: Blue.	
05h	2Ch	R/W	[7:0]	DGMA5B[7:0]	Digital gamma reference Y5[7:0]: Blue.	
06h	3Ch	R/W	[7:0]	DGMA6B[7:0]	Digital gamma reference Y6[7:0]: Blue.	
07h	5Ch	R/W	[7:0]	DGMA7B[7:0]	Digital gamma reference Y7[7:0]: Blue.	
08h	7Ch	R/W	[7:0]	DGMA8B[7:0]	Digital gamma reference Y8[7:0]: Blue.	
09h	BCh	R/W	[7:0]	DGMA9B[7:0]	Digital gamma reference Y9[7:0]: Blue.	
0Ah	FCh	R/W	[7:0]	DGMA10B[7:0]	Digital gamma reference Y10[7:0]: Blue.	
0Bh	7Ch	R/W	[7:0]	DGMA11B[7:0]	Digital gamma reference Y11[7:0]: Blue.	
0Ch	FCh	R/W	[7:0]	DGMA12B[7:0]	Digital gamma reference Y12[7:0]: Blue.	
0Dh	00h	R/W	[7:0]	DGMA13B[7:0]	Digital gamma reference Y13[7:0]: Blue.	
0Eh	80h	R/W	[7:0]	DGMA14B[7:0]	Digital gamma reference Y14[7:0]: Blue.	
0Fh	00h	R/W	[7:0]	DGMA15B[7:0]	Digital gamma reference Y15[7:0]: Blue	
10h	40h	R/W	[7:0]	DGMA16B[7:0]	Digital gamma reference Y16[7:0]: Blue.	
11h	80h	R/W	[7:0]	DGMA17B[7:0]	Digital gamma reference Y17[7:0]: Blue.	
12h	A0h	R/W	[7:0]	DGMA18B[7:0]	Digital gamma reference Y18[7:0]: Blue.	
13h	C0h	R/W	[7:0]	DGMA19B[7:0]	Digital gamma reference Y19[7:0]: Blue.	
14h	D0h	R/W	[7:0]	DGMA20B[7:0]	Digital gamma reference Y20[7:0]: Blue.	
15h	E0h	R/W	[7:0]	DGMA21B[7:0]	Digital gamma reference Y21[7:0]: Blue.	
16h	F0h	R/W	[7:0]	DGMA22B[7:0]	Digital gamma reference Y22[7:0]: Blue.	
17h	F8h	R/W	[7:0]	DGMA23B[7:0]	Digital gamma reference Y23[7:0]: Blue.	
18h	FCh	R/W	[7:0]	DGMA24B[7:0]	Digital gamma reference Y24[7:0]: Blue.	
19h	00h	R/W	[7:6]	DGMA1B[9:8]	Digital gamma reference Y1[9:8]: Blue.	
			[5:4]	DGMA2B[9:8]	Digital gamma reference Y2[9:8]: Blue.	
			[3:2]	DGMA3B[9:8]	Digital gamma reference Y3[9:8]: Blue.	
			[1:0]	DGMA4B[9:8]	Digital gamma reference Y4[9:8]: Blue.	
1Ah	00h	R/W	[7:6]	DGMA5B[9:8]	Digital gamma reference Y5[9:8]: Blue.	
			[5:4]	DGMA6B[9:8]	Digital gamma reference Y6[9:8]: Blue.	
			[3:2]	DGMA7B[9:8]	Digital gamma reference Y7[9:8]: Blue.	
			[1:0]	DGMA8B[9:8]	Digital gamma reference Y8[9:8]: Blue.	
1Bh	05h	R/W	[7:6]	DGMA9B[9:8]	Digital gamma reference Y9[9:8]: Blue.	
			[5:4]	DGMA10B[9:8]	Digital gamma reference Y10[9:8]: Blue.	
			[3:2]	DGMA11B[9:8]	Digital gamma reference Y11[9:8]: Blue.	
			[1:0]	DGMA12B[9:8]	Digital gamma reference Y12[9:8]: Blue.	
1Ch	AFh	R/W	[7:6]	DGMA13B[9:8]	Digital gamma reference Y13[9:8]: Blue.	
			[5:4]	DGMA14B[9:8]	Digital gamma reference Y14[9:8]: Blue.	
			[3:2]	DGMA15B[9:8]	Digital gamma reference Y15[9:8]: Blue.	
			[1:0]	DGMA16B[9:8]	Digital gamma reference Y16[9:8]: Blue.	
1Dh	FFh	R/W	[7:6]	DGMA17B[9:8]	Digital gamma reference Y17[9:8]: Blue.	
			[5:4]	DGMA18B[9:8]	Digital gamma reference Y18[9:8]: Blue.	
			[3:2]	DGMA19B[9:8]	Digital gamma reference Y19[9:8]: Blue.	
			[1:0]	DGMA20B[9:8]	Digital gamma reference Y20[9:8]: Blue.	
1Eh	FFh	R/W	[7:6]	DGMA21B[9:8]	Digital gamma reference Y21[9:8]: Blue.	
			[5:4]	DGMA22B[9:8]	Digital gamma reference Y22[9:8]: Blue.	
			[3:2]	DGMA23B[9:8]	Digital gamma reference Y23[9:8]: Blue.	
			[1:0]	DGMA24B[9:8]	Digital gamma reference Y24[9:8]: Blue.	

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8.1.10. Register table: Page09h (LVDS function setting)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	0Ch	R/W	[7:0]	PAGE[7:0]	Register page selection.	Group 16 **(2 times)**
01h	00h	R/W	[7]	-	Reserved.	
		R/W	[6]	DLL_BANK	LVDS input frequency range selection.	
		R/W	[5]	LVDS_AGING	LVDS power saving enable.	
		R/W	[4]	LVDS_FMT	LVDS and TTL input data format selection.	
		R/W	[3]	LANE_SW	LVDS lane swapping selection.	
		R/W	[2]	LANE_PN	LVDS lane PN polarity swapping selection.	
		R/W	[1:0]	LVDS_PULL[1:0]	LVDS DLL bias current adjustment.	
02h	13h	R/W	[7]	-	Reserved.	
		R/W	[6]	-	Reserved.	
		R/W	[5:4]	LVDS_BW[1:0]	Select odd DLL bandwidth for LVDS.	
		R/W	[3:0]	LVDS_CPB[3:0]	LVDS Charge pump current selection.	
03h	97h	R/W	[7:6]	RX_VB[1:0]	LVDS DLL bias current adjustment.	
		R/W	[5:4]	LVDS_VBDLL[1:0]	LVDS DLL bias current adjustment.	
		R/W	[3]	S3_EQ_OPT	RX equalization DC DB function of Slave3 chip.	
		R/W	[2]	S2_EQ_OPT	RX equalization DC DB function of Slave2 chip.	
		R/W	[1]	S1_EQ_OPT	RX equalization DC DB function of Slave1 chip.	
		R/W	[0]	M_EQ_OPT	RX equalization DC DB function of master chip.	
04h	AAh	R/W	[7:6]	S3_EQ_SW[1:0]	LVDS clock lane equalization peak function selection of Slave3 chip.	
		R/W	[5:4]	S2_EQ_SW[1:0]	LVDS clock lane equalization peak function selection of Slave2 chip.	
		R/W	[3:2]	S1_EQ_SW[1:0]	LVDS clock lane equalization peak function selection of Slave1 chip.	
		R/W	[1:0]	M_EQ_SW[1:0]	LVDS clock lane equalization peak function selection of master chip.	

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8.1.11. Register table: Page0Ah (Temperature sensor function setting)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	0Ch	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	03h	R/W	[7:2]	-	Reserved.	Group17 **(5 Times)**
		R/W	[1]	VCOMS_HT[8]	VCOM voltage adjustment at high temperature mode.	
		R/W	[0]	VCOMS_LT[8]	VCOM voltage adjustment at low temperature mode.	
02h	5Ch	R/W	[7:0]	VCOMS_HT[7:0]	VCOM voltage adjustment at high temperature mode.	
03h	5Ch	R/W	[7:0]	VCOMS_LT[7:0]	VCOM voltage adjustment at low temperature mode.	
04h	1Ch	R/W	[7]	-	Reserved.	Group18 **(2 times)**
		R/W	[6:0]	VGHS_HT[6:0]	5V.	
05h	0Ch	R/W	[7:6]	-	Reserved.	
		R/W	[5:0]	VGLS_HT[5:0]	-5.0V.	
06h	1Ch		[7]	-	Reserved.	
		R/W	[6:0]	VGHS_LT[6:0]	5V.	
07h	0Ch	R/W	[7]	DIM_OPT	Analog gamma **(AGAM)** voltage dimming option.	
		R/W	[6]	-	Reserved.	
		R/W	[5:0]	VGLS_LT[5:0]	VGL voltage selection at low temperature.	
08h	1Ah	R/W	[7]	DIM_EN	Voltage dimming enable at temperature mode.	
		R/W	[6:5]	DIM_FRAME[1:0]	Dimming frame period setting.	
		R/W	[4:0]	VGMPHS_HT[4:0]	VGMPLS voltage adjustment at high temperature mode.	
09h	1Ah	R/W	[7]	TS_GOE_EN	Temperature mode disable and GOE setting by RT register.	
		R/W	[6]	TS_GAMMA_EN	Gamma voltage setting for temperature.	
		R/W	[4:0]	VGMNHS_HT[4:0]	VGMNHS voltage adjustment at high temperature mode.	
0Ah	11h	R/W	[7:4]	VGMPLS_HT[3:0]	VGMPLS voltage adjustment at high temperature mode.	
		R/W	[3:0]	VGMNLS_HT[3:0]	VGMNLS voltage adjustment at high temperature mode.	
0Bh	1Ah	R/W	[7]	-	Reserved.	
		R/W	[6]	TS_VCOM_EN	VCOM voltage setting for temperature.	
		R/W	[5]	TS_VGHL_EN	VGH and VGL voltage setting for temperature.	
		R/W	[4:0]	VGMPHS_LT[4:0]	VGMPHS voltage adjustment at low temperature mode.	
0Ch	1Ah	R/W	[7:6]	-	Reserved.	
		R/W	[4:0]	VGMNHS_LT[4:0]	VGMNHS voltage adjustment at low temperature mode.	
0Dh	11h	R/W	[7:4]	VGMPLS_LT[3:0]	VGMPLS voltage adjustment at low temperature mode.	
		R/W	[3:0]	VGMNLS_LT[3:0]	VGMNLS voltage adjustment at low temperature mode.	

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8.1.12. Register table: Page0Bh (OTP function setting)

Address	Default	Read/ Write	D[7:0]	Name	Description	Note
00h	0Ch	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7:6]	-	Reserved.	-
		R/W	[5:0]	OTP_Group[5:0]	Write OTP group select.	-
02h	99h	R/W	[7:0]	WOTP[7:0]	OTP program command enable.	-
03h	00h	R/W	[7]	OTP_WR4	OTP write function enable. **(SID[1:0]=HH)**	-
		R/W	[6]	OTP_WR3	OTP write function enable. **(SID[1:0]=HL)**	-
		R/W	[5]	OTP_WR2	OTP write function enable. **(SID[1:0]=LH)**	-
		R/W	[4]	OTP_WR1	OTP write function enable. **(SID[1:0]=LL)**	-
		R/W	[3]	OTP_WR_ALL_GROUP	Write All OTP_Group enable	-
		R/W	[2]	OTP_RELOAD	OTP reload function enable.	-
		R/W	[1]	OTP_RD	OTP read function enable.	-
		R/W	[0]	-	Reserved.	-
04h	00h	R/W	[7:2]	-	Reserved.	-
		R/W	[1:0]	OTP_INDEX[9:8]	OTP address for read.	-
05h	00h	R/W	[7:0]	OTP_INDEX[7:0]	OTP address for read.	-
06h	00h	R	[7:0]	PDOB[7:0]	OTP read out data.	Read only
07h	00h	R/W	[7:0]	OTP_DIN[7:0]	OTP write in data. **(manual mode)**	-
08h	5Ah	R/W	[7:0]	-	Reserved.	-
09h	00h	R/W	[7:0]	-	Reserved.	-
0ah	5Ah	R/W	[7:0]	EEP_PWD[7:0]	EEPROM software reload enable.	-
0bh	00h	R	[7]	EEP_CKSUM_FAIL	EEPROM check-sum flag.	Read only
		R/W	[7:1]	-	Reserved.	-
		R/W	[0]	EEP_RL_CMD	EEPROM software reload.	-
0ch	42h	R/W	[7:5]	SIDEN_XOR[2:0]	SIDEN XOR hardware pin.	-
		R/W	[4]	EESEL	EEPROM controlled by System or Driver IC.	-
		R/W	[3]	-	Reserved.	-
		R/W	[2:0]	FCS_XOR[2:0]	FCS XOR hardware pin.	-
0dh	AAh	R/W	[7:0]	STBYB_XOR[7:0]	Standby command.	-
0eh	00h	R/W	[7:6]	-	Reserved.	-
		R/W	[5:4]	ATREN_XOR[1:0]	HW_PIN xor control.	-
		R/W	[3:2]	-	Reserved.	-
		R/W	[1:0]	TS_XOR[1:0]	TS PIN xor control.	-
0Fh	00h	R	[7:0]	TCON_CKSUM[7:0]	Checksum by TCON calculation.	Read only
10h	00h	R	[7:0]	EEPROM_CKSUM[7:0]	Checksum by eeprom.	Read only
11h	00h	R	[7:2]	-	Reserved.	-
		R	[1]	OTP_TRIM_FULL	OTP program check flag.	Read only
		R	[0]	OTP_TRIM_FLAG	OTP program check flag.	Read only
12h	00h	R	[7:0]	OTP_PASS1[7:0]	OTP table password1.	Read only
13h	00h	R	[7:0]	OTP_PASS2[7:0]	OTP table password2.	Read only
1Bh	00	R	[4:0]	TS_VCOM_FLAG[4:0]	OTP timer of group 17.	Read only
1Dh	00	R	[7:5]	NGAMMA_FLAG[2:0]	OTP timer of group 10.	Read only
		R	[4:2]	PGAMMA_FLAG[2:0]	OTP timer of group 9.	Read only
		R	[1:0]	VCOM_FLAG[9:8]	OTP timer of group 8.	Read only
1Eh	00h	R	[7:0]	VCOM_FLAG[7:0]	OTP timer of group 8.	Read only

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8.1.13. Register table: Page0Ch (LTPS function setting)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	00h	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	B5h	R/W	[7:6]	LTPS_SWB_POFF2[1:0]	MUXB state during power off period2.	Group 19 **(2 times)**
		R/W	[5:4]	LTPS_SWB_POFF1[1:0]	MUXB state during power off period1.	
		R/W	[3:2]	LTPS_SW_POFF2[1:0]	MUX state during power off period2.	
		R/W	[1:0]	LTPS_SW_POFF1[1:0]	MUX state during power off period1.	
02h	00h	R/W	[7:6]	LTPS_SWB_PON2[1:0]	MUXB state during power on period2.	
		R/W	[5]	-	Reserved.	
		R/W	[4]	LTPS_SWB_PON1	MUXB state during power on period1.	
		R/W	[3:2]	LTPS_SW_PON2[1:0]	MUX state during power on period2.	
		R/W	[1]	-	Reserved.	
		R/W	[0]	LTPS_SW_PON1	MUX state during power on period1.	
03h	00h	R/W	[7]	LTPS_SW_EQ_EN	LTPS SW pre-charge enable.	
		R/W	[6:0]	LTPS_SW_EQ_VSN_R[6:0]	Time for pre-charge LTPS SW output from VGL to VSN.	
04h	09h	R/W	[7]	-	Reserved.	
		R/W	[6:0]	LTPS_SW_EQ_GND_R[6:0]	Time for pre-charge LTPS SW output from VSN to GND.	
05h	00h	R/W	[7]	-	Reserved.	
		R/W	[6:0]	LTPS_SW_EQ_VSP_R[6:0]	Time for pre-charge LTPS SW output from GND to VSP.	
06h	00h	R/W	[7]	-	Reserved.	
		R/W	[6:0]	LTPS_SW_EQ_VSN_F[6:0]	Time for pre-charge LTPS SW output from GND to VSN.	
07h	09h	R/W	[7]	-	Reserved.	
		R/W	[6:0]	LTPS_SW_EQ_GND_F[6:0]	Time for pre-charge LTPS SW output from VSP to GND.	
08h	00h	R/W	[7]	-	Reserved.	
		R/W	[6:0]	LTPS_SW_EQ_VSP_F[6:0]	Time for pre-charge LTPS SW output from VGH to VSP.	
09h	57h	R/W	[7:6]	-	Reserved.	
		R/W	[5:4]	LTPS_RL_EN_S2[1:0]	Slave2 RL side LTPS MUX enable.	
		R/W	[3:2]	LTPS_RL_EN_S1[1:0]	Slave1 RL side LTPS MUX enable.	
		R/W	[1:0]	LTPS_RL_EN_M[1:0]	Master RL side LTPS MUX enable.	
0Ah	00h	R/W	[7:4]	H_TOTAL_OFT[3:0]	H total number offset.	
		R/W	[3]	LTPS_BANK_F	LTPS bank on sequence setting.	
		R/W	[2:1]	LTPS_BANK_L[1:0]	LTPS bank on sequence setting.	
		R/W	[0]	-	Reserved.	
0Bh	00h	R/W	[7:5]	OSC_DEVI_OFST[2:0]	Source OP output compensation.	
		R/W	[4]	LTPS_SW_VBLK	LTPS SW toggle at vertical blanking.	
		R/W	[3:2]	LTPS_SW_BP[1:0]	MUX output before source output line.	
		R/W	[1:0]	LTPS_SW_FP[1:0]	MUX output delay source output line.	
0Ch	00h	R/W	[7:0]	PRE_ST[7:0]	LTPS CKH pre-charge rising time between HS.	
0Dh	00h	R/W	[7:0]	PRE_WD[7:0]	LTPS CKH pre-charge time H_period.	
0Eh	08h	R/W	[7]	-	Reserved.	
		R/W	[6:0]	TOEB1[6:0]	Adjust the LTPS SW1/SW2/SW3 rising time from EQ0.	
0Fh	0Ah	R/W	[7]	-	Reserved.	
		R/W	[6:0]	TOEF1[6:0]	Adjust the LTPS SW1/SW2/SW3 falling time from next EQ0.	
10h	08h	R/W	[7]	-	Reserved.	
		R/W	[6:0]	TOEB2[6:0]	Adjust the LTPS SW1/SW2/SW3 rising time from EQ0.	
11h	0Ah	R/W	[7]	-	Reserved.	
		R/W	[6:0]	TOEF2[6:0]	Adjust the LTPS SW1/SW2/SW3 falling time from next EQ0.	
12h	08h	R/W	[7]	-	Reserved.	
		R/W	[6:0]	TOEB3[6:0]	Adjust the LTPS SW1/SW2/SW3 rising time from EQ0.	
13h	0Ah	R/W	[7]	-	Reserved.	
		R/W	[6:0]	TOEF3[6:0]	Adjust the LTPS SW1/SW2/SW3 falling time from next EQ0.	

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Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
14h	00h	R/W	[7:0]	BANK12_OFT_LINE1[7:0]	Line1 shift divided position between Bank1 and Bank2.	
15h	00h	R/W	[7:0]	BANK23_OFT_ LINE 1[7:0]	Line1 shift divided position between Bank2 and Bank3.	
16h	00h	R/W	[7:0]	BANK12_OFT_ LINE 2[7:0]	Line2 shift divided position between Bank1 and Bank2.	
17h	00h	R/W	[7:0]	BANK23_OFT_ LINE 2[7:0]	Line2 shift divided position between Bank2 and Bank3.	
18h	00h	R/W	[7:0]	BANK12_OFT_ LINE 3[7:0]	Line3 shift divided position between Bank1 and Bank2.	
19h	00h	R/W	[7:0]	BANK23_OFT_ LINE 3[7:0]	Line3 shift divided position between Bank2 and Bank3.	
1Ah	05h	R/W	[7]	LTPS_MUX_OPT	LTPS MUX waveform setting during line switch.	
		R/W	[6]	-	Reserved.	
		R/W	[5]	BANK_EQ_OPT	Bank2, Bank3 with EQ0 **(only for LTPS mode)**.	
		R/W	[4]	BANK_OFT_FACTOR	LTPS register step factor.	
		R/W	[3:2]	LTPS_SWB_GAS[1:0]	MUXB state during GAS.	
		R/W	[1:0]	LTPS_SW_GAS[1:0]	MUX state during GAS.	
1Bh	5Fh	R/W	[7:6]	LTPS_DRVP[1:0]	LTPS MUX output pin driving ability setting.	
		R/W	[5:4]	LTPS_DRVN[1:0]	LTPS MUX output pin driving ability setting.	
		R/W	[3:2]	GIP_DRVP[1:0]	GIP1~GIP20 output pin driving ability setting.	
		R/W	[1:0]	GIP_DRVN[1:0]	GIP1~GIP20 output pin driving ability setting.	
1Ch	00h	R/W	[7:2]	LTPS_BANK_EQ_OFT[5:0]	EQ0 delay time from bank.	
		R/W	[1:0]	LTPS_PRE_SEL[1:0]	For LTPS page , PRE_ST / PRE_WD setting.	
1Dh	00h	R/W	[7:0]	LTPS_GOE_PRE[7:0]	Set GOE leading cycles from OEH.	
1Eh	00h	R/W	[7:0]	BIST_LTPS_GOE_PRE[7:0]	Set GOE leading cycles from OEH.	

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8.1.14. Register table: Page0Dh ~ Page13h (GIP function)

Please refer to application note for GIP function.
(OTP group 20~26, and can be programmed 2 times.)

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8.1.15. Register table: Page14h (ESD and SSC function Cont.)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	0Ch	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	ABh	R/W	[7:6]	ESD_DEVALID_OPT[1:0]	Length of de valid.	Group 27 **(1 time)**
		R/W	[5:4]	GMASK_OPT[1:0]	Number line of oev_mask.	
		R/W	[3]	HBLK_PROT	H-blanking protection range selection.	
		R/W	[2]	HS_STABLE_EN	Hs stable function enable.	
		R/W	[1]	ESD_MASK_EN	OEV mask function when esd time enable.	
		R/W	[0]	ESD_PROT	Esd protection enable.	
02h	00h	R/W	[7:0]	-	Reserved.	
03h	00h	R/W	[7:0]	-	Reserved.	
04h	10h	R/W	[7:0]	HS_STABLE[7:0]	Hs stable time setting.	
05h	07h	R/W	[7]	ESD_REQ_MASK	Pass/reject gate_mask request from ESD_SYNC.	
		R/W	[6]	HS_VBLK_OPT	Vblking **(V-front porch)** not protect.	
		R/W	[5:4]	HS_SUM_TOL[1:0]	Hs_sum tolerance.	
		R/W	[3:0]	HS_REGEN_OPT[3:0]	Hs_regen point setting when hs hold high.	
06h	B0h	R/W	[7:6]	ESD_PROT_SEL[1:0]	Input HS/VS/DE /data de-glitch.	
		R/W	[5:3]	DEM_H_VBLK_DEV[2:0]	Define last line width on V-blanking for DE mode.	
		R/W	[2:0]	-	Reserved.	
07h	00h	R/W	[7]	GIP_SS_EN	Gate/GIP SS enable.	Group 28 **(2 times)**
		R/W	[6]	LTPS_T2_SSEN	LTPS mode SSC enable.	
		R/W	[5:4]	GIP_SS_ST[1:0]	GIP_GOE/GIP_T2/GIP_T3 SSC setting.	
		R/W	[3]	SG_SSEN	Source OP switch SSC feature enable.	
		R/W	[2]	SD_EQ_SSEN	Enable Source EQ switch SSC feature **(not for column inversion)**.	
		R/W	[1:0]	MUX_SSC[1:0]	Mux_ssc enable **(LTPS mode only)**.	
08h	00h	R/W	[7:4]	-	Reserved.	
		R/W	[3]	CPCLK_SSC_SEL	CPCLK SSC step.	
		R/W	[2]	CPCLK_SSCEN	Enable CPCLK SSC function.	
		R/W	[1:0]	SD_SS_ST[1:0]	Source OP SSC range /GATE ssc range.	
09h	11h	R/W	[7]	REG_LVDS_GATED_OPT	Gated VS / HS / DE by lvds_lock enable.	
		R/W	[6:5]	-	Reserved.	
		R/W	[4]	REG_HS_LONG_OPT	HS long high protection.	
		R/W	[3]	LOCK_GATED_ENB	LVDS_lock |bs7 gated HS/VS/DE for input signal.	
		R/W	[2]	STV_PROT_ENB	STV_PROTECTION enable.	
		R/W	[1:0]	EQ0_PCR[1:0]	tEQ0_1 -> tEQ0_6 divided select.	
0Ah	08h	R/W	[7:5]	-	Reserved.	
		R/W	[4:0]	DEM_VBLK_LINE[4:0]	Compensation line number setting **(only DE mode)**.	
0Bh	00h	R/W	[7:0]	-	Reserved.	
0Ch	00h	R/W	[7:0]	-	Reserved.	

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8.1.16. Register table: Page15h (Vender ID function)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	0Ch	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7:0]	VENDOR_ID1[7:0]	For vender OTP.	Group29 **(1 time)**
02h	0h	R/W	[7:0]	VENDOR_ID2[7:0]	For vender OTP.	
03h	0h	R/W	[7:0]	VENDOR_ID3[7:0]	For vender OTP.	
04h	0h	R/W	[7:0]	VENDOR_ID4[7:0]	For vender OTP.	
05h	0h	R/W	[7:0]	VENDOR_ID5[7:0]	For vender OTP.	
06h	0h	R/W	[7:0]	VENDOR_ID6[7:0]	For vender OTP.	
07h	0h	R/W	[7:0]	VENDOR_ID7[7:0]	For vender OTP.	
08h	0h	R/W	[7:0]	VENDOR_ID8[7:0]	For vender OTP.	
09h	0h	R/W	[7:0]	VENDOR_ID9[7:0]	For vender OTP.	
0Ah	0h	R/W	[7:0]	VENDOR_ID10[7:0]	For vender OTP.	
0Bh	0h	R/W	[7:0]	VENDOR_ID11[7:0]	For vender OTP.	
0Ch	0h	R/W	[7:0]	VENDOR_ID12[7:0]	For vender OTP.	
0Dh	0h	R/W	[7:0]	VENDOR_ID13[7:0]	For vender OTP.	
0Eh	0h	R/W	[7:0]	VENDOR_ID14[7:0]	For vender OTP.	
0Fh	0h	R/W	[7:0]	VENDOR_ID15[7:0]	For vender OTP.	
10h	0h	R/W	[7:0]	VENDOR_ID16[7:0]	For vender OTP.	
11h	0h	R/W	[7:0]	VENDOR_ID17[7:0]	For vender OTP.	
12h	0h	R/W	[7:0]	VENDOR_ID18[7:0]	For vender OTP.	
13h	0h	R/W	[7:0]	VENDOR_ID19[7:0]	For vender OTP.	
14h	0h	R/W	[7:0]	VENDOR_ID20[7:0]	For vender OTP.	
15h	0h	R/W	[7:0]	VENDOR_ID21[7:0]	For vender OTP.	
16h	0h	R/W	[7:0]	VENDOR_ID22[7:0]	For vender OTP.	
17h	0h	R/W	[7:0]	VENDOR_ID23[7:0]	For vender OTP.	
18h	0h	R/W	[7:0]	VENDOR_ID24[7:0]	For vender OTP.	
19h	0h	R/W	[7:0]	VENDOR_ID25[7:0]	For vender OTP.	
1Ah	0h	R/W	[7:0]	VENDOR_ID26[7:0]	For vender OTP.	
1Bh	0h	R/W	[7:0]	VENDOR_ID27[7:0]	For vender OTP.	
1Ch	0h	R/W	[7:0]	VENDOR_ID28[7:0]	For vender OTP.	
1Dh	0h	R/W	[7:0]	VENDOR_ID29[7:0]	For vender OTP.	
1Eh	0h	R/W	[7:0]	VENDOR_ID30[7:0]	For vender OTP.	

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8.1.17. Register table: Page16h (CRC function setting)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
01h	40h	R/W	[7]	-	Reserved.	-
		R/W	[6]	CRC_CNT_OPT	CRC compare mode selection.	
		R/W	[5]	CRC_TYPE	CRC compare mode selection.	
		R/W	[4:3]	CRC_MODE	CRC mode setting.	
		R/W	[2]	CRC_INI_SEL	CRC iniitial value.	
		R/W	[1:0]	CRC_IN_SWAP[1:0]	CRC input data order swap funtion.	
02h	00h	R/W	[7:4]	CRC_WIN1_H1[11:8]	Define CRC window1 left side X_ordinate.	
		R/W	[3:0]	CRC_WIN1_H2[11:8]	Define CRC window1 right side X_ordinate.	
03h	01h	R/W	[7:0]	CRC_WIN1_H1[7:0]	Define CRC window1 left side X_ordinate.	
04h	A0h	R/W	[7:0]	CRC_WIN1_H2[7:0]	Define CRC window1 right side X_ordinate.	
05h	00h	R/W	[7:4]	CRC_WIN1_V1[11:8]	Define CRC window1 Top side Y_ordinate.	
		R/W	[3:0]	CRC_WIN1_V2[11:8]	Define CRC window1 Bottom side Y_ordinate.	
06h	01h	R/W	[7:0]	CRC_WIN1_V1[7:0]	Define CRC window1 Top side Y_ordinate.	
07h	80h	R/W	[7:0]	CRC_WIN1_V2[7:0]	Define CRC window1 Bottom side Y_ordinate.	
08h	00h	R/W	[7:4]	CRC_WIN2_H1[11:8]	Define CRC window2 left side X_ordinate.	
		R/W	[3:0]	CRC_WIN2_H2[11:8]	Define CRC window2 right side X_ordinate.	
09h	01h	R/W	[7:0]	CRC_WIN2_H1[7:0]	Define CRC window2 left side X_ordinate.	
0Ah	A0h	R/W	[7:0]	CRC_WIN2_H2[7:0]	Define CRC window2 right side X_ordinate.	
0Bh	00h	R/W	[7:4]	CRC_WIN2_V1[11:8]	Define CRC window2 Top side Y_ordinate.	
		R/W	[3:0]	CRC_WIN2_V2[11:8]	Define CRC window2 Bottom side Y_ordinate.	
0Ch	01h	R/W	[7:0]	CRC_WIN2_V1[7:0]	Define CRC window2 Top side Y_ordinate.	
0Dh	80h	R/W	[7:0]	CRC_WIN2_V2[7:0]	Define CRC window2 Bottom side Y_ordinate.	
0Eh	00h	R/W	[7:4]	CRC_WIN3_H1[11:8]	Define CRC window3 left side X_ordinate.	
		R/W	[3:0]	CRC_WIN3_H2[11:8]	Define CRC window3 right side X_ordinate.	
0Fh	01h	R/W	[7:0]	CRC_WIN3_H1[7:0]	Define CRC window3 left side X_ordinate.	
10h	A0h	R/W	[7:0]	CRC_WIN3_H2[7:0]	Define CRC window3 right side X_ordinate.	
11h	00h	R/W	[7:4]	CRC_WIN3_V1[11:8]	Define CRC window3 Top side Y_ordinate.	
		R/W	[3:0]	CRC_WIN3_V2[11:8]	Define CRC window3 Bottom side Y_ordinate.	
12h	01h	R/W	[7:0]	CRC_WIN3_V1[7:0]	Define CRC window3 Top side Y_ordinate.	
13h	80h	R/W	[7:0]	CRC_WIN3_V2[7:0]	Define CRC window3 Bottom side Y_ordinate.	
14h	00h	R/W	[7:4]	CRC_WIN4_H1[11:8]	Define CRC window4 left side X_ordinate.	
		R/W	[3:0]	CRC_WIN4_H2[11:8]	Define CRC window4 right side X_ordinate.	
15h	01h	R/W	[7:0]	CRC_WIN4_H1[7:0]	Define CRC window4 left side X_ordinate.	
16h	A0h	R/W	[7:0]	CRC_WIN4_H2[7:0]	Define CRC window4 right side X_ordinate.	
17h	00h	R/W	[7:4]	CRC_WIN4_V1[11:8]	Define CRC window4 Top side Y_ordinate.	
		R/W	[3:0]	CRC_WIN4_V2[11:8]	Define CRC window4 Bottom side Y_ordinate.	
18h	01h	R/W	[7:0]	CRC_WIN4_V1[7:0]	Define CRC window4 Top side Y_ordinate.	
19h	80h	R/W	[7:0]	CRC_WIN4_V2[7:0]	Define CRC window4 Bottom side Y_ordinate.	
1Ah	00h	R/W	[7:0]	CRC_CKSUM_NUM[7:0]	CRC checksum compare frames.	
1Bh	00h	R/W	[7:5]	-	Reserved.	
		R/W	[4]	CRC_EN	CRC function enable.	
		R/W	[3]	CRC4_EN	CRC4 enable.	
		R/W	[2]	CRC3_EN	CRC3 enable.	
		R/W	[1]	CRC2_EN	CRC2 enable.	
		R/W	[0]	CRC1_EN	CRC1 enable.	

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8.1.18. Register table: Page17h (CRC predict value setting)

Address	Default	Read/ Write	D[7:0]	Name	Description	Note
00h	1Bh	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7:0]	CRC_PRED_SUM1[31:24]	CRC System predict value of window1.	-
02h	00h	R/W	[7:0]	CRC_PRED_SUM1[23:16]	CRC System predict value of window1.	-
03h	00h	R/W	[7:0]	CRC_PRED_SUM1[15:8]	CRC System predict value of window1.	-
04h	00h	R/W	[7:0]	CRC_PRED_SUM1[7:0]	CRC System predict value of window1	-
05h	00h	R/W	[7:0]	CRC_PRED_SUM2[31:24]	CRC System predict value of window2.	-
06h	00h	R/W	[7:0]	CRC_PRED_SUM2[23:16]	CRC System predict value of window2.	-
07h	00h	R/W	[7:0]	CRC_PRED_SUM2[15:8]	CRC System predict value of window2.	-
08h	00h	R/W	[7:0]	CRC_PRED_SUM2[7:0]	CRC System predict value of window2.	-
09h	00h	R/W	[7:0]	CRC_PRED_SUM3[31:24]	CRC System predict value of window3.	-
0Ah	00h	R/W	[7:0]	CRC_PRED_SUM3[23:16]	CRC System predict value of window3.	-
0Bh	00h	R/W	[7:0]	CRC_PRED_SUM[315:8]	CRC System predict value of window3.	-
0Ch	00h	R/W	[7:0]	CRC_PRED_SUM3[7:0]	CRC System predict value of window3.	-
0Dh	00h	R/W	[7:0]	CRC_PRED_SUM4[31:24]	CRC System predict value of window4.	-
0Eh	00h	R/W	[7:0]	CRC_PRED_SUM4[23:16]	CRC System predict value of window4.	-
0Fh	00h	R/W	[7:0]	CRC_PRED_SUM4[15:8]	CRC System predict value of window4.	-
10h	00h	R/W	[7:0]	CRC_PRED_SUM4[7:0]	CRC System predict value of window4.	-

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8.1.19. Register table: Page18h (CRC calculated value)

Address	Default	Read/ Write	D[7:0]	Name	Description	Note
00h	0Ch	R	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R	[7:1]	CRC_TCON_SUM1[31:24]	CRC TCON calculated value of window 1.	Read only
02h	00h	R	[7:2]	CRC_TCON_SUM1[23:16]	CRC TCON calculated value of window 1.	
03h	00h	R	[7:3]	CRC_TCON_SUM1[15:8]	CRC TCON calculated value of window 1.	
04h	00h	R	[7:4]	CRC_TCON_SUM1[7:0]	CRC TCON calculated value of window 1.	
05h	00h	R	[7:5]	CRC_TCON_SUM2[31:24]	CRC TCON calculated value of window 2.	
06h	00h	R	[7:6]	CRC_TCON_SUM2[23:16]	CRC TCON calculated value of window 2.	
07h	00h	R	[7:7]	CRC_TCON_SUM2[15:8]	CRC TCON calculated value of window 2.	
08h	00h	R	[7:8]	CRC_TCON_SUM2[7:0]	CRC TCON calculated value of window 2.	
09h	00h	R	[7:9]	CRC_TCON_SUM3[31:24]	CRC TCON calculated value of window 3.	
0Ah	00h	R	[7:10]	CRC_TCON_SUM3[23:16]	CRC TCON calculated value of window 3.	
0Bh	00h	R	[7:11]	CRC_TCON_SUM3[15:8]	CRC TCON calculated value of window 3.	
0Ch	00h	R	[7:12]	CRC_TCON_SUM3[7:0]	CRC TCON calculated value of window 3.	
0Dh	00h	R	[7:13]	CRC_TCON_SUM4[31:24]	CRC TCON calculated value of window 4.	
0Eh	00h	R	[7:14]	CRC_TCON_SUM4[23:16]	CRC TCON calculated value of window 4.	
0Fh	00h	R	[7:15]	CRC_TCON_SUM4[15:8]	CRC TCON calculated value of window 4.	
10h	00h	R	[7:16]	CRC_TCON_SUM4[7:0]	CRC TCON calculated value of window 4.	
11h	00h	R	[7:17]	CRC_ERR_CNT1[15:8]	CRC fail accumulated counter of window 1.	
12h	00h	R	[7:18]	CRC_ERR_CNT1[7:0]	CRC fail accumulated counter of window 1.	
13h	00h	R	[7:19]	CRC_ERR_CNT2[15:8]	CRC fail accumulated counter of window 2.	
14h	00h	R	[7:20]	CRC_ERR_CNT2[7:0]	CRC fail accumulated counter of window 2.	
15h	00h	R	[7:21]	CRC_ERR_CNT3[15:8]	CRC fail accumulated counter of window 3.	
16h	00h	R	[7:22]	CRC_ERR_CNT3[7:0]	CRC fail accumulated counter of window 3.	
17h	00h	R	[7:23]	CRC_ERR_CNT4[15:8]	CRC fail accumulated counter of window 4.	
18h	00h	R	[7:24]	CRC_ERR_CNT4[7:0]	CRC fail accumulated counter of window 4.	

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8.1.20. Register table: Page19h (Fail flag, read only)

Address	Default	Read/ Write	D[7:0]	Name	Description	Note
00h	0Ch	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R	[7]	PFM NG fail	Fail flag Group1. **(0: OK, 1: fail)**	Read only
		R	[6]	OTP trim fail		
		R	[5]	EEPROM fail		
		R	[4]	No-VIDEO fail		
		R	[3]	Gate fail		
		R	[2]	SD_DET fail		
		R	[1]	OTP full fail		
		R	[0]	LVDS lock fail		
02h	00h	R	[7]	GAS_VGL fail	Fail flag Group2. **(0: OK, 1: fail)**	Read only
		R	[6]	GAS_PFM fail		
		R	[5]	GAS_VCC fail		
		R	[4]	CRC check fail		
		R	[3]	AGM P/N check sum fail		
		R	[2]	OTP check sum fail		
		R	[1]	OTP reload fail		
		R	[0]	-	Reserved.	
03h	00h	R	[7]	OVP VCC fail	Fail flag Group3. **(0: OK, 1: fail)**	Read only
		R	[6]	OVP VSP fail		
		R	[5]	OVP VSN fail		
		R	[4]	OVP VGH fail		
		R	[3]	OVP VGL fail		
		R	[2]	OVP VCOM fail		
		R	[1]	LVD VGH fail		
		R	[0]	LVD VCOM fail		
04h	00h	R	[7]	OVP VGMPL fail	Fail flag Group4. **(0: OK, 1: fail)**	Read only
		R	[6]	OVP VGMNL fail		
		R	[5]	OVP VDDD fail		
		R	[4]	OVP VCL fail		
		R	[3]	LVD VGMPH fail		
		R	[2]	LVD VGMNH fail		
		R	[1]	LVD VSDPN fail		
		R	[0]	LVD VCL fail		
05h	00h	R	[7]	PFM NG fail	Group1: Power on fail flag. **(0: OK, 1: fail)**	Read only
		R	[6]	OTP reload fail		
		R	[5]	EEPROM fail		
		R	[4]	No-video fail		
		R	[3]	Gate fail		
		R	[2]	SOURCE fail		
		R	[1]	GAS		
		R	[0]	LVDS fail		
06h	00h	R	[7:2]	-	Reserved.	Read only
		R	[1]	OVP check fail	Group2: Power on fail flag. **(0: OK, 1: fail)**	
		R	[0]	CRC check fail		

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8.1.21. Register table: Page1Bh (OTP checksum)

Address	Default	Read/ Write	D[7:0]	Name	Description	Note
00h	0Ch	R	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R	[7:0]	OTP_CHECKSUM_GOLD [7:0]	OTP checksum golden for compare.	Group 30 **(3 times)**
02h	00h	R	[7:0]	OTP_CHECKSUM[7:0]	Checksum of group1~29 **(except 9 and 10)**.	Read only
03h	00h	R	[7:0]	P_CHECKSUM[7:0]	Checksum of group9.	
04h	00h	R	[7:0]	N_CHECKSUM[7:0]	Checksum of group10.	

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8.2. Register description

8.2.1. Page selection

R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
All	00h	1/0	PAGE[7:0]							
			0	0	0	0	1	1	0	0

PAGE[7:0]: Register page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	0	1	1	0	0	Page0Ch	Default

8.2.2. Page00h for Normal function setting

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	01h	1/0	GOA_ENB	PTS[2:0]			ZZS[1:0]		GSEL[1:0]	
			0	0	0	0	0	0	0	0

GOA_ENB: Gate type selection.

GDSEL	Function	Note
0	GIP	Default
1	Tradition gate driver	-

PTS[2:0]: Panel type selection.

PANEL_TYPE[2:0]			Function	Note
0	0	0	LTPS MUX 2:4	Default
0	0	1	LTPS MUX 2:6 TYPE1	-
0	1	0	LTPS MUX 2:6 TYPE2	-
0	1	1	LTPS MUX 1:1	-
1	0	0	Dual gate	-
1	0	1	Triple gate	-
:	:	:	Reserved	-
1	1	1	Reserved	-

ZZS[1:0]: Zig-Zag type selection.

ZIG-ZAG_TYPE[1:0]		Function	Note
0	0	Stripe panel	Default
0	1	Zig-Zag type 1	-
1	0	Zig-Zag type 2	-
1	1	Stripe panel	-

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GSEL[1:0]: Dual Gate on sequence select.

GSEL[1:0]		Function	Note
0	0	Z scan	Default
0	1	Bow scan	-
1	0	Inv-Z scan	-
1	1	Z+ inv-Z scan	-

R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	02h	1/0	TR[1:0]		DINT	MODE	HSP	VSP	CLOCKP	NB
			0	1	1	1	0	0	0	1

TR[1:0]: Interface select.

TR[1:0]		Function	Note
0	0	TTL	-
0	1	TTL	Default
1	0	1-port LVDS	-
1	1	2-port LVDS	-

DINT: Input data 6-bit or 8-bit selection.

DINT	Function	Note
0	6-bit	-
1	8-bit	Default

MODE: Sync or DE mode selection.

MODE	Function	Note
0	DE only mode	-
1	Sync (HS+VS) mode	Default

HSP: HS polarity for TTL / LVDS interface.

HSP	Function	Note
0	Low pulse	Default
1	High pulse	-

VSP: VS polarity for TTL / LVDS interface.

VSP	Function	Note
0	Low pulse	Default
1	High pulse	-

CLOCKP: Clock polarity for TTL interface.

CLOCKP	Function	Note
0	Rising edge	Default
1	Falling edge	-

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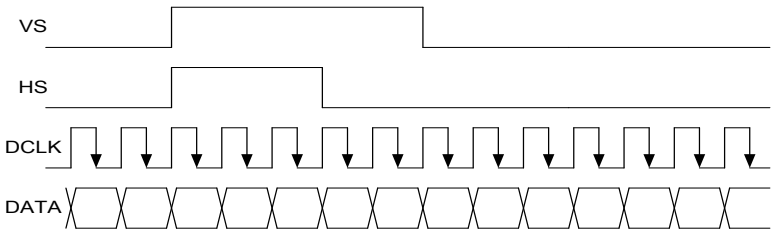
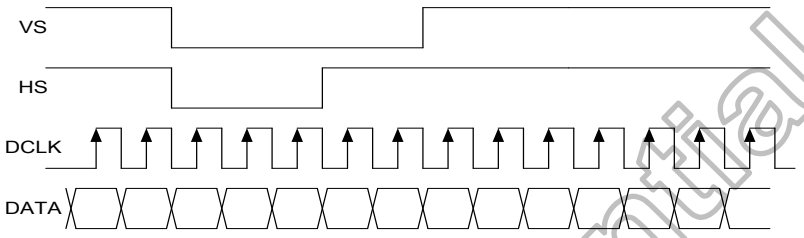
Example1: CLOCKP=1, VSP=1, HSP=1



Example2: CLOCKP=0, VSP=0, HSP=0 (default setting)



NB: Normally white/black selection.

NB	Function	Note
0	Normally white	-
1	Normally black	Default

R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	03h	1/0	RL	TB	INV[1:0]		RS[3:0]			
			0	0	0	0	0	0	0	0

RL: Horizontal scan direction. The horizontal scan direction=RL hardware pin "XOR" with RL register setting when FCS=L.

RL Hardware pin	RL Reg03[7]	Function	Note
L	0	Reverse **(S1920→S1)**	-
L	1	Forward **(S1→S1920)**	-
H	0	Forward **(S1→S1920)**	Default
H	1	Reverse **(S1920→S1)**	-

TB: Vertical scan direction. The vertical scan direction=TB hardware pin "XOR" with TB register setting when FCS=L.

TB Hardware pin	TB Reg03[6]	Function	Note
L	0	Reverse **(Bottom→Top)**	-
L	1	Forward **(Top→Bottom)**	-
H	0	Forward **(Top→Bottom)**	Default
H	1	Reverse **(Bottom→Top)**	-

INV[1:0]: Inversion algorithm selection.

INV[1:0]		Function			Note
		Single/ MUX2/ MUX3	Dual	Triple	
0	0	1 line dot inversion	1+2dot inversion	1line inversion	Default
0	1	1+2line dot inversion	2dot inversion	3line inversion	-
1	0	2+4line dot inversion	1+2line 2dot inversion	6line inversion	-
1	1	Column inversion	2+4line 2dot inversion	Column inversion	-

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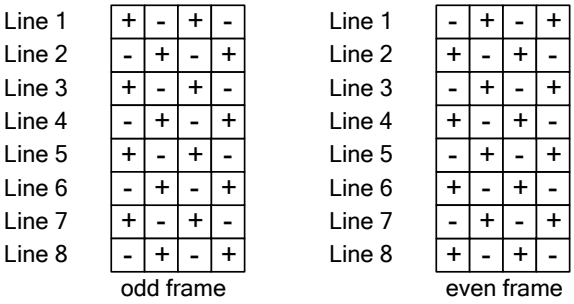
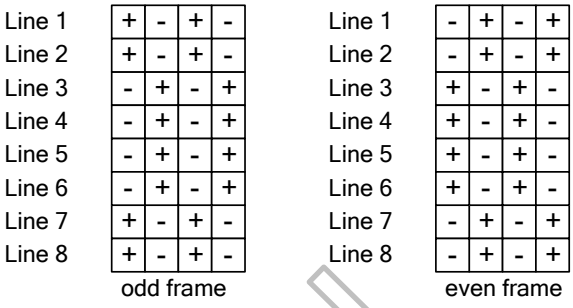
Single gate inversion algorithm

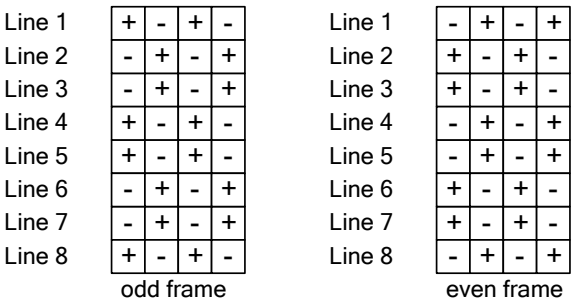
1 line dot inversion



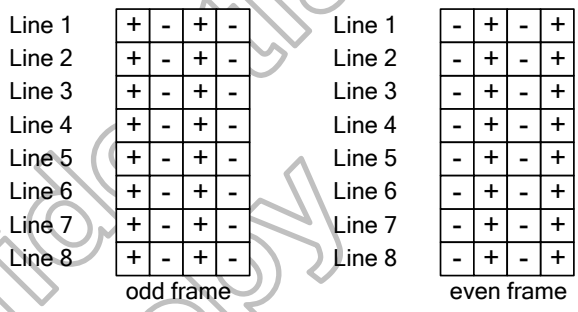
2+4 line dot inversion



1+2 line dot inversion

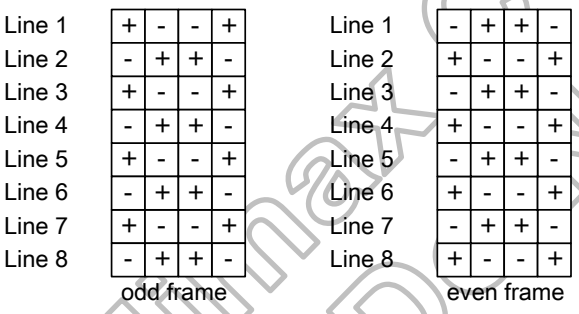


Column inversion

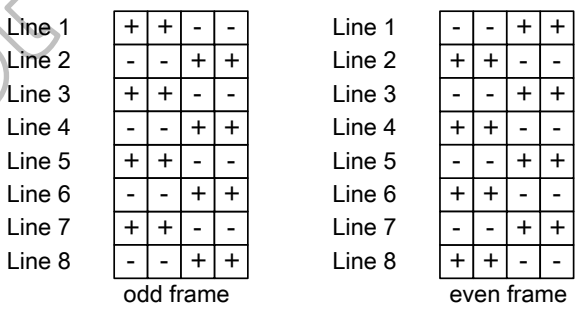


Dual gate inversion algorithm

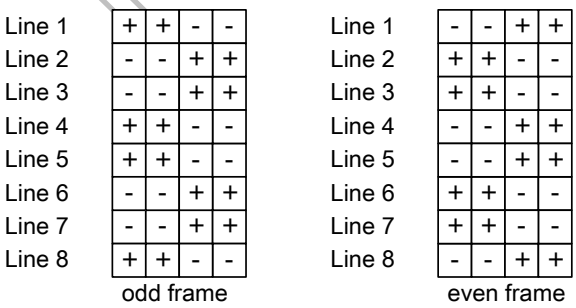
1+2 dot inversion



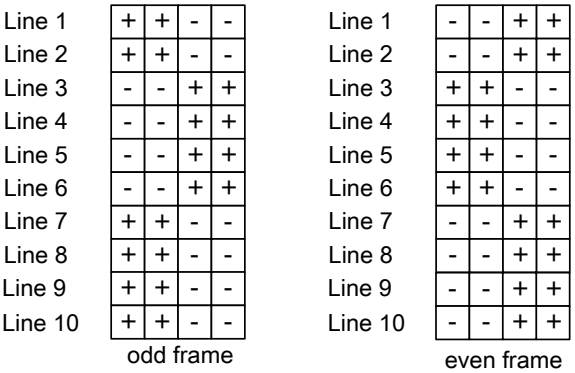
2 dot inversion



1+2 line 2 dot inversion



2+4 line 2 dot inversion



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Triple gate inversion algorithm

1 line inversion

Line 1	+	-	+	-
Line 2	-	+	-	+
Line 3	+	-	+	-
Line 4	-	+	-	+
Line 5	+	-	+	-
Line 6	-	+	-	+
Line 7	+	-	+	-
Line 8	-	+	-	+

odd frame

Line 1	-	+	-	+
Line 2	+	-	+	-
Line 3	-	+	-	+
Line 4	+	-	+	-
Line 5	-	+	-	+
Line 6	+	-	+	-
Line 7	-	+	-	+
Line 8	+	-	+	-

3 line inversion

Line 1	+	-	+	-
Line 2	+	-	+	-
Line 3	+	-	+	-
Line 4	-	+	-	+
Line 5	-	+	-	+
Line 6	-	+	-	+
Line 7	+	-	+	-
Line 8	+	-	+	-

odd frame

Line 1	-	+	-	+
Line 2	-	+	-	+
Line 3	-	+	-	+
Line 4	+	-	+	-
Line 5	+	-	+	-
Line 6	+	-	+	-
Line 7	-	+	-	+
Line 8	-	+	-	+

even frame

6 line inversion

Line 1	-	+	-	+
Line 2	-	+	-	+
Line 3	-	+	-	+
Line 4	+	-	+	-
Line 5	+	-	+	-
Line 6	+	-	+	-
Line 7	+	-	+	-
Line 8	+	-	+	-
Line 9	+	-	+	-
Line 10	-	+	-	+
Line 11	-	+	-	+
Line 12	-	+	-	+
Line 13	-	+	-	+
Line 14	-	+	-	+
Line 15	-	+	-	+

odd frame

Line 1	+	-	+	-
Line 2	+	-	+	-
Line 3	+	-	+	-
Line 4	-	+	-	+
Line 5	-	+	-	+
Line 6	-	+	-	+
Line 7	-	+	-	+
Line 8	-	+	-	+
Line 9	-	+	-	+
Line 10	+	-	+	-
Line 11	+	-	+	-
Line 12	+	-	+	-
Line 13	+	-	+	-
Line 14	+	-	+	-
Line 15	+	-	+	-

even frame

Column inversion

Line 1	+	-	+	-
Line 2	+	-	+	-
Line 3	+	-	+	-
Line 4	+	-	+	-
Line 5	+	-	+	-
Line 6	+	-	+	-
Line 7	+	-	+	-
Line 8	+	-	+	-

odd frame

Line 1	-	+	-	+
Line 2	-	+	-	+
Line 3	-	+	-	+
Line 4	-	+	-	+
Line 5	-	+	-	+
Line 6	-	+	-	+
Line 7	-	+	-	+
Line 8	-	+	-	+

even frame

RS[3:0]: Resolution selection.

RS[3:0]				Function	Note
0	0	0	0	2560 x RGB x 960	Default
0	0	0	1	1920 x RGB x 1080	-
0	0	1	0	1920 x RGB x 720	-
0	0	1	1	1660 x RGB x 1660	-
0	1	0	0	1560 x RGB x 720	-
0	1	0	1	1540 x RGB x 720	-
0	1	1	0	1440 x RGB x 540	-
0	1	1	1	1280 x RGB x 720	-
1	0	0	0	1280 x RGB x 480	-
1	0	0	1	1024 x RGB x 600	-
1	0	1	0	960 x RGB x 960	-
1	0	1	1	800 x RGB x 480	-
1	1	0	0	720 x RGB x 720	-
1	1	0	1	640 x RGB x 640	-
1	1	1	0	540 x RGB x 540	-
1	1	1	1	480 x RGB x 480	-

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R04h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	04h	1/0	RB_INV	DGAMEN	GPOS[1:0]		SD_GND_V[1:0]		PON	POFF
			0	0	0	0	0	1	0	0

RB_INV: R data and B data exchange.

RB_INV	Function	Note
0	R data and B data no exchange	Default
1	R data and B data exchange	-

DGAMEN: Digital gamma function enable.

DGAMEN	Function	Note
0	Disable	Default
1	Enable	-

GPOS[1:0]: Tradition Gate driver location.

GPOS[1:0]	Function	Note
00	Left side	Default
01	Right side	-
10	Interlaced driving at dual side	-
11	Progressive driving the same line at dual side **(multi-driving)**	-

SD_GND_V[1:0]: Source output state in vertical blanking.

SD_GND_V[1:0]	Function	Note
00	Source output keep the last data at V blanking	-
01	Source output pulled to ground at V blanking	Default
10	Source output keep Hi-Z at V blanking	-
11	Source output keep Hi-Z at V blanking	-

PON: White/Black pattern selection at power on sequence.

PON	Function	Note
0	Black pattern	Default
1	White pattern	-

POFF: White/Black pattern selection at power off sequence.

NB	POFF	Function	Note
1	0	Black pattern	Default
1	1	White pattern	-
0	0	White pattern	-
0	1	Black pattern	-

R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	05h	1/0	GAS_EN	SPFEN	SPFSEL	BISTEN	SD_CLK_SEL[1:0]		BIST_FNUM[1:0]	
			1	1	0	0	0	1	0	1

GAS_EN: GAS function enable.

GAS_EN	Function	Note
0	Disable	-
1	Enable	Default

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SPFEN: Self-protection mode enable.

SPFEN	Function	Note
0	Disable	-
1	Enable	Default

SPFSEL: White/Black pattern selection at self protection mode.

SPFSEL	Function	Note
0	Black pattern	Default
1	White pattern	-

BISTEN: BIST mode enable.

The BIST mode enable=BISTEN hardware pin “XOR” with BISTEN register setting when FCS = L.

BISTEN Hardware pin	BISTEN R05[4]	Function	Note
L	0	Disable	Default
L	1	Enable	-
H	0	Enable	-
H	1	Disable	-

SD_CLK_SEL[1:0]: GIP/Source clock select.

SD_CLK_SEL[1:0](1)		Function	Note
0	0	DCLK	-
0	1	DCLK/2	Default
1	0	Reserved	-
1	1	Reserved	-

Note: (1) Set SD_CLK_SEL[1:0]=0x01 when F_{DCLK} >55Mhz.

BIST_FNUM[1:0]: BIST pattern refresh frame setting

BIST_FNUM[1:0]	Function	Note
00	32 frames	-
01	120 frames	Default
10	300 frames	-
11	6000 frames	-

R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	06h	1/0	VSTS[7:0]							
			0	0	0	0	1	0	0	0

VSTS[7:0]: Vertical back porch adjustment.

VSTS[7:0]								Function	Note
0	0	0	0	0	0	0	0	2H	-
0	0	0	0	0	0	0	1	2H	-
0	0	0	0	0	0	1	0	2H	-
0	0	0	0	0	0	1	1	3H	-
:	:	:	:	:	:	:	:	:	-
0	0	0	0	1	0	0	0	8H	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	255H	-

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R07h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	07h	1/0	HSTS[7:0]							
			0	0	0	1	0	0	0	0

HSTS[7:0]: Horizontal back porch adjustment.

HSTS[7:0]								Function	Note
0	0	0	0	0	0	0	0	5CLK	-
:	:	:	:	:	:	:	:	5CLK	-
0	0	0	0	0	1	0	1	5CLK	-
0	0	0	0	0	1	1	0	6CLK	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	0	0	0	0	16CLK	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	255CLK	-

R08h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	08h	1/0	PWR_SPEED	TS_RHL_OPT	OEW[5:0]					
			1	1	0	0	1	0	0	1

PWR_SPEED: speed power on enable.

PWR_SPEED	Function	Note
0	Speed power on to 3 frames	-
1	Normal power on **(4 frames)**	Default

TS_RHL_OPT: VGMPHS, VGMNHS,VGMPLS,VGMNLS,VGHS,VGLS,VCOM,AGAM select by register value load from OTP write flag or temperature mode.

TS_RHL_OPT	Function	Note
0	By temperature mode	-
1	By write flag	Default

OEW[5:0]: Timing for gate driver control. tOEV is the high pulse width of OEV which is the time that all gate channels are off between two lines. tOEV=OEW[5:0] * 8+2, and it should be smaller than 0.5*Hactive.

OEW[5:0]						Function	Note
0	0	0	0	0	0	26T(1)	-
:	:	:	:	:	:	26T(1)	-
0	0	0	0	1	1	26T(1)	-
0	0	0	1	0	0	34T(1)	
:	:	:	:	:	:	:	-
0	0	1	0	0	1	74T(1)	Default
:	:	:	:	:	:	:	-
1	1	1	1	1	1	506T(1)	-

Note: (1) The unit of T is decided by register SD_CLK_SEL.

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R09h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	09h	1/0	-	-	GEQW[5:0]					
			-	-	0	0	0	1	1	0

GEQW[5:0]: Timing for gate driver control. tGEQ is the time from the falling edge of CPV to the rising edge of OEV.
tGEQ = GEQW[5:0] * 4.

GEQW[5:0]						Function	Note
0	0	0	0	0	0	0T(1)	-
:	:	:	:	:	:	:	-
0	0	0	1	1	0	24T(1)	Default
:	:	:	:	:	:	:	-
1	1	1	1	1	1	252T(1)	-

Note: (1) T is the internal oscillator clock unit.

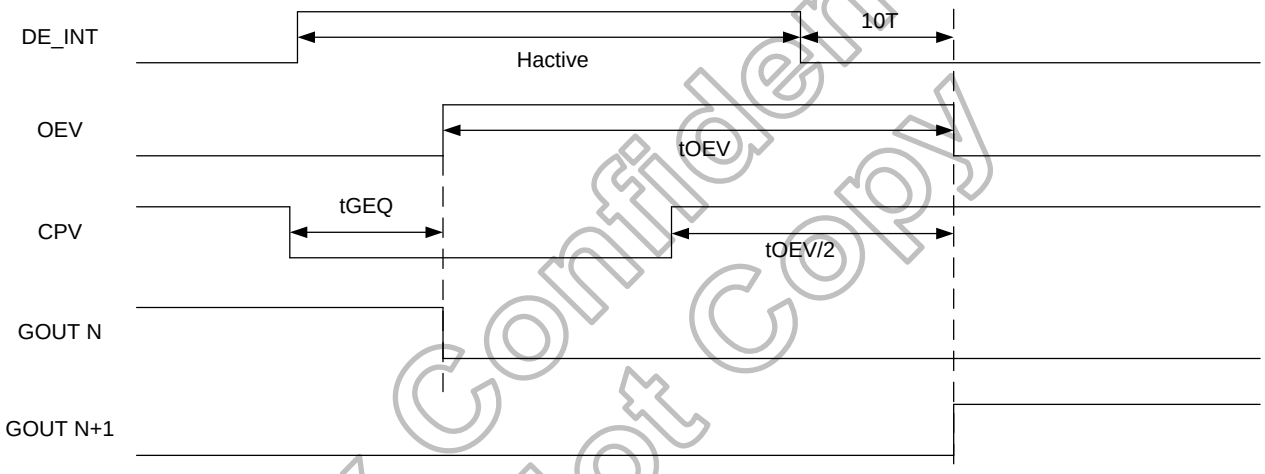

Figure 8.1: Gate control signals output

R0Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	0Ah	1/0	PCR[1:0]		EQ0W[5:0]					
			1	0	0	0	1	1	1	1

PCR[1:0]: Source SW divided selection.

PCR[1:0]		Function						Note
		tSW1	tSW2	tSW3	tSW4	tSW5	tSW6	
0	0	4T(1)	4T(1)	4T(1)	4T(1)	4T(1)	4T(1)	-
0	1	4T(1)	5T(1)	6T(1)	7T(1)	8T(1)	9T(1)	-
1	0	4T(1)	6T(1)	8T(1)	10T(1)	12T(1)	14T(1)	Default
1	1	4T(1)	8T(1)	12T(1)	16T(1)	20T(1)	24T(1)	-

Note: (1) The unit of T is decided by register SD_CLK_SEL.

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EQ0W[5:0]: Timing for source driver control. Source outputs are pulled to ground between each line if polarity changes and tEQ is the time pulling output to ground. tEQ0=EQ0W[5:0] *4T. It is suggested to set tEQ0 to 10%~20% of one line.

EQ0W[5:0](1)						Function	Note
0	0	0	0	0	0	4T(2)	-
:	:	:	:	:	:	:	-
0	0	0	0	1	1	12T(2)	-
:	:	:	:	:	:	:	-
0	0	1	1	1	1	60T(2)	Default
:	:	:	:	:	:	:	-
1	1	1	1	1	1	252T(2)	-

Note: (1) tEQ0 < Htotal - SD output time for MUX1:1.
tEQ0 < Htotal/2 - SD output time for MUX2:4.
tEQ0 < Htotal/3 - SD output time for MUX2:6.
(2) The unit of T is decided by register SD_CLK_SEL.

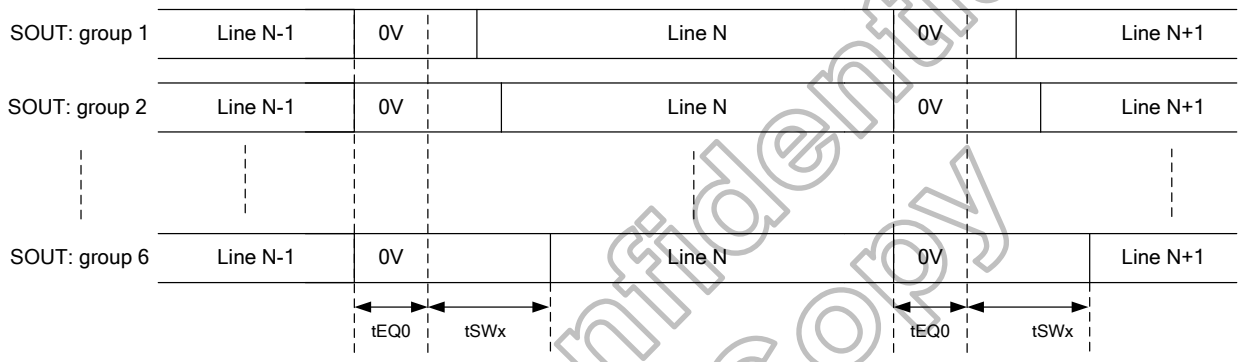

Figure 8.2: Source output timing

R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	0Bh	1/0	-	BC[2:0]			POCSD[1:0]		POCGM[1:0]	
			-	0	1	1	0	0	0	0

BC[2:0]: Source driver bias current selection.

BC[2:0]			Function	Note
0	0	0	40%	-
0	0	1	60%	-
0	1	0	80%	-
0	1	1	100%	Default
1	0	0	120%	-
1	0	1	140%	-
1	1	0	160%	-
1	1	1	180%	-

POCSD[1:0]: Source output offset cancelling selection.

POCSD[1:0]		Function	Note
0	0	Type 1	Default
0	1	Type 2	-
1	0	Type 3	-
1	1	Type 4	-

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POCGM[1:0]: Gamma offset cancelling selection.

POCGM[1:0]		Function	Note
0	0	Type 1	Default
0	1	Type 2	-
1	0	Type 3	-
1	1	Type 4	-

R0Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	0Ch	1/0	-	CAS_DEL_OPT[2:0]			RGATE	GM_SWAP	DUAL_F	TP_SYNC_VBLK
			-	0	0	0	0	0	0	0

CAS_DEL_OPT[2:0]: Sync the GIP signal between Master and Slave.
Delay the GIP signal of Master to sync the Slave.

CAS_DEL_OPT[2:0]			Function	Note
0	0	0	0T(1)	Default
:	:	:	:	-
0	1	1	3T(1)	-
:	:	:	:	-
1	1	1	7T(1)	-

Note: (1) The unit of T is decided by register SD_CLK_SEL.

RGATE: Interlace GATE swap

RGATE	Function	Note
0	L side: 1,3, 5; R side: 2, 4, 6	Default
1	L side: 2,4, 6; R side: 1, 3, 5	-

GM_SWAP: Gate line and color filter mapping selection. **(For dual gate)**

GM_SWAP	Function	Note
0	Normal	Default
1	Swap the gate line and color filter mapping	-

DUAL_F: Dual gate frame control. **(For dual gate)**

DUAL_F	Function	Note
0	Depend on GSEL[1:0]	Default
1	One Frame Z scan, another frame inv_Z scan	-

TP_SYNC_VBLK: TP_SYNC output toggle at vertical blanking.

TP_SYNC_VBLK	Function	Note
0	Disable	Default
1	Enable	-

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R0Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	0Dh	1/0	OSC_BISTS[1:0]		BISTS_CLK_SEL[1:0]		BIST_VFP[3:0]			
			1	0	0	0	0	0	0	0

OSC_BISTS[1:0]: Source/GIP clock selection in BIST mode.

OSC_BISTS[1:0]		Function	Note
0	0	70Mhz	-
0	1	60Mhz	-
1	0	50Mhz	Default
1	1	40Mhz	-

BISTS_CLK_SEL[1:0]: OSC_BISTS division. BIST_SD_CLK_SEL=2, means OSC_BISTS/2.

BIST_CLK_SEL[1:0]		Function	Note
0	0	1	Default
0	1	2	-
1	0	4	-
1	1	8	-

BIST_VFP[3:0]: Adjust vertical front porch of BIST mode.
VFPB = (BIST_VFP * 2 + 8)

BIST_VFP[3:0]				Function	Note
0	0	0	0	8H	Default
:	:	:	:	:	-
0	0	1	1	14H	-
:	:	:	:	:	-
1	1	1	1	38H	-

R0Eh ~ R10h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	0Eh	1/0	-	-	ROB[5:0]					
			-	-	0	1	0	0	0	0
	0Fh		-	-	GOB[5:0]					
			-	-	0	1	0	0	0	0
	10h		-	-	BOB[5:0]					
			-	-	0	1	0	0	0	0

ROB[5:0]/GOB[5:0]/BOB[5:0]: Offset **(brightness)** setting for red/green/blue color.
D brightness = D contrast + Offset
Offset= -16+ROB/GOB/BOB[5:0].

ROB[5:0] GOB[5:0] BOB[5:0]						Function	Note
0	0	0	0	0	0	-16	-
0	0	0	0	0	1	-15	-
:	:	:	:	:	:	:	-
0	1	0	0	0	0	0	Default
:	:	:	:	:	:	:	-
1	1	1	1	1	1	47	-

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R11h ~ R13h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	11h	1/0	RGC[7:0]							
			1	0	0	0	0	0	0	0
	12h		GGC[7:0]							
			1	0	0	0	0	0	0	0
	13h		BGC[7:0]							
			1	0	0	0	0	0	0	0

RGC[7:0]/GGC[7:0]/BGC[7:0]: Gain **(contrast)** setting for red / green / blue color.
D contrast = Din * Gain
Gain=0.5+RGC/GGC/BGC[7:0]/256.

RGC[7:0] GGC[7:0] BGC[7:0]								Function	Note
0	0	0	0	0	0	0	0	128/256 = 0.500	-
0	0	0	0	0	0	0	1	129/256 = 0.504	-
:	:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	0	256/256 = 1.000	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	383/256 = 1.496	-

R14h ~ R15h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	14h	1/0	GATENUM[7:0]							
			0	1	1	0	1	0	0	0
	15h		GATEPASS[3:0]				GATENUM[11:8]			
			1	0	1	0	0	0	0	1

GATEPASS[3:0]: Password to enable manual vertical resolution selection.

GATEPASS[3:0]				Function	Note
0	1	0	1	Enable	-
1	0	1	0	Disable	Default
Else				Disable	-

GATENUM[11:0]: Manual vertical resolution selection. It is effective only if GATEPASS[3:0] is set to 0101b. When manual vertical resolution selection is enabled, vertical resolution Vactive is set to GATENUM[11:0], where GATENUM[11:0]=80~4000 **(Vactive=80~4000)**.

GATENUM[11:0](1)												Function	Note
0	0	0	0	0	0	0	0	0	0	0	0	Reserved	-
:	:	:	:	:	:	:	:	:	:	:	:		-
0	0	0	0	0	1	0	0	1	1	1	1		-
0	0	0	0	0	1	0	1	0	0	0	0	Vactive=80	-
0	0	0	0	0	1	0	1	0	0	0	1	Vactive=81	-
:	:	:	:	:	:	:	:	:	:	:	:	:	-
0	0	0	1	0	1	1	0	1	0	0	0	Vactive=360	Default
:	:	:	:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	0	1	0	0	0	0	0	Vactive=4000	-
1	1	1	1	1	0	1	0	0	0	0	1	Reserved	-
:	:	:	:	:	:	:	:	:	:	:	:		-
1	1	1	1	1	1	1	1	1	1	1	1		-

Note: (1) For single gate: the Vtotal must be less than 4094 lines.
For dual gate/ MUX2: the Vtotal must be less than 2000 lines.
For triple gate/ MUX3: the Vtotal must be less than 1333 lines.
For dual gate: VRES should be even number.

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R16h ~ R17h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	16h	1/0	HSETNUM[7:0]							
			0	0	0	0	0	0	0	0
	17h		HSETPASS[3:0]				-	HSETNUM[10:8]		
			1	0	1	0	-	1	0	1

HSETPASS[3:0]: HSET_NUM_SEL function enables.

HSETPASS[3:0]				Function	Note
0	0	0	0	Disable	-
:	:	:	:	Disable	-
0	1	0	1	Enable	-
:	:	:	:	Disable	-
1	0	1	0	Disable	Default
:	:	:	:	Disable	-
1	1	1	1	Disable	-

HSETNUM[10:0]: Manual horizontal resolution selection. It is effective only if HSETPASS[3:0] is set to 0101b. When manual horizontal resolution selection is enabled, horizontal resolution Hactive is set to HSETNUM[10:0]. HSETNUM[10:0] must be multiple of 4. The Hactive setting range is HSETNUM[10:0] =240~3840.

HSETNUM[10:0]											Function	Note
0	0	0	0	0	0	0	0	0	0	0	Reserved	-
:	:	:	:	:	:	:	:	:	:	:		-
0	0	0	0	0	1	1	1	0	1	1		-
0	0	0	0	0	1	1	1	1	0	0	Hactive=240	-
0	0	0	0	0	1	1	1	1	0	1	Hactive=244	-
:	:	:	:	:	:	:	:	:	:	:	:	-
0	1	0	1	0	0	0	0	0	0	0	Hactive=1280	Default
:	:	:	:	:	:	:	:	:	:	:	:	-
0	1	1	1	1	0	0	0	0	0	0	Hactive=3840	-
0	1	1	1	1	0	0	0	0	0	1	Reserved	-
:	:	:	:	:	:	:	:	:	:	:		-
1	1	1	1	1	1	1	1	1	1	1		-

R18h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	07h	1/0	BIST_H_OFFSET[7:0]							
			0	0	0	0	0	0	0	0

BIST_H_OFFSET[7:0]: BIST mode H_width offset.

BIST_H_OFFSET [7:0]								Function	Note
0	0	0	0	0	0	0	0	0T(1)	Default
:	:	:	:	:	:	:	:	:	-
0	0	0	0	0	1	0	1	10T(1)	-
0	0	0	0	0	1	1	0	12T(1)	-
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	510T(1)	-

Note: (1) T is the OSC_BISTS/ BISTS_CLK_SEL.

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R19h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	19h	1/0	-	BIST_OSC_SEL	H_OSCLK_SEL[5:0]					
			-	0	0	0	1	1	1	1

BIST_OSC_SEL: Oscillator frequency selection for BIST.

BIST_OSC_SEL	Function	Note
0	Setting by HRES*VRES*60	Default
1	Setting by H_OSCLK_SEL	-

H_OSCLK_SEL[5:0]: Oscillator selection for BIST mode.

H_OSCLK_SEL[5:0]						Function	Note
0	0	0	0	0	0	85.0000MHz	-
0	0	0	0	0	1	80.0000MHz	-
0	0	0	0	1	0	75.0000MHz	-
0	0	0	0	1	1	70.0000MHz	-
0	0	0	1	0	0	65.0000MHz	-
0	0	0	1	0	1	57.0000MHz	-
0	0	0	1	1	0	50.0000MHz	-
0	0	0	1	1	1	42.0000MHz	-
0	0	1	0	0	0	42.5000MHz	-
0	0	1	0	0	1	40.0000MHz	-
0	0	1	0	1	0	37.5000MHz	-
0	0	1	0	1	1	35.0000MHz	-
0	0	1	1	0	0	32.5000MHz	-
0	0	1	1	0	1	28.5000MHz	-
0	0	1	1	1	0	25.0000MHz	-
0	0	1	1	1	1	21.0000MHz	Default
0	1	0	0	0	0	21.2500MHz	-
0	1	0	0	0	1	20.0000MHz	-
0	1	0	0	1	0	18.7500MHz	-
0	1	0	0	1	1	17.5000MHz	-
0	1	0	1	0	0	16.2500MHz	-
0	1	0	1	0	1	14.2500MHz	-
0	1	0	1	1	0	12.5000MHz	-
0	1	0	1	1	1	10.5000MHz	-
0	1	1	0	0	0	10.6250MHz	-
0	1	1	0	0	1	10.0000MHz	-
0	1	1	0	1	0	9.3750MHz	-
0	1	1	0	1	1	8.7500MHz	-
0	1	1	1	0	0	8.1250MHz	-
0	1	1	1	0	1	7.1250MHz	-
0	1	1	1	1	0	6.2500MHz	-
0	1	1	1	1	1	5.2500MHz	-
1	0	0	0	0	0	5.3125MHz	
1	0	0	0	0	1	5.0000MHz	
1	0	0	0	1	0	4.6875MHz	
1	0	0	0	1	1	4.3750MHz	
1	0	0	1	0	0	4.0625MHz	
1	0	0	1	0	1	3.5625MHz	
1	0	0	1	1	0	3.1250MHz	
1	0	0	1	1	1	2.6250MHz	
:	:	:	:	:	:	Reserved	

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R1Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	1Ch	1/0	POL_INV_FRM[3:0]				-	-	PRE_SCAN[1:0]	
			0	0	0	0	-	-	0	0

POL_INV_FRM[3:0]: Polarity change sequence method selection.
When the polarity change sequence inversion occurred, the VCOM has offset voltage continue one frame.

POL_INV_FRM[3:0]				Function	Note
0	0	0	0	Polarity change every frame	Default
0	0	0	1	Polarity change by 2 frames	-
0	0	1	0	Polarity change by 4 frames	-
0	0	1	1	Polarity change by 8 frames	-
:	:	:	:	:	-
1	0	1	0	Polarity change by 1024 frames	-
1	0	1	1	Polarity change by 2048 frames	-

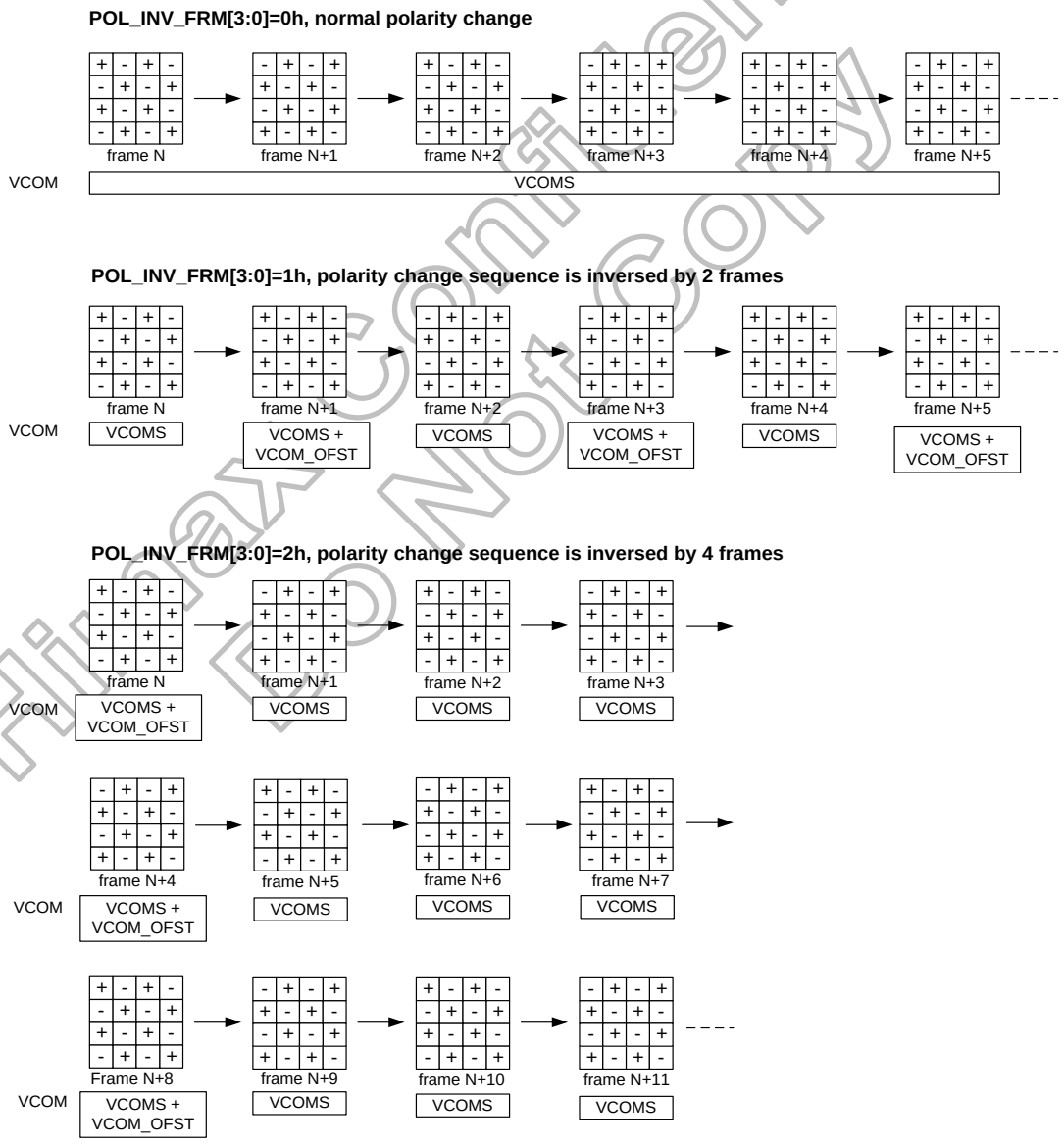

Figure 8.3: Polarity change sequence inversion

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PRE_SCAN[1:0]: Tradition Gate driver pre-scan mode select.

PRE_SCAN[1:0]		Function	Note
0	0	Normal gate **(disable pre-scan)**	Default
0	1	Gate Pre-scan md1(1)	-
1	0	Gate Pre-scan md2(2 **(Only support single gate mode)**	-
1	1		-

Note: (1) Pre-scan function only support Z-scan and Inv-Z scan in dual gate mode.
(2) Gate Pre-scan md2 vertical blanking timing limitation:

INV[1:0]		Single gate mode	Sync mode	DE mode
			t_{hbp} limitation	t_v-t_{vd} limitation
0	0	1 line dot inversion	≥4 H	≥8 H
0	1	1+2line dot inversion	≥4H	≥8 H
1	0	2+4line dot inversion	≥8H	≥16 H
1	1	Column inversion	≥4H	≥8 H

R1Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	1Dh	1/0	BIST_GRAY[7:0]							
			1	0	0	0	0	0	0	0

BIST_GRAY[7:0]: BIST mode gray scale pattern setting.

R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	1Eh	1/0	DMY_DATA[7:0]							
			1	0	0	0	0	0	0	0

DMY_DATA[7:0]: Source dummy data select for Zig-Zag type panel.

DMY_DATA[7:0]								Function	Note
0	0	0	0	0	0	0	0	0	-
:	:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	0	128	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	255	-

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8.2.3. Page01h for Power control function setting

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	01h	1/0	-	PFMFREN	VSPEN	VSNEN	DRVPD[1:0]		DRVND[1:0]	
			-	0	1	1	1	0	1	0

PFMFREN: PFM frequency randomizer enable.

PFMFREN	Function	Note
0	Disable	Default
1	Enable	-

VSPEN: VSP enable.

VSPEN	Function	Note
0	Disable	-
1	Enable	Default

VSNEN: VSN enable.

VSNEN	Function	Note
0	Disable	-
1	Enable	Default

DRVPD[1:0]: DRVP buffer size selection.

DRVPD[1:0]		Function	Note
0	0	25%	-
0	1	50%	-
1	0	100%	Default
1	1	150%	-

DRVND[1:0]: DRVN buffer size selection.

DRVND[1:0]		Function	Note
0	0	25%	-
0	1	50%	-
1	0	100%	Default
1	1	150%	-

R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	02h	1/0	VMONPS[1:0]		OCPEN	VSPS[4:0]				
			1	0	0	1	0	1	0	0

VMONPS[1:0]: PFM of VSP over current detection voltage selection.

VMONPS[1:0]		Function	Note
0	0	0.100V	-
0	1	0.125V	-
1	0	0.150V	Default
1	1	0.175V	-

OCPEN: PFM over current protection function enable.

OCPEN	Function	Note
0	Disable	Default
1	Enable	-

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VSPS[4:0]: VSP voltage selection, VSP=5V+VSPS[4:0] x 0.1V.

VSPS[4:0]					Function	Note
0	0	0	0	0	5.0V	-
0	0	0	0	1	5.1V	-
:	:	:	:	:	:	-
0	1	1	0	1	6.3V	-
:	:	:	:	:	:	-
1	0	0	1	1	6.9V	-
1	0	1	0	0	7.0V	Default
1	0	1	0	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	03h	1/0	VMONNS[1:0]		VCOM_OTP	VSNS[4:0]				
			1	0	0	1	0	1	0	0

VMONNS[1:0]: PFM of VSN over current detection voltage selection.

VMONNS[1:0]		Function	Note
0	0	0.100V	-
0	1	0.125V	-
1	0	0.150V	Default
1	1	0.175V	-

VCOM_OTP: VCOMS setting selection.

VCOM_OTP	Function	Note
0	If EEPEN=H, VCOMS from EEPROM	Default
1	VCOMS from OTP, doesn't matter EEPEN setting	-

VSNS[4:0]: VSN voltage selection, VSN = -5V-VSNS[4:0] x 0.1V.

VSNS[4:0]					Function	Note
0	0	0	0	0	-5.0V	-
0	0	0	0	1	-5.1V	-
:	:	:	:	:	:	-
0	1	1	0	1	-6.3V	-
:	:	:	:	:	:	-
1	0	0	1	1	-6.9V	-
1	0	1	0	0	-7.0V	Default
1	0	1	0	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

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Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	04h	1/0	-	VGHS[6:0]						
			-	0	0	1	1	1	0	0

VGHS[6:0]: VGH voltage selection, VGH=5+VGHS[6:0] x 0.25V.

VGHS[6:0](1)							Function	Note
0	0	0	0	0	0	0	5.00V	-
0	0	0	0	0	0	1	5.25V	-
0	0	0	0	0	1	0	5.50V	-
:	:	:	:	:	:	:	:	-
0	0	1	1	1	0	0	12.00V	Default
:	:	:	:	:	:	:	:	-
1	0	0	1	0	1	1	23.75V	-
1	0	0	1	1	0	0	24.00V	-
1	0	0	1	1	0	1	24.00V	-

Note: (1) VGH + |VGL| < 32V.
VGH > VSP.

R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	05h	1/0	-	VGLXS	VGLS[5:0]					
			-	0	0	0	1	1	0	0

VGLXS: VGL boosting mode selection.

VGLXS	Function	Note
0	2X	Default
1	3X	-

VGLS[5:0]: VGL voltage selection, VGL=-5-VGLS[5:0] x 0.25V.

VGLS[5:0] (1)						Function	Note
0	0	0	0	0	0	-5.00V	-
0	0	0	0	1	0	-5.25V	-
:	:	:	:	:	:	:	-
0	0	1	0	1	1	-7.75V	-
0	0	1	1	0	0	-8.00V	Default.
0	0	1	1	0	1	-8.25V	-
:	:	:	:	:	:	:	-
1	0	1	1	0	0	-16.00V	-
:	:	:	:	:	:	Reserved	-
1	1	1	1	1	1	Reserved	-

Note: (1) VGH + |VGL| < 32V.
|VGL| > |VSN|.

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R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	06h	1/0	VSPON[4]	VSNON[4]	POFF_GAS_EN	VSDPS[4:0]				
			0	0	0	1	0	1	0	0

VSPON[4] : refer to Page01h/ R08h[7:4]

VSNON[4]: refer to Page01h/ R07h[7:4]

POFF_GAS_EN: GAS function during power off function enable.

POFF_GAS_EN	Function	Note
0	Disable	Default
1	Enable	-

VSDPS[4:0]: VSDP voltage selection, VSDP = 4.8V+VSDPS[4:0] x 0.1V.

VSDPS[4:0]					Function	Note
0	0	0	0	0	4.8V	-
0	0	0	0	1	4.9V	-
:	:	:	:	:	:	-
0	1	1	0	0	6.0V	-
:	:	:	:	:	:	-
1	0	0	1	1	6.7V	-
1	0	1	0	0	6.8V	Default
1	0	1	0	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

R07h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	07h	1/0	-	-	CAS_VGHL_OPT	VSDNS[4:0]				
			-	-	0	1	0	1	0	0

CAS_VGHL_OPT: VGH/VGL power on sequence between master and slave.

CAS_VGHL_OPT	Function	Note
0	Slave delay, master normal when cascade	Default
1	Slave normal , master delay when cascade	-

VSDNS[4:0]: VSDN voltage selection, VSDN = -4.8V-VSDNS[4:0] x 0.1V.

VSDNS[4:0]					Function	Note
0	0	0	0	0	-4.8V	-
0	0	0	0	1	-4.9V	-
:	:	:	:	:	:	-
0	1	1	0	0	-6.0V	-
:	:	:	:	:	:	-
1	0	0	1	1	-6.7V	-
1	0	1	0	0	-6.8V	Default
1	0	1	0	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

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R08h ~ R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	08h	1/0	VSPON[3:0]				VSPOFF[3:0]			
			0	1	0	1	0	1	0	1
	09h		VSNON[3:0]				VSNOFF[3:0]			
			0	1	0	1	0	1	0	1
	0Ah		VSPON_SS2[3:0]				VSPOFF_SS2[3:0]			
			0	1	0	0	1	1	1	1
	0Bh		VSNON_SS2[3:0]				VSNOFF_SS2[3:0]			
			1	0	0	0	1	0	1	0

VSPON[4:0] / VSNON[4:0]: PFM turn on duty of DRVP **(tONP)**/DRVN **(tONN)** at normal operation.(VSPON[4] in Page01h/ R06h[7], VSNON[4] in Page01h/ R06h[6])

VSPON[4:0]					Function	Note
0	0	0	0	0	tPFM * 2	-
:	:	:	:	:	:	-
0	0	1	0	1	tPFM * 7	Default
:	:	:	:	:	:	-
0	1	1	1	1	tPFM * 17	-
:	:	:	:	:		
1	1	1	1	1	tPFM * 33	

VSNON[4:0]					Function	Note
0	0	0	0	0	tPFM * 2	-
:	:	:	:	:	:	-
0	0	1	0	1	tPFM * 7	Default
:	:	:	:	:	:	-
0	1	1	1	1	tPFM * 17	-
:	:	:	:	:		
1	1	1	1	1	tPFM * 33	

VSPOFF[3:0]/VSNOFF[3:0]: PFM turn off duty of DRVP **(tOFFP)**/DRVN **(tOFFP)** at normal operation. Also note that low state will be larger than setting if VSP/VSN already reaches **(higher than)** the target.

VSPOFF[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	1	0	1	tPFM * 7	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

VSNOFF[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	1	0	1	tPFM * 7	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

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VSPON_SS2[3:0]/VSNON_S[3:0]: PFM turn on duty of DRVP **(tONP)**/DRVN **(tONN)** at soft start SS2 period of power on sequence.

VSPON_SS2[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	1	0	0	tPFM * 6	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

VSNON_SS2[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
1	0	0	0	tPFM * 10	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

VSPOFF_SS2[3:0]/VSNOFF_SS2[3:0]: PFM turn off duty of DRVP **(tOFFP)** /DRVN **(tOFFP)** at soft start SS2 period of power on sequence. Also note that low state will be larger than setting if VSP/VSN already reaches **(higher than)** the target.

VSPOFF_SS2[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
1	1	1	0	tPFM * 16	-
1	1	1	1	tPFM * 17	Default

VSNOFF_SS2[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
1	0	1	0	tPFM * 12	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

R0Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	0Ch	1/0	GAS_VCC_EN	VGHXS[1:0]		VCOMEN	S_VCL_ENB	M_VCL_ENB	VCOMD[1:0]	
			1	0	1	1	0	0	0	1

GAS_VCC_EN: GAS detect VCC1 enable.

GAS_VCC_EN	Function	Note
0	Disable	-
1	Enable	Default

VGHXS[1:0]: select VGH boosting mode.

VGHXS[1:0]		Function	Note
0	0	2X	-
0	1	3X	Default
1	0	4X	-
1	1	4X	-

VCOMEN: VCOM regulator enable.

VCOMEN	Function	Note
0	Disable	-
1	Enable	Default

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S_VCL_ENB: Slave chip VCL regulator enable.

S_VCL_ENB	Function	Note
0	Enable	Default
1	Disable	-

M_VCL_ENB: Master chip VCL regulator enable.

M_VCL_ENB	Function	Note
0	Enable	Default
1	Disable	-

VCOMD[1:0]: VCOM driving capability selection.

VCOMD[1:0]		Function	Note
0	0	50%	-
0	1	100%	Default
1	0	150%	-
1	1	200%	-

R0Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	0Dh	1/0	VGHL_LIMIT	VGHEN	VGLEN	-	PFM_SS_SEL	POL_TOG_VBLK	FCP[1:0]	
			1	1	1	-	0	0	1	1

VGHL_LIMIT: Auto setting for (VGH + |VGL| ≦ 32).

VGHL_LIMIT	Function	Note
0	Disable	-
1	VGH + |VGL| ≦ 32	Default

VGHEN: VGH charge pump circuit enable.

EXT_PWR2	VGHEN	Function	Note
L	0	Disable	-
L	1	Enable	Default
H	0	Disable	-
H	1	Disable	-

VGLEN: VGL charge pump circuit enable.

EXT_PWR2	VGLEN	Function	Note
L	0	Disable	-
L	1	Enable	Default
H	0	Disable	-
H	1	Disable	-

PFM_SS_SEL: PFM SSC enable.

PFM_SS_SEL	Function	Note
0	Disable	Default
1	Enable	-

POL_TOG_VBLK: POL keep toggle at vertical blanking.

POL_TOG_VBLK	Function	Note
0	Disable	Default
1	Enable	-

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FCP[1:0]: VGH and VGL charge pump frequency setting.

FCP[1:0]		Function	Note
0	0	1 CPCLK / 2HS	-
0	1	1 CPCLK / HS	-
1	0	2 CPCLK / HS	-
1	1	4 CPCLK / HS	Default

R0Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	0Eh	1/0	GAS_VGL_EN	-	T_VGMREGEN	VGMPHS[4:0]				
			1	-	1	1	1	0	1	0

GAS_VGL_EN: GAS detect VGL enable.

GAS_VGL_EN	Function	Note
0	Disable	-
1	Enable	Default

T_VGMREGEN: VGMPH/LO and VGMNH/LO regulators enable.

T_VGMREGEN	Function	Note
0	Disable	-
1	Enable	Default

VGMPHS[4:0]: VGMPHO voltage selection, VGMPHO=4+T_VGMPHS[4:0] x 0.1V.

VGMPHS[4:0]					Function	Note
0	0	0	0	0	4.0V	-
0	0	0	0	1	4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	5.8V	-
:	:	:	:	:	:	-
1	1	0	0	1	6.5V	-
1	1	0	1	0	6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

R0Fh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	0Fh	1/0	GASVCIS[2:0]			VGMNHS[4:0]				
			0	1	0	1	1	0	1	0

GASVCIS[2:0]: VCC1 GAS voltage selection.

GASVCIS[2:0]			Function	Note
0	0	0	2.2V	-
0	0	1	2.3V	-
0	1	0	2.4V	Default
0	1	1	2.5V	-
1	0	0	2.6V	-
1	0	1	2.7V	-
1	1	0	2.8V	-
1	1	1	2.9V	-

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VGMNHS[4:0]: VGMNHO voltage selection, VGMNHO= -4 -T_VGMNHS[4:0] x 0.1V.

T_VGMNHS[4:0]					Function	Note
0	0	0	0	0	-4.0V	-
0	0	0	0	1	-4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	-5.8V	-
:	:	:	:	:	:	-
1	1	0	0	1	-6.5V	-
1	1	0	1	0	-6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

R10h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	10h	1/0	VGMPLS[3:0]				VGMNLS[3:0]			
			0	0	0	1	0	0	0	1

VGMPLS[3:0]: VGMPLO voltage selection, VGMPLO= 0.1+T_VGMPLS[3:0] x 0.1V.

VGMPLS[3:0]				Function	Note
0	0	0	0	0.1V	-
0	0	0	1	0.2V	Default
0	0	1	0	0.3V	-
:	:	:		:	-
1	0	0	0	0.9V	-
:	:	:		:	-
1	1	1	0	1.5V	-
1	1	1	1	1.6V	-

VGMNLS[3:0]: VGMNLO voltage selection, VGMNLO= -0.1-T_VGMNLS[3:0] x 0.1V.

VGMNLS[3:0]				Function	Note
0	0	0	0	-0.1V	-
0	0	0	1	-0.2V	Default
0	0	1	0	-0.3V	-
:	:	:		:	-
1	0	0	0	-0.9V	-
:	:	:		:	-
1	1	1	0	-1.5V	-
1	1	1	1	-1.6V	-

R11h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	11h	1/0	DCHG2R[1:0]		DCHG2ON[1:0]		DCHG1R[1:0]		DCHG1ON[1:0]	
			1	0	1	0	1	0	1	0

DCHG2R[1:0]: VGH2 dis-charge resistance selection.

DCHG2R[1:0]		Function	Note
0	0	1K+ext	-
0	1	20K	-
1	0	40K	Default
1	1	60K	-

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DCHG2ON[1:0]:

DCHG2ON[1:0]		Function	Note
0	0	Gas off disable DCHG2R function **(0.5k)**, and Normal off disable DCHG2R function **(0.5K)**	-
0	1	Gas off disable DCHG2R function **(0.5k)**, and Normal off enable DCHG2R function	-
1	0	Gas off enable DCHG2R function, and Normal off disable DCHG2R function **(0.5K)**	Default
1	1	Gas off enable DCHG2R function, and Normal off enable DCHG2R function	-

DCHG1R[1:0]: VGH1 dis-charge resistance selection.

DCHG1R[1:0]		Function	Note
0	0	1.0K+ext	-
0	1	0.5K	-
1	0	1.5K	Default
1	1	2.0K	-

DCHG1ON[1:0]:

DCHG1ON[1:0]		Function	Note
0	0	Gas off disable DCHG1R function **(0.5K)**, and Normal off disable DCHG1R function **(0.5K)**	-
0	1	Gas off disable DCHG1R function **(0.5K)**, and Normal off enable DCHG1R function	-
1	0	Gas off enable DCHG1R function, and Normal off disable DCHG1R function **(0.5K)**	Default
1	1	Gas off enable DCHG1R function, and Normal off enable DCHG1R function	-

R12h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	12h	1/0	POFF_BLACK_OPT	POFF_BLACK_NUM	PON_BLACK_NUM[1:0]		HT_POL_OPT	VCLS[2:0]		
			0	1	0	1	0	1	0	0

POFF_BLACK_OPT: Power off black frame numbers.

POFF_BLACK_OPT	Function	Note
0	Power off black frame by POFF_BLACK_NUM setting	Default
1	2 frames	-

POFF_ BLACK_NUM: Power off black frame numbers.

POFF_ BLACK_NUM	Function	Note
0	0 frame	-
1	1 frame	Default

PON_ BLACK_NUM[1:0]: Power on black frame numbers.

PON_ BLACK_NUM[1:0]		Function	Note
0	0	0 frame	-
0	1	1 frame	Default
1	0	2 frames	-
1	1	X	-

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HT_POL_OPT:

HT_POL_OPT	Function	Note
0	POL inversion not change at HT	Default
1	Force Column inversion at OH	-

VCLS[2:0]: Select VCL level.

VCLS[2:0]			Function	Note
0	0	0	-2.125V	-
0	0	1	-2.250V	-
0	1	0	-2.375V	-
0	1	1	-2.500V	-
1	0	0	-2.625V	Default
1	0	1	-2.750V	-
1	1	0	-2.875V	-
1	1	1	-3.000V	-

R13h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	13h	1/0	GD_OEV_OFF	-	LTPS_GIP_PWR_OPT	LOAD_OPT	-	-	TFVBAT1[1:0]	
			0	-	0	0	-	-	0	0

GD_OEV_OFF:

GD_OEV_OFF	Function	Note
0	Normal OEW function	Default
1	Tradition gate OEV keep low **(Not support interlace scan)**	-

LTPS_GIP_PWR_OPT: GIP and LTPS signal level in power on period.

LTPS_GIP_PWR_OPT	Function	Note
0	VGL	Default
1	GND	-

LOAD_OPT: Panel loading option.

LOAD_OPT	Function	Note
0	Normal loading	Default
1	Light loading	-

TFVBAT1[1:0]: GIP signal with VGH1 level setting in abnormal power off sequence.

TFVBAT1[1:0]		Function	Note
0	0	0μs	-
0	1	10μs	Default
1	0	20μs	-
1	1	30μs	-

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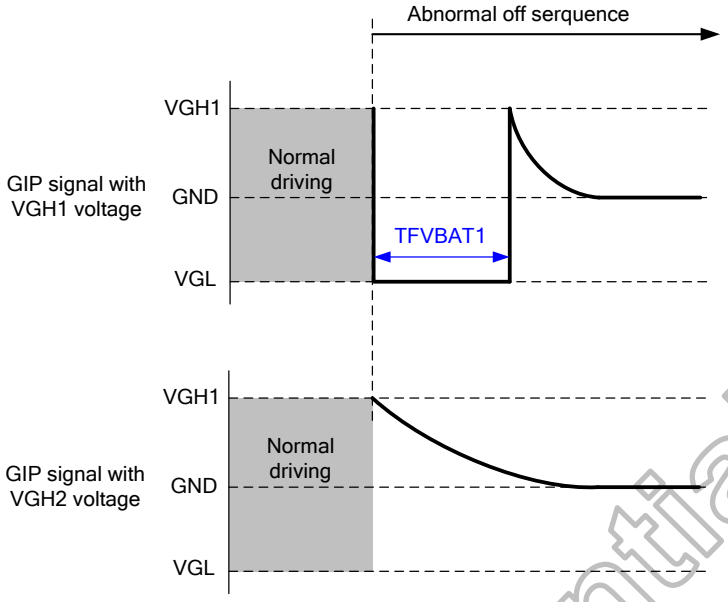

R14h ~ R15h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	14h	1/0	VSPON_SS1[3:0]				VSPOFF_SS1[3:0]			
			0	0	0	1	1	1	1	1
	15h		VSNON_SS1[3:0]				VSNOFF_SS1[3:0]			
			0	0	1	0	1	1	1	1

VSPON_SS1[3:0]/VSNON_SS1[3:0]: PFM turn on duty of DRVP **(tONP)**/DRVN **(tONN)** at soft start SS1 period of power on sequence.

VSPOFF_SS1[3:0]/VSNOFF_SS1[3:0]: PFM turn off duty of DRVP **(tOFFP)** /DRVN **(tOFFP)** at soft start SS1 period of power on sequence. Also note that low state will be larger than setting if VSP/VSN already reaches **(higher than)** the target.

PTSEL[15:0]: BIST pattern selection.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	18h	1/0	PTSEL[15:8]							
			1	1	1	1	1	1	1	1
	19h		PTSEL[7:0]							
			1	1	1	1	1	1	1	1

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PTSEL[15:0]																Function	Note
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	White boarder pattern selected	-
-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	VCOM trimming pattern selected	-
-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	H Gray scale 256 pattern selected	-
-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	V Gray scale 256 pattern selected	-
-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	BIST Gray level pattern selected	-
-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	Gray Scale 16 pattern selected	-
-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	Checker board pattern selected	-
-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	Cross talk2 pattern selected	-
-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	Cross talk1 pattern selected	-
-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	H Gomi2 pattern selected	-
-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	H Gomi1 pattern selected	-
-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	Full Blue pattern selected	-
-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	Full Green pattern selected	-
-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	Full Red pattern selected	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	Full White pattern selected	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	Full Black pattern selected	-

R1Ah ~ R1Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	1Ah	1/0	-	-	-	-	-	-	-	OFF_VCOM[8]
			-	-	-	-	-	-	-	1
01h	1Bh	1/0	OFF_VCOM[7:0]							
			0	1	0	1	1	1	0	0

OFF_VCOM[8:0]: VCOM voltage in power off sequence selection.
VCOM= 2 + VCOMS[8:0] x (-0.01V)

VCOMS[8:0]									Function	Note
0	0	0	0	0	0	0	0	0	2.00V	-
0	0	0	0	0	0	0	0	1	1.99V	-
:	:	:	:	:	:	:	:	:	:	-
1	0	1	0	1	1	1	0	0	-1.48V	Default
:	:	:	:	:	:	:	:	:	:	-
1	1	1	0	0	0	0	1	0	-2.50V	-
1	1	1	0	0	0	0	1	1	Reserved	-
:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	1	Reserved	-

R1Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	1Ch	1/0	VCOM_OFST[7:0]							
			0	0	0	0	0	0	0	0

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VCOM_OFST[7:0]: VCOM voltage offset setting.
When the polarity change sequence inversion occurred, the VCOM has offset voltage continue one frame. The function is enabled when POL_INV_FRM≠0h (**Page00h R16h[7:4]**).
VCOM= 2 + (VCOMS[8:0] + VCOM_OFST[6:0]) x (-0.01V) when VCOM_OFST[7] = 0.
VCOM= 2 + (VCOMS[8:0] - VCOM_OFST[6:0]) x (-0.01V) when VCOM_OFST[7] = 1.

VCOM_OFST[7:0]								Function	Note
0	0	0	0	0	0	0	0	VCOM offset + 0	Default
0	0	0	0	0	0	0	1	VCOM offset + 1	-
:	:	:	:	:	:	:	:	:	-
:	:	:	:	:	:	:	:	:	-
0	1	1	1	1	1	1	1	VCOM offset + 127	-
1	0	0	0	0	0	0	0	VCOM offset - 0	-
:	:	:	:	:	:	:	:	:	-
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	0	VCOM offset - 126	-
1	1	1	1	1	1	1	1	VCOM offset - 127	-

R1Dh ~ R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	1Dh	1/0	-	-	-	-	-	-	-	VCOMS[8]
			-	-	-	-	-	-	-	1
01h	1Eh	1/0	VCOMS[7:0]							
			0	1	0	1	1	1	0	0

VCOMS[8:0]: VCOM voltage selection.
VCOM= 2 + VCOMS[8:0] x (-0.01V)

VCOMS[8:0]									Function	Note
0	0	0	0	0	0	0	0	0	2.00V	-
0	0	0	0	0	0	0	0	1	1.99V	-
:	:	:	:	:	:	:	:	:	:	-
1	0	1	0	1	1	1	0	0	-1.48V	Default
:	:	:	:	:	:	:	:	:	:	-
1	1	1	0	0	0	0	1	0	-2.50V	-
1	1	1	0	0	0	0	1	1	Reserved	-
:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	1	Reserved	-

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8.2.4. Page02h for Positive analog gamma, PAGM

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
	01h		-	-	-	T_VP0[4:0]				
			-	-	-	0	0	0	0	0
	02h		-	-	T_VP2[5:0]					
			-	-	0	0	0	1	0	0
	03h		-	-	T_VP4[5:0]					
			-	-	0	0	1	0	0	0
	04h		-	-	T_VP8[5:0]					
			-	-	0	1	1	0	0	0
	05h		-	-	T_VP14[5:0]					
			-	-	1	0	0	0	1	1
	06h		-	-	T_VP22[5:0]					
			-	-	0	1	0	0	1	0
	07h		-	-	T_VP30[5:0]					
			-	-	0	1	0	0	0	1
	08h		-	-	T_VP47[5:0]					
			-	-	0	1	0	1	1	1
	09h		-	-	T_VP79[5:0]					
			-	-	1	0	0	0	0	0
	0Ah		-	-	T_VP111[5:0]					
			-	-	1	0	0	0	1	1
	0Bh		-	-	T_VP143[5:0]					
			-	-	1	0	0	1	1	0
	0Ch		-	-	T_VP175[5:0]					
			-	-	1	0	1	0	1	1
	0Dh		-	-	T_VP207[5:0]					
			-	-	1	0	0	1	0	1
	0Eh		-	-	T_VP224[5:0]					
			-	-	1	0	0	1	0	1
	0Fh		-	-	T_VP232[5:0]					
			-	-	1	1	0	1	0	1
	10h		-	-	T_VP240[5:0]					
			-	-	1	1	0	0	0	0
	11h		-	-	T_VP246[5:0]					
			-	-	1	0	0	1	0	0
	12h		-	-	T_VP251[5:0]					
			-	-	1	1	0	0	0	1
	13h		-	-	T_VP253[5:0]					
			-	-	1	1	1	0	0	0
	14h		-	-	-	T_VP255[4:0]				
			-	-	-	1	1	1	1	0
	15h		P_checksum[7:0]							
			0	0	0	0	0	0	0	0

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Reg name	Setting value								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
T_VP0[4:0]	-	-	-	0	0	0	0	0	Positive gamma reference “GSH0” selection.
	-	-	-	:	:	:	:	:	
	-	-	-	1	1	1	1	1	
T_VP2[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH2” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP4[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH4” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP8[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH8” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP14[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH14” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP22[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH22” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP30[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH30” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP47[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH47” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP79[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH79” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP111[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH111” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP143[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH143” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP175[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH175” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP207[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH207” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP224[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH224” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP232[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH232” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP240[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH240” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP246[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH246” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP251[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH251” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	

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Reg name	Setting value								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
T_VP253[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH253” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP255[4:0]	-	-	-	0	0	0	0	0	Positive gamma reference “GSH255” selection.
	-	-	-	:	:	:	:	:	
	-	-	-	1	1	1	1	1	

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8.2.5. Page03h for Negative analog gamma, NAGM

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
	01h		-	-	-	T_VN0[4:0]				
			-	-	-	0	0	0	0	0
	02h		-	-	T_VN2[5:0]					
			-	-	0	0	0	1	0	0
	03h		-	-	T_VN4[5:0]					
			-	-	0	0	1	0	0	0
	04h		-	-	T_VN8[5:0]					
			-	-	0	1	1	0	0	0
	05h		-	-	T_VN14[5:0]					
			-	-	1	0	0	0	1	1
	06h		-	-	T_VN22[5:0]					
			-	-	0	1	0	0	1	0
	07h		-	-	T_VN30[5:0]					
			-	-	0	1	0	0	0	1
	08h		-	-	T_VN47[5:0]					
			-	-	0	1	0	1	1	1
	09h		-	-	T_VN79[5:0]					
			-	-	1	0	0	0	0	0
	0Ah		-	-	T_VN111[5:0]					
			-	-	1	0	0	0	1	1
	0Bh		-	-	T_VN143[5:0]					
			-	-	1	0	0	1	1	0
	0Ch		-	-	T_VN175[5:0]					
			-	-	1	0	1	0	1	1
	0Dh		-	-	T_VN207[5:0]					
			-	-	1	0	0	1	0	1
	0Eh		-	-	T_VN224[5:0]					
			-	-	1	0	0	1	0	1
	0Fh		-	-	T_VN232[5:0]					
			-	-	1	1	0	1	0	1
	10h		-	-	T_VN240[5:0]					
			-	-	1	1	0	0	0	0
	11h		-	-	T_VN246[5:0]					
			-	-	1	0	0	1	0	0
	12h		-	-	T_VN251[5:0]					
			-	-	1	1	0	0	0	1
	13h		-	-	T_VN253[5:0]					
			-	-	1	1	1	0	0	0
	14h		-	-	-	T_VN255[4:0]				
			-	-	-	1	1	1	1	0
	15h		N_checksum[7:0]							
			0	0	0	0	0	0	0	0

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Reg name	Setting value								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
T_VN0[4:0]	-	-	-	0	0	0	0	0	Negative gamma reference “GSL0” selection.
	-	-	-	:	:	:	:	:	
	-	-	-	1	1	1	1	1	
T_VN2[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL2” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN4[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL4” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN8[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL8” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN14[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL14” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN22[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL22” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN30[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL30” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN47[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL47” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN79[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL79” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN111[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL111” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN143[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL143” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN175[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL175” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN207[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL207” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN224[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL224” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN232[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL232” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN240[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL240” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN246[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL246” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN251[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL251” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	

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Reg name	Setting value								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
T_VN253[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL253” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN255[4:0]	-	-	-	0	0	0	0	0	Negative gamma reference “GSL255” selection.
	-	-	-	:	:	:	:	:	
	-	-	-	1	1	1	1	1	

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8.2.6. Page04h for Fail flag function setting

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	01h	1/0	FAIL_DET_SEL	FAIL_DET_INV	ASIL_PRIOR_SEL	ASIL_NOSIG_SEL	ASIL_INV	ASIL_WD[2:0]		
			1	0	0	0	0	1	0	0

FAIL_DET_SEL: FAIL_DET output signal selection.

FAIL_DET_SEL	Function	Note
0	Fail flag output to FAIL_DET	-
1	ASIL signal output to FAIL_DET	Default

FAIL_DET_INV: FAIL_DET output signal inverse.

FAIL_DET_INV	Function	Note
0	Normal **(FAIL_DET output low when failure occur)**	Default
1	Inverse	-

ASIL_PRIOR_SEL: FAIL_DET detect signal priority selection.

ASIL_PRIOR_SEL	Function	Note
0	Abnormal > NO CLK	Default
1	NO CLK > abnormal	-

ASIL_NOSIG_SEL: No signal define for ASIL.

ASIL_NOSIG_SEL	Function	Note
0	Only no clock, ASIL output 40Hz pulse.	Default
1	No clock / DE **(DE mode)** / HS/VS **(SYNC mode)**, ASIL output 40Hz pulse.	-

ASIL_INV: ASIL output inverse enable.

ASIL_INV	Function	Note
0	Disable	Default
1	Enable	-

ASIL_WD[2:0]: ASIL signal pulse width selection.
When ASIL output 60 Hz signal **(same as frame rate)**, ASIL pulse width **(WD)** selection.

ASIL_WD[2:0]			Function	Note
0	0	0	2H	-
0	0	1	2H	-
0	1	0	4H	-
0	1	1	6H	-
1	0	0	8H	Default
1	0	1	10H	-
1	1	0	12H	-
1	1	1	14H	-

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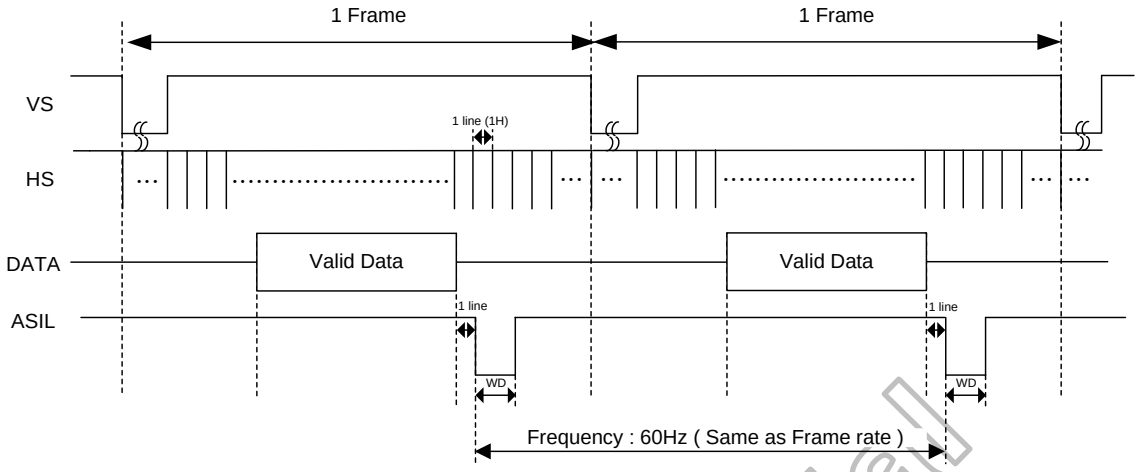
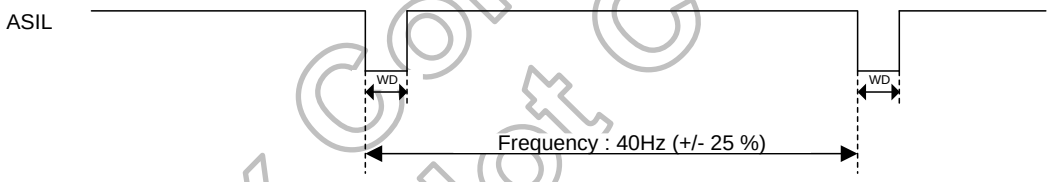


When ASIL output 40 Hz signal **(+/-25%)**, ASIL pulse width **(WD)** selection.

ASIL_WD[2:0]			Function	Note
0	0	0	100μs	-
0	0	1	100μs	-
0	1	0	200μs	-
0	1	1	300μs	-
1	0	0	400μs	Default
1	0	1	500μs	-
1	1	0	600μs	-
1	1	1	700μs	-



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R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	02h	1/0	-	-	SD_DET_EN	PON_FDET_EN	CRC4_FAIL_ENB	CRC3_FAIL_ENB	CRC2_FAIL_ENB	CRC1_FAIL_ENB
			-	-	1	1	1	1	1	1

SD_DET_EN: Enable source_R/L block self detect function.

SD_DET_EN	Function	Note
0	Disable	-
1	Enable	Default

PON_FDET_EN: Power on fail detect test enable.

PON_FDET_EN	Function	Note
0	Disable	-
1	Enable	Default

CRC4_FAIL_ENB: CRC 4th window fail flag output to FAIL_DET pin.

CRC4_FAIL_ENB	Function	Note
0	Enable	-
1	Disable	Default

CRC3_FAIL_ENB: CRC 3rd window fail flag output to FAIL_DET pin.

CRC3_FAIL_ENB	Function	Note
0	Enable	-
1	Disable	Default

CRC2_FAIL_ENB: CRC 2nd window fail flag output to FAIL_DET pin.

CRC2_FAIL_ENB	Function	Note
0	Enable	-
1	Disable	Default

CRC1_FAIL_ENB: CRC 1st window fail flag output to FAIL_DET pin.

CRC1_FAIL_ENB	Function	Note
0	Enable	-
1	Disable	Default

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R03h

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	03h	1/0	PFM_NG_ENB	OTP_TRIM_ FAIL_ENB	EEPROM_ FAIL_ENB	NO_VIDEO_ FAIL_ENB	GATE_F_ FAIL_ENB	SOURCE_ FAIL_ENB	OTP_FULL_FAIL_ENB	LVDS_ FAIL_ENB
			0	0	0	0	0	0	0	0

PFM_NG_ENB: PFM abnormal flag output to FAIL_DET pin.

PFM_NG_ENB	Function	Note
0	Enable	Default
1	Disable	-

OTP_TRIM_FAIL_ENB: OTP program fail flag output to FAIL_DET pin.

OTP_TRIM_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

EEPROM_FAIL_ENB: EEPROM reload fail flag output to FAIL_DET pin.

EEPROM_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

NO_VIDEO_FAIL_ENB: Self-protection mode fail flag output to FAIL_DET pin.

NO_VIDEO_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

GATE_FAIL_ENB: Tradition gate signal fail flag output to FAIL_DET pin.

GATE_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

SOURCE_FAIL_ENB: Internal source circuit fail flag output to FAIL_DET pin.

SOURCE_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

OTP_FULL_FAIL _ENB: OTP program time full fail flag output to FAIL_DET pin.

POWER_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

LVDS_FAIL_ENB: LVDS lock fail flag output to FAIL_DET pin.

LVDS_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

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R04h

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	04h	1/0	GAS_VGL_ENB	GAS_PFM_FAIL_ENB	GAS_VCC_FAIL_ENB	SLV_VCOM_DET_ENB	OTP_CKSUM_FAIL2_ENB	OTP_CHKSUM_FAIL_ENB	OTP_RL_FAIL_ENB	SLV_GAM_DET_ENB
			1	0	0	1	1	1	0	1

GAS_VGL_ENB: GAS of VGL fail flag output to FAIL_DET pin.

GAS_VGL_ENB	Function	Note
0	Enable	Default
1	Disable	-

GAS_PFM_ENB: GAS of PFM fail flag output to FAIL_DET pin.

GAS_PFM_ENB	Function	Note
0	Enable	Default
1	Disable	-

GAS_VCC_ENB: GAS of VCC fail flag output to FAIL_DET pin.

GAS_VCC_ENB	Function	Note
0	Enable	Default
1	Disable	-

SLV_VCOM_DET_ENB: Slave VCOM fail flag output to FAIL_DET pin.

SLV_VCOM_ENB	Function	Note
0	Enable	-
1	Disable	Default

OTP_CKSUM_FAIL2_ENB: Gamma P/N table OTP checksum fail flag output to FAIL_DET pin.

OTP_CKSUM_FAIL2_ENB	Function	Note
0	Enable	-
1	Disable	Default

OTP_CKSUM_FAIL_ENB: OTP checksum fail flag output to FAIL_DET pin.

OTP_CKSUM_FAIL_ENB	Function	Note
0	Enable	-
1	Disable	Default

OTP_RL_FAIL_ENB: OTP reload fail flag output to FAIL_DET pin.

OTP_RL_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

SLV_GAM_DET_ENB: Slave VGM fail flag output to FAIL_DET pin.

SLV_GAM_ENB	Function	Note
0	Enable	-
1	Disable	Default

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R05h

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	05h	1/0	OVP_VCC_ENB	OVP_VSP_ENB	OVP_VSN_ENB	OVP_VGH_ENB	OVP_VGL_ENB	OVP_VCOM_ENB	LVD_VGH_ENB	LVD_VCOM_ENB
			0	0	0	0	0	0	0	0

OVP_VCC_ENB: VCC detect and output to FAIL_DET pin.

OVP_VCC_ENB	Function	Note
0	Enable	Default
1	Disable	-

OVP_VSP_ENB: VSP detect and output to FAIL_DET pin.

OVP_VSP_ENB	Function	Note
0	Enable	Default
1	Disable	-

OVP_VSN_ENB: VSN detect and output to FAIL_DET pin.

OVP_VSN_ENB	Function	Note
0	Enable	Default
1	Disable	-

OVP_VGH_ENB: VGH detect and output to FAIL_DET pin.

OVP_VGH_ENB	Function	Note
0	Enable	Default
1	Disable	-

OVP_VGL_ENB: VGL detect and output to FAIL_DET pin.

OVP_VGL_ENB	Function	Note
0	Enable	Default
1	Disable	-

OVP_VCOM_ENB: VCOM detect and output to FAIL_DET pin.

OVP_VCOM_ENB	Function	Note
0	Enable	Default
1	Disable	-

LVD_VGH_ENB: Low VGH detect and output to FAIL_DET pin.

LVD_VGH_ENB	Function	Note
0	Enable	Default
1	Disable	-

LVD_VCOM_ENB: Low VCOM detect and output to FAIL_DET pin.

LVD_VCOM_ENB	Function	Note
0	Enable	Default
1	Disable	-

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R06h

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	06h	1/0	OVP_VGMPL_ENB	OVP_VGMNL_ENB	OVP_VDDD_ENB	OVP_VCL_ENB	LVD_VGMPH_ENB	LVD_VGMNH_ENB	LVD_VSDPN_ENB	LVD_VCL_ENB
			0	0	0	0	0	0	0	0

OVP_VGMPL_ENB: VGMPL detect and output to FAIL_DET pin.

OVP_VGMPL_ENB	Function	Note
0	Enable	Default
1	Disable	-

OVP_VGMNL_ENB: VGMNL detect and output to FAIL_DET pin.

OVP_VGMNL_ENB	Function	Note
0	Enable	Default
1	Disable	-

OVP_VDDD_ENB: VDDD detect and output to FAIL_DET pin.

OVP_VDDD_ENB	Function	Note
0	Enable	Default
1	Disable	-

OVP_VCL_ENB: VCL detect and output to FAIL_DET pin.

OVP_VCL_ENB	Function	Note
0	Enable	Default
1	Disable	-

LVD_VGMPH_ENB: Low VGMPH detect and output to FAIL_DET pin.

LVD_VGMPH_ENB	Function	Note
0	Enable	Default
1	Disable	-

LVD_VGMNH_ENB: Low VGMNH detect and output to FAIL_DET pin.

LVD_VGMNH_ENB	Function	Note
0	Enable	Default
1	Disable	-

LVD_VSDPN_ENB: Low VSDP/VSDN detect and output to FAIL_DET pin.

LVD_VSDPN_ENB	Function	Note
0	Enable	Default
1	Disable	-

LVD_VCL_ENB: Low VCL detect and output to FAIL_DET pin.

LVD_VCL_ENB	Function	Note
0	Enable	Default
1	Disable	-

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R07h

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	07h	1/0	-	-	-	-	PFM_NG_ACT	OTP_TRIM_FAIL_ACT	EEPROM_OTP_FAIL_ACT	GATE_SD_FAIL_ACT
			-	-	-	-	1	0	0	0

PFM_NG_ACT: PFM NG failed action.

PFM_NG_ACT	Function	Note
0	Black pattern	-
1	Abnormal off	Default

OTP_TRIM_FAIL_ACT: OTP trimmig failed action.

OTP_TRIM_FAIL_ACT	Function	Note
0	Keep normal	Default
1	Black pattern	-

EEPROM_OTP_FAIL_ACT: EEPROM/OTP load failed action.

EEPROM_OTP_FAIL_ACT	Function	Note
0	Keep normal	Default
1	Black pattern	-

GATE_SD_FAIL_ACT: Gate/SD failed action.

GATE_SD_FAIL_ACT	Function	Note
0	Keep normal	Default
1	Black pattern	-

R08h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	08h	1/0	CRC_FAIL_ACT[1:0]		GAS_VGL_FAIL_ACT[1:0]		GAS_PFM_FAIL_ACT[1:0]		GAS_VCC_FAIL_ACT[1:0]	
			0	0	0	0	1	0	1	0

CRC_FAIL_ACT[1:0]: CRC failed action.

CRC_FAIL_ACT[1:0]		Function	Note
0	0	Keep normal	Default
0	1	Black pattern	-
1	0	Abnormal off	-
1	1	Keep normal	-

GAS_VGL_FAIL_ACT[1:0]: GAS VGL failed action.

GAS_VGL_FAIL_ACT[1:0]		Function	Note
0	0	Keep normal	Default
0	1	Black pattern	-
1	0	Abnormal off	-
1	1	Keep normal	-

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GAS_PFM_FAIL_ACT[1:0]: GAS PFM failed action.

GAS_PFM_FAIL_ACT[1:0]		Function	Note
0	0	Keep normal	-
0	1	Black pattern	-
1	0	Abnormal off	Default
1	1	Keep normal	-

GAS_VCC_FAIL_ACT[1:0]: GAS VCC failed action.

GAS_VCC_FAIL_ACT[1:0]		Function	Note
0	0	Keep normal	-
0	1	Black pattern	-
1	0	Abnormal off	Default
1	1	Keep normal	-

R09h

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	09h	1/0	-	-	-	VGMA_PWR_NG_ACT	VCOM_NG_ACT	OVP_PWR_ACT	LVD_PWR_ACT	LVD_VCL_ACT
			-	-	-	0	0	0	0	0

VGMA_PWR_NG_ACT: LVD_VGMPH/ LVD_VGMNH/ OVP_VGMPL/ OVP_VGMNL failed action.

VGMA_PWR_NG_ACT	Function	Note
0	Keep normal	Default
1	Black pattern	-

VCOM_NG_ACT: LVD_VCOM/ OVP_VCOM failed action.

VCOM_NG_ACT	Function	Note
0	Keep normal	Default
1	Black pattern	-

OVP_PWR_ACT: OVP_VCC/ OVP_VDDD/ OVP_VSP/ OVP_VSN/ OVP_VGH/ OVP_VGL/ OVP_VCL failed action.

OVP_PWR_ACT	Function	Note
0	Keep normal	Default
1	Black pattern	-

LVD_PWR_ACT: LVD_VGH/ LVD_VSDPN failed action.

LVD_PWR_ACT	Function	Note
0	Keep normal	Default
1	Black pattern	-

LVD_VCL_ACT: LVD_VCL failed action.

LVD_VCL_ACT	Function	Note
0	Keep normal	Default
1	Black pattern	-

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R0Bh

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	0Bh	1/0	PFM_DET_EN	PFM_DET_OTP	PFM_REDET_OPT	DPFM_OSC_SEL	-	-	-	-
			1	1	0	1	-	-	-	-

PFM_DET_EN: PFM_NG detect circuit enable **(SID[1:0]=LL)**

PFM_DET_EN	Function	Note
0	Enable	Default
1	Disable	-

PFM_DET_OPT: PFM fail-detect time selection. PFM abnormal boost state over the N frame, then PFM_NG trigger and DRVP/DRVN stop.

PFM_DET_OPT	Function	Note
0	60ms	Default
1	30ms	-

PFM_REDET_OPT: PFM re-detect time after PFM_NG

PFM_REDET_OPT	Function	Note
0	381ms	Default
1	762ms	-

DPFM_OSC_SEL: PFM clock frequency selection.

DPFM_OSC_SEL	Function	Note
0	5MHz	Default
1	10MHz	-

R0Ch

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	0Ch	1/0	CROSS_TALK_GRAY	FLICK_GRAY	GIP_MX_TABLE_SEL[1:0]		-	GAS_OTP_SELB	RESET_SLP_OPT	ZZS_FORCE_POL_ENB
			0	0	0	0	-	0	0	0

CROSS_TALK_GRAY: Gray level selection of cross talk pattern in BIST mode.

CROSS_TALK_GRAY	Function	Note
0	L186	Default
1	L128	-

FLICK_TALK_GRAY: Gray level selection of flick pattern in BIST mode.

FLICK _TALK_GRAY	Function	Note
0	L186	Default
1	L128	-

GIP_MX_TABLE_SEL[1:0]: GIP MUX setting table selection.

GIP_MX_TABLE_SEL[1:0]		Function	Note
0	0	GIP use Table1 **(Page16h, Page17h)**	Default
0	1	GIP use Table2 **(Page18h, Page19h)**	-
1	0	GIP use Table1 when TB=H or GIP use Table2 when TB=L	-
1	1	Reserved	-

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GAS_OTP_SELB: Exit gas need do otp /eeprom reload.

GAS_OTP_SELB	Function	Note
0	Exit gas don't otp /eeprom reload	Default
1	Exit gas need do otp /eeprom reload	-

RESET_SLP_OPT: Sleep or GAS mode option for RESETB_SLP function.

RESET_SLP_OPT	Function	Note
0	Enter Sleep mode at RESETB_SLP falling edge.	Default
1	Enter GAS mode at RESETB_SLP falling edge.	-

ZZS_FORCE_POL_ENB: Zigzag panel inversion selection.

ZZS_FORCE_POL_ENB	Function	Note
0	Zigzag panel force column inversion	Default
1	Zigzag panel by register INV[1:0] select POL inversion type	-

R0Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	0Dh	1/0	ENDRVN[1:0]		ENDRVP[1:0]		-	-	-	-
			1	1	1	1	-	-	-	-

ENDRVN[1:0]: Negative polarity driving ability control.

ENDRVN[1:0]		Function	Note
0	0	100%	-
0	1	130%	-
1	0	170%	Default
1	1	200%	-

ENDRVP[1:0]: Positive polarity driving ability control.

ENDRVP[1:0]		Function	Note
0	0	100%	-
0	1	130%	-
1	0	170%	Default
1	1	200%	-

R0Eh ~ R0Fh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	0Eh	1/0	PON_FAIL_EN[7:0]							
			1	1	1	1	1	1	1	1
	0Fh		-	-	-	-	-	-	PON_FAIL_EN[9:8]	
			-	-	-	-	-	-	1	1

PON_FAIL_EN[9:0]: Power on self-test enable **(1: enable)**.

PON_ FAIL _EN[9:0]										Function	Note
-	-	-	-	-	-	-	-	-	1	LVDS fail	Default=1
-	-	-	-	-	-	-	-	1	-	GAS	Default=1
-	-	-	-	-	-	-	1	-	-	SOURCE fail	Default=1
-	-	-	-	-	-	1	-	-	-	Gate fail	Default=1
-	-	-	-	-	1	-	-	-	-	No-video fail	Default=1
-	-	-	-	1	-	-	-	-	-	EEPROM fail	Default=1
-	-	-	1	-	-	-	-	-	-	OTP reload fail	Default=1
-	-	1	-	-	-	-	-	-	-	PFM NG fail	Default=1
-	1	-	-	-	-	-	-	-	-	CRC check fail **(CRC1 or CRC2 or CRC 3 or CRC4 check fail)**	Default=1
1	-	-	-	-	-	-	-	-	-	OVP check fail **(over voltage detect)**	Default=1

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R10h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	10h	1/0	TP_DLY[7:0]							
			0	1	0	0	0	0	0	0

TP_DLY: TP_SYNC rising edge offset setting when TP_SYNC_SEL[2:0] = 3'b110.
Range = (1~255) * 4T.

TP_DLY[7:0]								Function	Note
0	0	0	0	0	0	0	0	4T(1)	-
0	0	0	0	0	0	0	1	4T(1)	-
0	0	0	0	0	0	1	0	8T(1)	-
:	:	:	:	:	:	:	:	:	-
0	1	0	0	0	0	0	0	256T(1)	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	1020T(1)	-

Note: (1) The unit of T is decided by register SD_CLK_SEL.

R11h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	11h	1/0	TP_WIDTH[7:0]							
			0	1	0	0	0	0	0	0

TP_WIDTH[7:0]: TP_SYNC width setting when TP_SYNC_SEL[2:0] = 3'b110.
Range = (1~255) * 4T.

TP_WIDTH[7:0]								Function	Note
0	0	0	0	0	0	0	0	4T(1)	-
0	0	0	0	0	0	0	1	4T(1)	-
0	0	0	0	0	0	1	0	8T(1)	-
:	:	:	:	:	:	:	:	:	-
0	1	0	0	0	0	0	0	256T(1)	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	1020T(1)	-

Note: (1) The unit of T is decided by register SD_CLK_SEL.

R12h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
4	12h	1/0	TP_SYNC_INV	TP_SYNC1_SEL[2:0]			TP_WIDTH_ENB	TP_SYNC2_SEL[2:0]		
			0	1	1	0	1	1	1	0

TP_SYNC_INV: TP_SYNC output inverse function.

TP_SYNC_INV	Function	Note
0	Disable	Default
1	Enable	-

TP_WIDTH_ENB: TP_SYNC width selection when TP_SYNC_SEL[2:0] = 3'b110.

TP_WIDTH_ENB	Function	Note
0	TP_SYNC width by TP_WIDTH **(Page04h R11h)**	-
1	TP_SYNC falling follow Source_SW rising edge.	Default

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TP_SYNC1_SEL[2:0]/TP_SYNC2_SEL[2:0]: TP_SYNC1/2 output signal selection.

TP_SYNC1_SEL[2:0] TP_SYNC2_SEL[2:0]			Function	Note
0	0	0	Output HS signal.	-
0	0	1	Output Source output period by frame. **(Internal VDEN)**	-
0	1	0	Output VS signal.	-
0	1	1	Reserved.	-
1	0	0	Reserved.	-
1	0	1	Output XAO signal.	-
1	1	0	TP_SYNC register setting. **(TP_SYNC trigger by TP_DLY and TP_WIDTH_ENB setting)**	-
1	1	1	Output GND.	Default

R13h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	13h	1/0	GIP_RL_EN_S3 [1:0]		GIP_RL_EN_S2 [1:0]		GIP_RL_EN_S1 [1:0]		GIP_RL_EN_M [1:0]	
			0	1	0	1	0	1	1	1

GIP_RL_EN_M[1:0]: RL side LTPS MUX enable for master chip.
GIP_RL_EN_S1[1:0]: RL side LTPS MUX enable for Slave1 chip.
GIP_RL_EN_S2[1:0]: RL side LTPS MUX enable for Slave2 chip.
GIP_RL_EN_S3[1:0]: RL side LTPS MUX enable for Slave3 chip.

GIP_RL_EN_M[1:0] GIP_RL_EN_S1[1:0] GIP_RL_EN_S2[1:0] GIP_RL_EN_S3[1:0]		Function	Note
0	0	GIP R/L side output both disable	-
0	1	GIP R side output enable	Default
1	0	GIP L side enable	-
1	1	GIP R/L side output both enable	-

R14h ~ R18h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
04h	14h	1/0	L_GIP_VGH_SEL[19:16]				R_GIP_VGH_SEL[19:16]			
			0	0	0	0	0	0	0	0
	15h	1/0	L_GIP_VGH_SEL[15:8]							
			0	0	0	0	0	0	0	0
	16h	1/0	L_GIP_VGH_SEL[7:0]							
			0	0	0	0	0	0	0	0
	17h	1/0	R_GIP_VGH_SEL[15:8]							
			0	0	0	0	0	0	0	0
	18h	1/0	R_GIP_VGH_SEL[7:0]							
			0	0	0	0	0	0	0	0

L_GIP_VGH_SEL[19:0]: Left side GIP PIN VGH power select for GAS state.
R_GIP_VGH_SEL[19:0]: Right side GIP PIN VGH power select for GAS state.

Bit	Function	Note
0	VGH1	Default
1	VGH2	-

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8.2.7. Page05h for GIP function

Please refer to application note for GIP function.
(OTP group 12, and can be programmed 2 times.)

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8.2.8. Page06h for Digital gamma correction for Red color

R01h ~ R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
06h	01h	1/0	GMA1R[7:0]							
			0	0	0	0	0	0	0	0
	02h		GMA2R[7:0]							
			0	0	0	0	0	1	0	0
	03h		GMA3R[7:0]							
			0	0	0	0	1	1	0	0
	04h		GMA4R[7:0]							
			0	0	0	1	1	1	0	0
	05h		GMA5R[7:0]							
			0	0	1	0	1	1	0	0
	06h		GMA6R[7:0]							
			0	0	1	1	1	1	0	0
	07h		GMA7R[7:0]							
			0	1	0	1	1	1	0	0
	08h		GMA8R[7:0]							
			0	1	1	1	1	1	0	0
	09h		GMA9R[7:0]							
			1	0	1	1	1	1	0	0
	0Ah		GMA10R[7:0]							
			1	1	1	1	1	1	0	0
	0Bh		GMA11R[7:0]							
			0	1	1	1	1	1	0	0
	0Ch		GMA12R[7:0]							
			1	1	1	1	1	1	0	0
	0Dh		GMA13R[7:0]							
			0	0	0	0	0	0	0	0
	0Eh		GMA14R[7:0]							
			1	0	0	0	0	0	0	0
	0Fh		GMA15R[7:0]							
			0	0	0	0	0	0	0	0

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Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
06h	10h	1/0	GMA16R[7:0]							
			0	1	0	0	0	0	0	0
	11h		GMA17R[7:0]							
			1	0	0	0	0	0	0	0
	12h		GMA18R[7:0]							
			1	0	1	0	0	0	0	0
	13h		GMA19R[7:0]							
			1	1	0	0	0	0	0	0
	14h		GMA20R[7:0]							
			1	1	0	1	0	0	0	0
	15h		GMA21R[7:0]							
			1	1	1	0	0	0	0	0
	16h		GMA22R[7:0]							
			1	1	1	1	0	0	0	0
	17h		GMA23R[7:0]							
			1	1	1	1	1	0	0	0
	18h		GMA24R[7:0]							
			1	1	1	1	1	1	0	0
	19h		GMA1R[9:8]		GMA2R[9:8]		GMA3R[9:8]		GMA4R[9:8]	
			0	0	0	0	0	0	0	0
	1Ah		GMA5R[9:8]		GMA6R[9:8]		GMA7R[9:8]		GMA8R[9:8]	
			0	0	0	0	0	0	0	0
	1Bh		GMA9R[9:8]		GMA10R[9:8]		GMA11R[9:8]		GMA12R[9:8]	
			0	0	0	0	0	1	0	1
	1Ch		GMA13R[9:8]		GMA14R[9:8]		GMA15R[9:8]		GMA16R[9:8]	
			1	0	1	0	1	1	1	1
	1Dh		GMA17R[9:8]		GMA18R[9:8]		GMA19R[9:8]		GMA20R[9:8]	
			1	1	1	1	1	1	1	1
	1Eh		GMA21R[9:8]		GMA22R[9:8]		GMA23R[9:8]		GMA24R[9:8]	
			1	1	1	1	1	1	1	1

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Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
GMA1R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference ”Y1[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA2R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y2[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA3R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y3[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA4R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y4[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA5R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y5[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA6R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y6[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA7R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y7[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA8R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y8[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA9R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y9[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA10R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y10[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA11R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y11[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA12R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y12[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA13R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y13[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA14R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y14[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA15R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y15[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA16R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y16[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA17R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y17[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA18R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y18[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

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Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
GMA19R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y19[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA20R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y20[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA21R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y21[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA22R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y22[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA23R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y23[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA24R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y24[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

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8.2.9. Page07h for Digital gamma correction for Green color

R01h ~ R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
07h	01h	1/0	GMA1G[7:0]							
			0	0	0	0	0	0	0	0
	02h		GMA2G[7:0]							
			0	0	0	0	0	1	0	0
	03h		GMA3G[7:0]							
			0	0	0	0	1	1	0	0
	04h		GMA4G[7:0]							
			0	0	0	1	1	1	0	0
	05h		GMA5G[7:0]							
			0	0	1	0	1	1	0	0
	06h		GMA6G[7:0]							
			0	0	1	1	1	1	0	0
	07h		GMA7G[7:0]							
			0	1	0	1	1	1	0	0
	08h		GMA8G[7:0]							
			0	1	1	1	1	1	0	0
	09h		GMA9G[7:0]							
			1	0	1	1	1	1	0	0
	0Ah		GMA10G[7:0]							
			1	1	1	1	1	1	0	0
	0Bh		GMA11G[7:0]							
			0	1	1	1	1	1	0	0
	0Ch		GMA12G[7:0]							
			1	1	1	1	1	1	0	0
	0Dh		GMA13G[7:0]							
			0	0	0	0	0	0	0	0
	0Eh		GMA14G[7:0]							
			1	0	0	0	0	0	0	0
	0Fh		GMA15G[7:0]							
			0	0	0	0	0	0	0	0

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Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
07h	10h	1/0	GMA16G[7:0]							
			0	1	0	0	0	0	0	0
	11h		GMA17G[7:0]							
			1	0	0	0	0	0	0	0
	12h		GMA18G[7:0]							
			1	0	1	0	0	0	0	0
	13h		GMA19G[7:0]							
			1	1	0	0	0	0	0	0
	14h		GMA20G[7:0]							
			1	1	0	1	0	0	0	0
	15h		GMA21G[7:0]							
			1	1	1	0	0	0	0	0
	16h		GMA22G[7:0]							
			1	1	1	1	0	0	0	0
	17h		GMA23G[7:0]							
			1	1	1	1	1	0	0	0
	18h		GMA24G[7:0]							
			1	1	1	1	1	1	0	0
	19h		GMA1G[9:8]		GMA2G[9:8]		GMA3G[9:8]		GMA4G[9:8]	
			0	0	0	0	0	0	0	0
	1Ah		GMA5G[9:8]		GMA6G[9:8]		GMA7G[9:8]		GMA8G[9:8]	
			0	0	0	0	0	0	0	0
	1Bh		GMA9G[9:8]		GMA10G[9:8]		GMA11G[9:8]		GMA12G[9:8]	
			0	0	0	0	0	1	0	1
	1Ch		GMA13G[9:8]		GMA14G[9:8]		GMA15G[9:8]		GMA16G[9:8]	
			1	0	1	0	1	1	1	1
	1Dh		GMA17G[9:8]		GMA18G[9:8]		GMA19G[9:8]		GMA20G[9:8]	
			1	1	1	1	1	1	1	1
	1Eh		GMA21G[9:8]		GMA22G[9:8]		GMA23G[9:8]		GMA24G[9:8]	
			1	1	1	1	1	1	1	1

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Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
GMA1G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference ”Y1[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA2G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y2[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA3G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y3[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA4G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y4[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA5G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y5[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA6G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y6[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA7G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y7[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA8G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y8[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA9G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y9[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA10G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y10[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA11G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y11[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA12G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y12[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA13G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y13[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA14G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y14[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA15G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y15[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA16G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y16[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA17G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y17[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA18G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y18[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

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Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
GMA19G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y19[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA20G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y20[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA21G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y21[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA22G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y22[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA23G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y23[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA24G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y24[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

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8.2.10. Page08h for Digital gamma correction for Blue color

R01h ~ R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
08h	01h	1/0	GMA1B[7:0]							
			0	0	0	0	0	0	0	0
	02h		GMA2B[7:0]							
			0	0	0	0	0	1	0	0
	03h		GMA3B[7:0]							
			0	0	0	0	1	1	0	0
	04h		GMA4B[7:0]							
			0	0	0	1	1	1	0	0
	05h		GMA5B[7:0]							
			0	0	1	0	1	1	0	0
	06h		GMA6B[7:0]							
			0	0	1	1	1	1	0	0
	07h		GMA7B[7:0]							
			0	1	0	1	1	1	0	0
	08h		GMA8B[7:0]							
			0	1	1	1	1	1	0	0
	09h		GMA9B[7:0]							
			1	0	1	1	1	1	0	0
	0Ah		GMA10B[7:0]							
			1	1	1	1	1	1	0	0
	0Bh		GMA11B[7:0]							
			0	1	1	1	1	1	0	0
	0Ch		GMA12B[7:0]							
			1	1	1	1	1	1	0	0
	0Dh		GMA13B[7:0]							
			0	0	0	0	0	0	0	0
	0Eh		GMA14B[7:0]							
			1	0	0	0	0	0	0	0
	0Fh		GMA15B[7:0]							
			0	0	0	0	0	0	0	0

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Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
08h	10h	1/0	GMA16B[7:0]							
			0	1	0	0	0	0	0	0
	11h		GMA17B[7:0]							
			1	0	0	0	0	0	0	0
	12h		GMA18B[7:0]							
			1	0	1	0	0	0	0	0
	13h		GMA19B[7:0]							
			1	1	0	0	0	0	0	0
	14h		GMA20B[7:0]							
			1	1	0	1	0	0	0	0
	15h		GMA21B[7:0]							
			1	1	1	0	0	0	0	0
	16h		GMA22B[7:0]							
			1	1	1	1	0	0	0	0
	17h		GMA23B[7:0]							
			1	1	1	1	1	0	0	0
	18h		GMA24B[7:0]							
			1	1	1	1	1	1	0	0
	19h		GMA1B[9:8]		GMA2B[9:8]		GMA3B[9:8]		GMA4B[9:8]	
			0	0	0	0	0	0	0	0
	1Ah		GMA5B[9:8]		GMA6B[9:8]		GMA7B[9:8]		GMA8B[9:8]	
			0	0	0	0	0	0	0	0
	1Bh		GMA9B[9:8]		GMA10B[9:8]		GMA11B[9:8]		GMA12B[9:8]	
			0	0	0	0	0	1	0	1
	1Ch		GMA13B[9:8]		GMA14B[9:8]		GMA15B[9:8]		GMA16B[9:8]	
			1	0	1	0	1	1	1	1
	1Dh		GMA17B[9:8]		GMA18B[9:8]		GMA19B[9:8]		GMA20B[9:8]	
			1	1	1	1	1	1	1	1
	1Eh		GMA21B[9:8]		GMA22B[9:8]		GMA23B[9:8]		GMA24B[9:8]	
			1	1	1	1	1	1	1	1

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Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
GMA1B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference ”Y1[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA2B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y2[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA3B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y3[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA4B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y4[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA5B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y5[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA6B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y6[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA7B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y7[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA8B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y8[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA9B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y9[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA10B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y10[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA11B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y11[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA12B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y12[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA13B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y13[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA14B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y14[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA15B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y15[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA16B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y16[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA17B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y17[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA18B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y18[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

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Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
GMA19B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y19[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA20B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y20[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA21B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y21[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA22B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y22[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA23B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y23[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
GMA24B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y24[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

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8.2.11. Page09h for LVDS function setting

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
09h	01h	1/0	-	DLL_BANK	LVDS_AGING	LVDS_FMT	LANE_SW	LANE_PN	LVDS_PULL[1:0]	
			-	0	0	0	0	0	0	0

DLL_BANK: LVDS input frequency range selection.

DLL_BANK	Function	Note
0	> 30MHZ	Default
1	< 30MHZ	-

LVDS_AGING: LVDS power saving enable.
When enabled, data lanes are turned off in BIST and self protection mode.

LVDS_AGING	Function	Note
0	Disabled	Default
1	Enabled	-

LVDS_FMT: LVDS and TTL input data format selection.

LVDS_FMT	Function	Note
0	NS **(JEIDA)** format	Default
1	Thine **(VESA)** format	-

LANE_SW: LVDS Lane swap selection, effective when FCS=0.

LVDS_SW	Function	Note
0	Not swap	Default
1	Swap	-

LVDS_PN: LVDS lane PN polarity swapping selection, effective when FCS=0.

LVDS_PN	Function	Note
0	Not swap	Default
1	Swap	-

LVDS_PULL[1:0] : LVDS pull up control.

LVDS_PULL[1:0]		Function	Note
0	0	LVDS pull up/down enable when lock is low	-
0	1		Default
1	0	Always disable LVDS pull up/down	-
1	1	Always enable LVDS pull up/down	-

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R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
09h	02h	1/0	-	-	LVDS_BW[1:0]		LVDS_CPB[3:0]			
			-	-	0	1	0	0	1	1

LVDS_BW[1:0]: LVDS DLL bandwidth selection.

LVDS_BW[1:0]		Function	Note
0	0	Low	-
0	1	Medium	Default
1	0	High	-
1	1	Maximum	-

LVDS_CPB[3:0]: LVDS charge pump current selection.

LVDS_CPB[3:0]				Function	Note
0	0	0	0	0%	-
0	0	0	1	25%	-
0	0	1	0	50%	-
0	0	1	1	75%	Default
:	:	:	:	:	-
1	0	0	0	200%	-
:	:	:	:	:	-
:	:	:	:	:	-
1	1	1	0	350%	-
1	1	1	1	375%	-

R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
09h	03h	1/0	RX_VB[1:0]		LVDS_VBDLL[1:0]		S3_EQ_OPT	S2_EQ_OPT	S1_EQ_OPT	M_EQ_OPT
			1	0	0	1	0	1	1	1

RX_VB[1:0]: LVDS receiver bias current adjustment.

RX_VB[1:0]		Function	Note
0	0	75%	-
0	1	100%	Default
1	0	125%	-
1	1	150%	-

LVDS_VBDLL[1:0]: LVDS DLL bias current adjustment.

LVDS_VBDLL[1:0]		Function	Note
0	0	82%	-
0	1	100%	Default
1	0	137%	-
1	1	160%	-

M_EQ_OPT/S1_EQ_OPT/S2_EQ_OPT/S3_EQ_OPT:
LVDS receiver equalization DC DB function enable of each chip.

M_EQ_OPT S1_EQ_OPT S2_EQ_OPT S3_EQ_OPT	Function	Note
0	Disabled	-
1	Enabled	Default

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R04h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
09h	04h	1/0	S3_EQ_SW[1:0]		S2_EQ_SW[1:0]		S1_EQ_SW[1:0]		M_EQ_SW[1:0]	
			1	0	1	0	1	0	1	0

M_EQ_SW[1:0]/S1_EQ_SW[1:0]/S2_EQ_SW[1:0] /S3_EQ_SW[1:0]:

LVDS clock lane equalization peak function selection of each chip.

M_EQ_SW[1:0] S1_EQ_SW[1:0] S2_EQ_SW[1:0] S3_EQ_SW[1:0]		Function	Note
0	0	0dB	-
0	1	1dB	-
1	0	2dB	Default
1	1	3dB	-

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8.2.12. Page0Ah for Temperature sensor function setting

R01h ~ R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	01h	1/0	-	-	-	-	-	-	VCOMS_HT[8]	VCOMS_LT[8]
			-	-	-	-	-	-	1	1
0Ah	02h	1/0	VCOMS_HT[7:0]							
			0	1	0	1	1	1	0	0
0Ah	03h	1/0	VCOMS_LT[7:0]							
			0	1	0	1	1	1	0	0

VCOMS_HT[8:0]: VCOM voltage adjustment at high temperature mode.
VCOM= 2 + VCOMS_HT[8:0] x (-0.01)V

VCOMS_HT[8:0]									Function	Note
0	0	0	0	0	0	0	0	0	2.00V	-
0	0	0	0	0	0	0	0	1	1.99V	-
:	:	:	:	:	:	:	:	:	:	-
1	0	1	0	1	1	1	0	0	-1.48V	Default
:	:	:	:	:	:	:	:	:	:	-
1	1	1	0	0	0	0	1	0	-2.50V	-
1	1	1	0	0	0	0	1	1	Reserved	-
:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	1	Reserved	-

VCOMS_LT[8:0]: VCOM voltage adjustment at low temperature mode.
VCOM= 2 + VCOMS_LT[8:0] x (-0.01)V

VCOMS_LT[8:0]									Function	Note
0	0	0	0	0	0	0	0	0	2.00V	-
0	0	0	0	0	0	0	0	1	1.99V	-
:	:	:	:	:	:	:	:	:	:	-
1	0	1	0	1	1	1	0	0	-1.48V	Default
:	:	:	:	:	:	:	:	:	:	-
1	1	1	0	0	0	0	1	0	-2.50V	-
1	1	1	0	0	0	0	1	1	Reserved	-
:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	1	Reserved	-

R04h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	04h	1/0	-	VGHS_HT[6:0]						
			-	0	0	1	1	1	0	0

VGHS_HT[6:0]: VGH voltage adjustment at high temperature mode.
VGH=5.0+VGHS_HT[5:0] x 0.25V

VGHS_HT[6:0](1)							Function	Note
0	0	0	0	0	0	0	5.00V	-
0	0	0	0	0	0	1	5.25V	-
0	0	0	0	0	0	1	5.50V	-
:	:	:	:	:	:	:	:	-
0	0	1	1	1	0	0	12.0V	Default
:	:	:	:	:	:	:	:	-
1	0	0	1	1	0	0	24.0V	-
1	0	0	1	1	1	1	24.0V	-

Note: (1) VGH + |VGL| < 32V.

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R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	05h	1/0	-	-	VGLS_HT[5:0]					
			-	-	0	0	1	1	0	0

VGLS_HT[5:0]: VGL voltage adjustment at high temperature mode.
VGL= -5.0+VGLS_HT[4:0] x (-0.25) V

VGLS_HT[5:0](1)						Function	Note
0	0	0	0	0	0	-5.00V	-
0	0	0	0	0	1	-5.25V	-
:	:	:	:	:	:	:	-
0	0	1	1	0	0	-8.00V	Default
:	:	:	:	:	:	:	-
1	0	1	1	0	0	-16.00V	-
:	:	:	:	:	:	:	-
1	1	1	1	1	1	-16.00V	-

Note: (1) VGH + |VGL| < 32V.

R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	06h	1/0	-	VGHS_LT[6:0]						
			-	0	0	1	1	1	0	0

VGHS_LT[6:0]: VGH voltage adjustment at low temperature mode.
VGH=5.0+VGHS_LT[6:0] x 0.25V

VGHS_LT[6:0](1)							Function	Note
0	0	0	0	0	0	0	5.00V	-
0	0	0	0	0	0	1	5.25V	-
0	0	0	0	0	0	1	5.50V	-
:	:	:	:	:	:	:	:	-
0	0	1	1	1	0	0	12.00V	Default
:	:	:	:	:	:	:	:	-
1	0	0	1	1	0	0	24.00V	-
1	0	0	1	1	1	1	24.00V	-

Note: (1) VGH + |VGL| < 32V.

R07h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	07h	1/0	DIM_ OPT	-	VGLS_LT[5:0]					
			0	-	0	0	1	1	0	0

DIM_OPT: Analog gamma **(AGAM)** voltage dimming option.

DIM_OPT	Function	Note
0	AGAM dimming with VGMPH/PL/NH/NL & VCOM	Default
1	AGAM dimming after VGMPH/PL/NH/NL & VCOM done	-

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VGLS_LT[5:0]: VGL voltage adjustment at low temperature mode.
VGL= -5.0+VGLS_LT[5:0] x (-0.25) V

VGLS_HT[5:0](1)						Function	Note
0	0	0	0	0	0	-5.00V	-
0	0	0	0	0	1	-5.25V	-
:	:	:	:	:	:	:	-
0	0	1	1	0	0	-8.00V	Default
:	:	:	:	:	:	:	-
1	0	1	1	0	0	-16.00V	-
:	:	:	:	:	:	:	-
1	1	1	1	1	1	-16.00V	-

Note: (1) VGH + |VGL| < 32V.

R08h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	08h	1/0	DIM_EN	DIM_FRAME[1:0]		VGMPHS_HT[4:0]				
			0	0	0	1	1	0	1	0

DIM_EN: Voltage dimming enable at temperature mode.

DIM_EN	Function	Note
0	Disable	Default
1	Enable	-

DIM_FRAME[1:0]: Dimming frame period setting.

DIM_EN		Function	Note
0	0	8 frames	Default
0	1	16 frames	-
1	0	32 frames	-
1	1	Reserved	-

VGMPHS_HT[4:0]: VGMPH voltage adjustment at high temperature mode.
VGMPH= 4.0 + VGMPHS_HT[4:0] x 0.1V

VGMPHS_HT[4:0]					Function	Note
0	0	0	0	0	4.0V	Min.
0	0	0	0	1	4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	5.8V	-
:	:	:	:	:	:	-
1	1	0	0	1	6.5V	-
1	1	0	1	0	6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

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R09h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	09h	1/0	TS_GOE_EN	TS_GAMMA_EN	-	VGMNHS_HT[4:0]				
			0	0	-	1	1	0	1	0

TS_GOE_EN: Temperature mode disable and GOE setting by RT register.

TS_GOE_EN	Function	Note
0	GOE timing setting by RT register	Default
1	GOE timing setting selection by[TS_H:TS_L]	-

TS_GAMMA_EN: Temperature sensor enable for VGMPHS, VGMNHS, VGMPLS, VGMNLS voltage setting.

TS_GAMMA_EN	Function	Note
0	By OTP times	Default
1	Enable **(selection by TS)**	-

VGMNHS_HT[4:0]: VGMNH voltage adjustment at high temperature mode.
VGMNH= -4.0 + VGMNHS_HT[4:0] x (-0.1V)

VGMNHS_HT[4:0]					Function	Note
0	0	0	0	0	-4.0V	Min.
0	0	0	0	1	-4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	-5.8V	-
:	:	:	:	:	:	-
1	1	0	0	1	-6.5V	-
1	1	0	1	0	-6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

R0Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	0Ah	1/0	VGMPLS_HT[3:0]				VGMNLS_HT[3:0]			
			0	0	0	1	0	0	0	1

VGMPLS_HT[3:0]: VGMPL voltage adjustment at low temperature mode.
VGMPL=0.2 + VGMPLS_HT[3:0] x 0.1V

VGMPLS_HT[3:0]				Function	Note
0	0	0	0	0.2V	-
0	0	0	1	0.3V	Default
:	:	:	:	:	-
1	1	1	0	1.6V	-
1	1	1	1	1.7V	-

VGMNLS_HT[3:0]: VGMNL voltage adjustment at low temperature mode.
VGMNL= -0.2 - VGMNLS_HT[3:0] x 0.1V

VGMNLS_HT[3:0]				Function	Note
0	0	0	0	-0.2V	-
0	0	0	1	-0.3V	Default
:	:	:	:	:	-
1	1	1	0	-1.6V	-
1	1	1	1	-1.7V	-

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R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	0Bh	1/0	-	TS_VCOM_EN	TS_VGHL_EN	VGMPHS_LT[4:0]				
			-	0	-	1	1	0	1	0

TS_VCOM_EN: VCOM voltage setting for temperature.

TS_VCOM_EN	Function	Note
0	Disable	Default
1	Enable	-

TS_VGHL_EN: VGH and VGL voltage setting for temperature.

TS_VGHL_EN	Function	Note
0	Disable	Default
1	Enable	-

VGMPHS_LT[4:0]: VGMPH voltage adjustment at low temperature mode.
VGMPH= 4.0 + VGMPHS_LT[4:0] x 0.1V

VGMPHS_LT[4:0]					Function	Note
0	0	0	0	0	4.0V	Min.
0	0	0	0	1	4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	5.8V	-
:	:	:	:	:	:	-
1	1	0	0	0	6.4V	-
1	1	0	0	1	6.5V	-
1	1	0	1	0	6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

R0Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	0Ch	1/0	-	-	-	VGMNHS_LT[4:0]				
			-	-	-	1	1	0	1	0

VGMNHS_LT[4:0]: VGMNH voltage adjustment at low temperature mode.
VGMNH= -4.0 + VGMNHS_LT[4:0] x (-0.1V)

VGMNHS_LT[4:0]					Function	Note
0	0	0	0	0	-4.0V	Min.
0	0	0	0	1	-4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	-5.8V	-
:	:	:	:	:	:	-
1	1	0	0	1	-6.5V	-
1	1	0	1	0	-6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

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R0Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	0Dh	1/0	VGMPLS_LT[3:0]				VGMNLS_LT[3:0]			
			0	0	0	1	0	0	0	1

VGMPLS_LT[3:0]: VGMPL voltage adjustment at low temperature mode.
VGMPL=0.2 + VGMPLS_LT[3:0] x 0.1V

VGMPLS_LT[3:0]				Function	Note
0	0	0	0	0.2V	-
0	0	0	1	0.3V	Default
:	:	:	:	:	-
1	1	1	0	1.6V	-
1	1	1	1	1.7V	-

VGMNLS_LT[3:0]: VGMNL voltage adjustment at low temperature mode.
VGMNL= -0.2 - VGMNLS_LT[3:0] x 0.1V

VGMNLS_LT[3:0]				Function	Note
0	0	0	0	-0.2V	-
0	0	0	1	-0.3V	Default
:	:	:	:	:	-
1	1	1	0	-1.6V	-
1	1	1	1	-1.7V	-

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8.2.13. Page0Bh for OTP function setting

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	01h	1/0	-	-	OTP_GROUP[5:0]					
			-	-	0	0	0	0	0	0

OTP_GROUP[5:0]: OTP group select.

OTP_GROUP[5:0]						Reg. mapping	OTP times	Note
0	0	0	0	0	1	Page00h, 01h~05h	2	Operation setting
0	0	0	0	1	0	Page00h, 06h~0Dh	2	TCON setting
0	0	0	0	1	1	Page00h, 0Eh~13h	2	TCON setting
0	0	0	1	0	0	Page00h, 14h~19h	2	TCON setting
0	0	0	1	0	1	Page00h, 1Ah~1Eh	2	TCON setting
0	0	0	1	1	0	Page01h, 01h~19h	2	Power setting
0	0	0	1	1	1	Page01h, 1Ah~1Ch	3	VCOM offset setting
0	0	1	0	0	0	Page01h, 1Dh~1Eh	10	VCOM setting
0	0	1	0	0	1	Page02h, 01h~15h	3	Positive analog gamma
0	0	1	0	1	0	Page03h, 01h~15h	3	Negative analog gamma
0	0	1	0	1	1	Page04h, 01h~18h	2	TCON setting
0	0	1	1	0	0	Page05h, 01h~11h	2	GIP function setting
0	0	1	1	0	1	Page06h, 01h~1Eh	1	Digital gamma R
0	0	1	1	1	0	Page07h, 01h~1Eh	1	Digital gamma G
0	0	1	1	1	1	Page08h, 01h~1Eh	1	Digital gamma B
0	1	0	0	0	0	Page09h, 01h~04h	2	LVDS setting
0	1	0	0	0	1	Page10h, 01h~03h	5	VCOM HT/LT voltage setting
0	1	0	0	1	0	Page10h, 04h~0Dh	2	TS setting
0	1	0	0	1	1	Page12h, 01h~1Eh	2	LTPS function setting
0	1	0	1	0	0	Page13h, 01h~1Ch	2	GIP function setting
0	1	0	1	0	1	Page14h, 01h~1Eh	2	GIP function setting
0	1	0	1	1	0	Page15h, 01h~1Eh	2	GIP function setting
0	1	0	1	1	1	Page16h, 01h~17h	2	GIP function setting
0	1	1	0	0	0	Page17h, 01h~17h	2	GIP output setting
0	1	1	0	0	1	Page18h, 01h~14h	2	GIP output setting
0	1	1	0	1	0	Page19h, 01h~14h	2	GIP output setting
0	1	1	0	1	1	Page20h, 01h~06h	1	ESD function setting
0	1	1	1	0	0	Page20h, 07h~0Ch	1	ESD function setting
0	1	1	1	0	1	Page21h, 01h~1Eh	1	VENDOR_ID
0	1	1	1	1	0	Page27h, 01h	3	OTP checksum

R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	02h	1/0	WOTP[7:0]							
			1	0	0	1	1	0	0	1

WOTP[7:0]: OTP program command enable.

WOTP[7:0]								Function	Note
0	0	0	0	0	0	0	0	Disable	-
:	:	:	:	:	:	:	:	Disable	-
0	1	1	0	0	1	0	1	Disable	-
0	1	1	0	0	1	1	0	Enable	-
0	1	1	0	0	1	1	1	Disable	-
:	:	:	:	:	:	:	:	Disable	-
1	0	0	1	1	0	0	1	Disable	Default
:	:	:	:	:	:	:	:	Disable	-
1	1	1	1	1	1	1	1	Disable	-

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R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	03h	1/0	OTP_WR4	OTP_WR3	OTP_WR2	OTP_WR1	OTP_WR_ALL_GROUP	OTP_RELOAD	OTP_RD	-
			0	0	0	0	0	0	0	-

OTP_WR1: OTP write function selection for SID[1:0]=LL. **(Automatically cleared)**
OTP_WR2: OTP write function selection for SID[1:0]=LH. **(Automatically cleared)**
OTP_WR3: OTP write function selection for SID[1:0]=HL. **(Automatically cleared)**
OTP_WR4: OTP write function selection for SID[1:0]=HH. **(Automatically cleared)**

OTP_WR1 OTP_WR2 OTP_WR3 OTP_WR4	Function	Note
0	Disable	Default
1	Enable	-

OTP_WR_ALL_ GROUP: Write All OTP_Group enable. **(Automatically cleared)**

OTP_RD	Function	Note
0	Disable	Default
1	Enable	-

OTP_RELOAD: OTP reload function enable. **(Automatically cleared)**

OTP_RELOAD	Function	Note
0	Disable	Default
1	Enable	-

OTP_RD: OTP read function enable. **(Automatically cleared)**

OTP_RD	Function	Note
0	Disable	Default
1	Enable	-

R04h ~ R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	04h	1/0	-	-	-	-	-	-	OTP_INDEX[9:8]	
			-	-	-	-	-	-	0	0
	05h		OTP_INDEX[7:0]							
			0	0	0	0	0	0	0	0

OTP_INDEX[9:0]: OTP address for read.

R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	06h	1	PDOB[7:0]							
			0	0	0	0	0	0	0	0

PDOB[7:0]: OTP read out data. **(Read only)**

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R0Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	0Ah	1/0	EEP_PWD[7:0]							
			0	1	0	1	1	0	1	0

EEP_PWD[7:0]: EEPROM software reload password

EEP_PWD[7:0]								Function	Note
0	0	0	0	0	0	0	0	Disable	-
:	:	:	:	:	:	:	:	Disable	-
0	1	0	1	1	0	1	0	Disable	Default
:	:	:	:	:	:	:	:	Disable	-
1	0	1	0	0	1	0	1	Enable	-
:	:	:	:	:	:	:	:	Disable	-
1	0	0	1	1	0	0	1	Disable	-
:	:	:	:	:	:	:	:	Disable	-
1	1	1	1	1	1	1	1	Disable	-

R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	0Bh	1/0	EEP_CKSUM_FAIL	-	-	-	-	-	-	EEP_RL_CMD
			0	-	-	-	-	-	-	0

EEP_CKSUM_FAIL: EEPROM Check-sum flag. **(Read only)**

EEP_CKSUM_FAIL	Function	Note
0	Check-sum pass	Default
1	Check-sum fail	-

EEP_RL_CMD: EEPROM software reload. **(Automatically cleared)**

EEP_RL_CMD	Function	Note
0	-	Default
1	Reload	-

R0Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	0Ch	1/0	SIDEN_XOR[2:0]			EESEL	-	FCS_XOR[2:0]		
			0	1	0	0	0	0	1	0

SIDEN_XOR[2:0]: XOR with hardwire pin SIDEN

R_SIDEN_XOR[2:0]			Function	Note
0	0	0	Depend on SIDEN hardware pin	-
0	0	1		-
0	1	0		Default
0	1	1		-
1	0	0		-
1	0	1	Inverse SIDEN hardware pin	-
1	1	0	Depend on SIDEN hardware pin	-
1	1	1		-

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EESEL: EEPROM controlled by System or Driver IC

EESEL	Function	Note
0	EEPROM controlled by Driver IC	Default
1	EEPROM controlled by System	-

FCS_XOR[2:0]: XOR with hardwire pin FCS

FCS _XOR[2:0]			Function	Note
0	0	0	Depend on FCS hardware pin	-
0	0	1		-
0	1	0		Default
0	1	1		-
1	0	0		-
1	0	1	Inverse FCS hardware pin	-
1	1	0	Depend on FCS hardware pin	-
1	1	1		-

R0Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	0Dh	1/0	STBYB_XOR[7:0]							
			0	0	0	0	0	0	0	0

STBYB_ XOR[7:0]: Standby mode enable.

STBYB_XOR[7:0]								Function	Note
0	0	0	0	0	0	0	0	Normal mode	Default
0	1	0	1	0	1	0	1	Standby mode	-
Else								Normal mode	-

STBYB Hardware pin	STBYB_XOR	Function	Note
H	Not 55h	Normal mode	-
H	55h	Standby mode	-
L	Not 55h	Standby mode	-
L	55h	Normal mode	-

R0Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	0Eh	1/0	-	-	ATREN_XOR[1:0]		-	-	TS_XOR[1:0]	
			-	-	0	0	-	-	0	0

ATREN_XOR[1:0]:

ATREN Hardware pin	ATREN_XOR	Function	Note
H	Not 11h	Enable auto-reload OTP/EEPROM	-
H	11h	Disable auto-reload OTP/EEPROM	-
L	Not 11h	Disable auto-reload OTP/EEPROM	-
L	11h	Enable auto-reload OTP/EEPROM	-

TS _ XOR[1:0]: Software TS_H/TS_L , HW_PIN xor Reg.

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R0Fh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	0Fh	1	EEP_CKSUM_TCON[7:0]							
			0	0	0	0	0	0	0	0

EEP_CKSUM_TCON[7:0]: EEPROM checksum value calculated by TCON. **(Read only)**

R10h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	10h	1	EEP_CKSUM_DESIRE[7:0]							
			0	0	0	0	0	0	0	0

EEP_CKSUM_DESIRE[7:0]: EEPROM checksum value read from EEPROM. **(Read only)**

R11h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	11h	1	-	-	-	-	-	-	OTP_TRIM_FULL	OTP_TRIM_FLAG
			-	-	-	-	-	-	0	0

OTP_TRIM_FULL: OTP program check flag **(Read only)**.

OTP_TRIM_FULL	Function	Note
0	Not full	-
1	Trimming full	-

OTP_TRIM_FLAG: OTP program check flag **(Read only)**.

OTP_TRIM_FLAG	Function	Note
0	Not fail	-
1	Trimming fail	-

R1Dh ~ R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	1Dh	1/0	NGAMMA_FLAG[2:0]			PGAMMA_FLAG[2:0]			VCOM_FLAG[9:8]	
			0	0	0	0	0	0	0	0
0Bh	1Eh	1/0	VCOM_FLAG[7:0]							
			0	0	0	0	0	0	0	0

NGAMMA_FLAG[2:0]: Flag of negative analog Gamma OTP trimming times. **(Read only)**

NGAMMA_FLAG 2:0]			Function	Note
0	0	0	No trimming	Read only
0	0	1	Trimming 1 time	
0	1	1	Trimming 2 time	
1	1	1	Trimming 3 time	

PGAMMA_FLAG[2:0]: Flag of positive analog Gamma OTP trimming times. **(Read only)**

PGAMMA_FLAG 2:0]			Function	Note
0	0	0	No trimming	Read only
0	0	1	Trimming 1 time	
0	1	1	Trimming 2 time	
1	1	1	Trimming 3 time	

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VCOM_FLAG[9:0]: Flag of VCOM OTP trimming times. **(Read only)**

VCOM_FLAG[9:0]										Function	Note
0	0	0	0	0	0	0	0	0	0	No trimming	Read only
0	0	0	0	0	0	0	0	0	1	Trimming 1 time	
0	0	0	0	0	0	0	0	1	1	Trimming 2 time	
0	0	0	0	0	0	0	1	1	1	Trimming 3 time	
0	0	0	0	0	0	1	1	1	1	Trimming 4 time	
0	0	0	0	0	1	1	1	1	1	Trimming 5 time	
0	0	0	0	1	1	1	1	1	1	Trimming 6 time	
0	0	0	1	1	1	1	1	1	1	Trimming 7 time	
0	0	1	1	1	1	1	1	1	1	Trimming 8 time	
0	1	1	1	1	1	1	1	1	1	Trimming 9 time	
1	1	1	1	1	1	1	1	1	1	Trimming 10 time	

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8.2.14. Page0Ch for LTPS function setting

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	01h	1/0	LTPS_SWB _POFF2[1:0]		LTPS_SWB _POFF1[1:0]		LTPS_SW _POFF2[1:0]		LTPS_SW _POFF1[1:0]	
			1	0	1	1	0	1	0	1

LTPS_SWB_POFF2[1:0]: SWB output level at POFF2 state.

LTPS_SWB_POFF2[1:0]		Function	Note
0	0	VGL	-
0	1	VGH	-
1	0	GND	Default
1	1	GND	-

LTPS_SWB_POFF1[1:0]: SWB output level at POFF1 state.

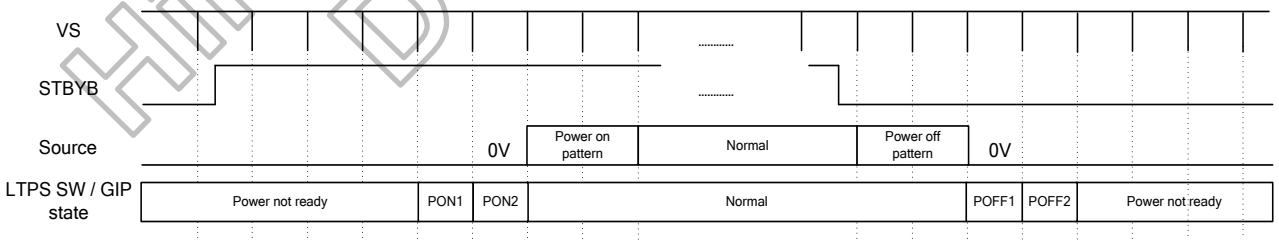
LTPS_SWB_POFF1[1:0]		Function	Note
0	0	VGL	-
0	1	VGH	-
1	0	Active	-
1	1	GND	Default

LTPS_SW_POFF2[1:0]: SW output level at POFF2 state.

LTPS_SW_POFF2[1:0]		Function	Note
0	0	VGL	-
0	1	VGH	Default
1	0	GND	-
1	1	GND	-

LTPS_SW_POFF1[1:0]: SW output level at POFF1 state.

LTPS_SW_POFF1[1:0]		Function	Note
0	0	VGL	-
0	1	VGH	Default
1	0	Active	-
1	1	GND	-



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R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	02h	1/0	LTPS_SWB_PON2[1:0]		-	LTPS_SWB_PON1	LTPS_SW_PON2[1:0]		-	LTPS_SW_PON1
			0	0	-	0	0	0	-	0

LTPS_SWB_PON2[1:0]: SWB output level at PON2 state.

LTPS_SWB_PON2[1:0]		Function	Note
0	0	VGL	Default
0	1	VGH	-
1	0	Active	-
1	1	Active	-

LTPS_SWB_PON1: SWB output level at PON1 state.

LTPS_SWB_PON1	Function	Note
0	VGL	Default
1	VGH	-

LTPS_SW_PON2[1:0]: SW output level at PON2 state.

LTPS_SW_PON2[1:0]		Function	Note
0	0	VGL	Default
0	1	VGH	-
1	0	Active	-
1	1	Active	-

LTPS_SW_PON1: SW output level at PON1 state.

LTPS_SW_PON1	Function	Note
0	VGL	Default
1	VGH	-

R03h ~ R08h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	03h	1/0	LTPS_SW_EQ_EN	LTPS_SW_EQ_VSN_R[6:0]						
			0	0	0	0	0	0	0	0
	04h	1/0	-	LTPS_SW_EQ_GND_R[6:0]						
			-	0	0	0	1	0	0	1
	05h	1/0	-	LTPS_SW_EQ_VSP_R[6:0]						
			-	0	0	0	0	0	0	0
	06h	1/0	-	LTPS_SW_EQ_VSP_F[6:0]						
			-	0	0	0	0	0	0	0
	07h	1/0	-	LTPS_SW_EQ_GND_F[6:0]						
			-	0	0	0	1	0	0	1
	08h	1/0	-	LTPS_SW_EQ_VSN_F[6:0]						
			-	0	0	0	0	0	0	0

LTPS_SW_EQ_EN: LTPS SW output pre-charge enable.

LTPS_SW_EQ_EN	Function	Note
0	Disable	Default
1	Enable	-

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LTPS_SW_EQ_VSN_R[6:0]: Time for LTPS SW output pre-charge from VGL to VSN.

LTPS_SW_EQ_VSN_R[6:0]							Function	Note
0	0	0	0	0	0	0	1T(1)	Default
0	0	0	0	0	0	1	2T(1)	-
:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	65T(1)	-
:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	128T(1)	-

Note: (1) T is the internal oscillator clock unit.

LTPS_SW_EQ_GND_R[6:0]: Time for LTPS SW output pre-charge from VSN to GND.

LTPS_SW_EQ_GND_R[6:0]							Function	Note
0	0	0	0	0	0	0	1T(1)	Default
0	0	0	0	0	0	1	2T(1)	-
:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	65T(1)	-
:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	128T(1)	-

Note: (1) T is the internal oscillator clock unit.

LTPS_SW_EQ_VSP_R[6:0]: Time for LTPS SW output pre-charge from GND to VSP.

LTPS_SW_EQ_VSP_R[6:0]							Function	Note
0	0	0	0	0	0	0	1T(1)	Default
0	0	0	0	0	0	1	2T(1)	-
:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	65T(1)	-
:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	128T(1)	-

Note: (1) T is the internal oscillator clock unit.

LTPS_SW_EQ_VSP_F[6:0]: Time for LTPS SW output pre-charge from VGH to VSP.

LTPS_SW_EQ_VSP_F[6:0]							Function	Note
0	0	0	0	0	0	0	1T(1)	Default
0	0	0	0	0	0	1	2T(1)	-
:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	65T(1)	-
:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	128T(1)	-

Note: (1) T is the internal oscillator clock unit.

LTPS_SW_EQ_GND_F[6:0]: Time for LTPS SW output pre-charge from VSP to GND.

LTPS_SW_EQ_GND_R[6:0]							Function	Note
0	0	0	0	0	0	0	1T(1)	Default
0	0	0	0	0	0	1	2T(1)	-
:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	65T(1)	-
:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	128T(1)	-

Note: (1) T is the internal oscillator clock unit.

LTPS_SW_EQ_VSN_F[6:0]: Time for LTPS SW output pre-charge from GND to VSN.

LTPS_SW_EQ_VSN_F[6:0]							Function	Note
0	0	0	0	0	0	0	1T(1)	Default
0	0	0	0	0	0	1	2T(1)	-
:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	65T(1)	-
:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	128T(1)	-

Note: (1) The unit of T is decided by register SD_CLK_SEL.

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R09h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	09h	1/0	-	-	LTPS_RL_EN_S2 [1:0]		LTPS_RL_EN_S1 [1:0]		LTPS_RL_EN_M [1:0]	
			-	-	0	1	0	1	1	1

LTPS_RL_EN_S2[1:0]: RL side LTPS MUX enable for Slave2 chip **(SID[1:0]=HL)**.
LTPS_RL_EN_S1[1:0]: RL side LTPS MUX enable for Slave1 chip **(SID[1:0]=LH)**.
LTPS_RL_EN_M[1:0]: RL side LTPS MUX enable for mater chip **(SID[1:0]=LL)**.

LTPS_RL_EN_S2[1:0] LTPS_RL_EN_S1[1:0] LTPS_RL_EN_M[1:0]		Function	Note
0	0	Left and right side LTPS MUX both disable	-
0	1	Left side LTPS MUX disable and right side LTPS MUX enable	Default
1	0	Left side LTPS MUX enable and right side LTPS MUX disable	-
1	1	Left and right side LTPS MUX both enable	-

R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	0Ah	1/0	H_TOTAL_OFT[3:0]				LTPS_BANK_F	LTPS_BANK_L[1:0]		-
			0	0	0	0	0	0	0	-

H_TOTAL_OFT[3:0]: H total number offset.

H_TOTAL_OFT[3:0]				Function	Note
0	0	0	0	0T(1)	Default
0	0	0	1	1T(1)	-
:	:	:	:	:	-
1	1	1	1	255T(1)	-

Note: (1) T step = 4*(The unit of T is decided by register SD_CLK_SEL)

LTPS_BANK_F: LTPS bank on sequence setting by frame

LTPS_BANK_F	Function	Note
0	LTPS bank on sequence: bank1→bank2→bank1→bank2	Default
1	LTPS bank on sequence: bank1→bank2**(Frame N)** bank2→bank1**(Frame N+1)**	-

LTPS_BANK_L[1:0]: LTPS bank on sequence setting by line

LTPS_BANK_L[1:0]		Function	Note
0	0	LTPS bank on sequence: bank1→bank2→bank1→bank2	Default
0	1	LTPS bank on sequence: bank1→bank2**(Line N)** bank2→bank1**(Line N+1)**	-
1	x	LTPS bank on sequence **(MUX3 only)**: bank1→bank2→bank3 **(Line N)** bank3→bank2→bank1**(Line N+1)** bank2→bank3→bank1**(Line N+2)**	-

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R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	0Bh	1/0	OSC_DEVI_OFST[2:0]			LTPS_SW_VBLK	-	-	-	-
			0	0	0	0	0	0	0	0

OSC_DEVI_OFST[2:0]: Source OP output compensation.

OSC_DEVI_OFST[2:0]			Function	Note
0	0	0	0T(1)	Default
:	:	:	:	-
1	1	1	7T(1)	-

Note: (1) The unit of T is decided by register SD_CLK_SEL.

LTPS_SW_VBLK: LTPS SW toggle at vertical blanking.

LTPS_SW_VBLK	Function	Note
0	Disable	Default
1	Enable	-

R0Eh ~ R13h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	0Eh	1/0	-	[6:0]						
			-	0	0	0	1	0	0	0
	0Fh		-	TOEF1[6:0]						
			-	0	0	0	1	0	1	0
	10h		-	TOEB2[6:0]						
			-	0	0	0	1	0	0	0
	11h		-	TOEF2[6:0]						
			-	0	0	0	1	0	1	0
	12h		-	TOEB3[6:0]						
			-	0	0	0	1	0	0	0
	13h		-	TOEF3[6:0]						
			-	0	0	0	1	0	1	0

TOEB1[6:0]/TOEB2[6:0]/TOEB3[6:0]: Adjust the LTPS SW1/SW2/SW3 rising time from EQ0

TOEB1[6:0] TOEB2[6:0] TOEB3[6:0]							Function	Note
0	0	0	0	0	0	0	2T(1)	-
0	0	0	0	0	0	1	2T(1)	-
0	0	0	0	0	1	0	2T(1)	-
0	0	0	0	0	1	1	3T(1)	-
:	:	:	:	:	:	:	:	-
0	0	0	1	0	0	0	8T(1)	Default
:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	127T(1)	-

Note: (1) The unit of T is decided by register SD_CLK_SEL.

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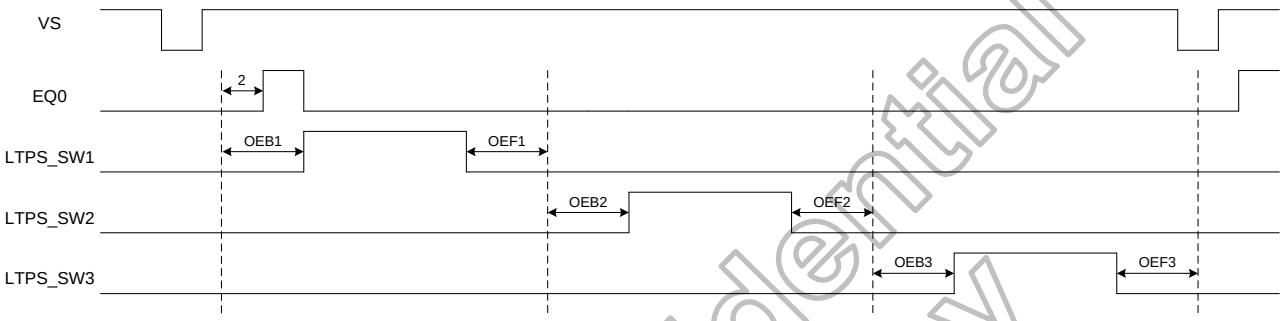
TOEF1[6:0]/TOEF2[6:0]/TOEF3[6:0]: Adjust the LTPS SW1/SW2/SW3 falling time from next EQ0

TOEF1[6:0] TOEF2[6:0] TOEF3[6:0]							Function	Note
0	0	0	0	0	0	0	10T(1)	-
:	:	:	:	:	:	:	:	-
0	0	0	1	0	1	0	10T(1)	Default
0	0	0	1	0	1	1	11T(1)	-
:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	127T(1)	-

Note: (1) The unit of T is decided by register SD_CLK_SEL.



R0Fh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	14h	1/0	BANK12_OFT_LINE1[7:0]							
			0	0	0	0	0	0	0	0
	15h	1/0	BANK23_OFT_LINE1[7:0]							
			0	0	0	0	0	0	0	0
	16h	1/0	BANK12_OFT_LINE2[7:0]							
			0	0	0	0	0	0	0	0
	17h	1/0	BANK23_OFT_LINE2[7:0]							
			0	0	0	0	0	0	0	0
	18h	1/0	BANK12_OFT_LINE3[7:0]							
			0	0	0	0	0	0	0	0
	19h	1/0	BANK23_OFT_LINE3[7:0]							
			0	0	0	0	0	0	0	0

BANK12_OFT_LINE1[7:0]: Shift divided position between Bank1 and Bank2 in line1
BANK12_OFT_LINE2[7:0]: Shift divided position between Bank1 and Bank2 in line2
BANK12_OFT_LINE3[7:0]: Shift divided position between Bank1 and Bank2 in line3

BANK12_OFT_LINE1[7:0] BANK12_OFT_LINE2[7:0] BANK12_OFT_LINE3[7:0]								Function	Note
0	0	0	0	0	0	0	0	0	Default
0	0	0	0	0	0	0	1	Right shift 1T(1)	-
0	0	0	0	0	0	1	0	Right shift 2T(1)	-
:	:	:	:	:	:	:	:	:	-
0	1	1	1	1	1	1	1	Right shift 63T(1)	-
1	0	0	0	0	0	0	0	0	-
1	0	0	0	0	0	0	1	Left shift 1T(1)	-
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	Left shift 63T(1)	-

Note: (1) The unit of T is decided by register SD_CLK_SEL.

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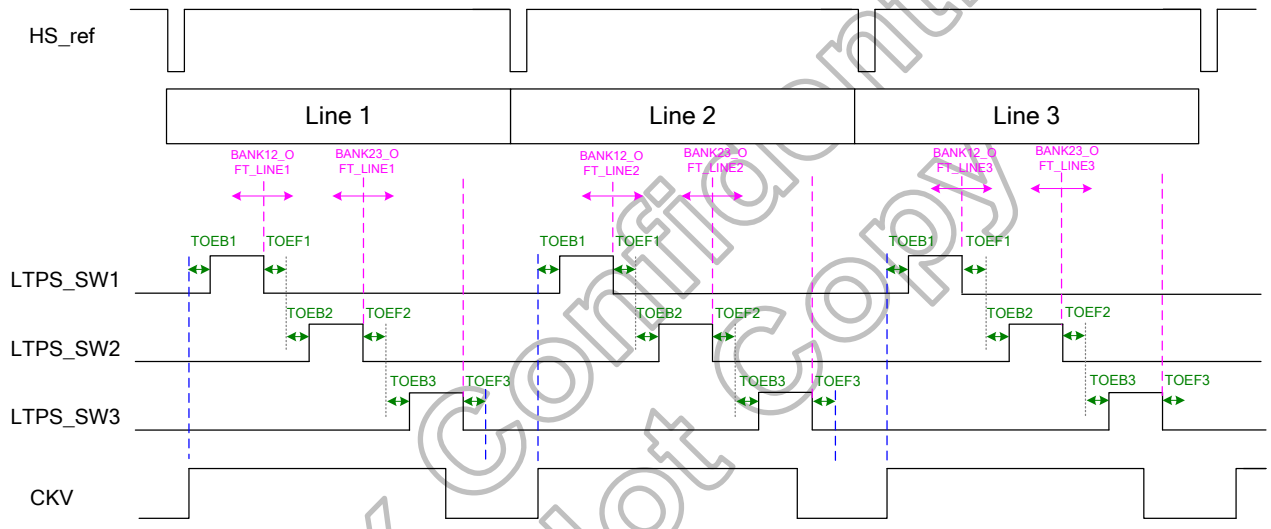
BANK23_OFT_LINE1[7:0]: Shift divided position between Bank2 and Bank3 in line1
BANK23_OFT_LINE2[7:0]: Shift divided position between Bank2 and Bank3 in line2
BANK23_OFT_LINE3[7:0]: Shift divided position between Bank2 and Bank3 in line3

BANK23_OFT_LINE1[7:0] BANK23_OFT_LINE2[7:0] BANK23_OFT_LINE3[7:0]								Function	Note
0	0	0	0	0	0	0	0	0	Default
0	0	0	0	0	0	0	1	Right shift 1T(1)	-
0	0	0	0	0	0	1	0	Right shift 2T(1)	-
:	:	:	:	:	:	:	:	:	-
0	1	1	1	1	1	1	1	Right shift 63T(1)	-
1	0	0	0	0	0	0	0	0	-
1	0	0	0	0	0	0	1	Left shift 1T(1)	-
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	Left shift 63T(1)	-

Note: (1) The unit of T is decided by register SD_CLK_SEL.

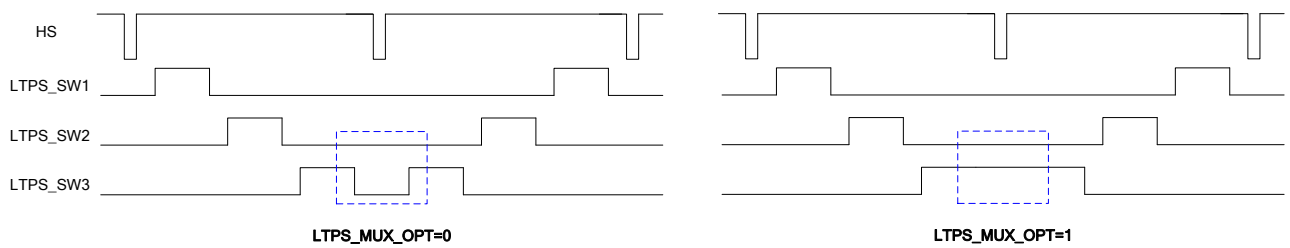


R1Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	1Ah	1/0	LTPS_MUX_OPT	-	-	BANK_OFT_FACTOR	LTPS_SWB_GAS [1:0]		LTPS_SW_GAS [1:0]	
			0	-	-	0	0	1	0	1

LTPS_MUX_OPT: LTPS MUX waveform setting during line switch.

LTPS_MUX_OPT	Function	Note
0	LTPS MUX is alone during line switch	Default
1	LTPS MUX is serial during line switch	-



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BANK_OFT_FACTOR: LTPS register step factor.

BANK_OFT_FACTOR	Function	Note
0	P12R14~P12R19 step is 1T(1)	Default
1	P12R14~P12R19 step is 2T(1)	-

LTPS_SWB_GAS[1:0]: LTPS_SWB state in GAS period.

LTPS_SWB_POFF2[1:0]		Function	Note
0	0	VGL	-
0	1	VGH	Default
1	0	GND	-
1	1	GND	-

LTPS_SW_GAS[1:0]: LTPS_SW state in GAS period.

LTPS_SW_POFF2[1:0]		Function	Note
0	0	VGL	-
0	1	VGH	Default
1	0	GND	-
1	1	GND	-

R12h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	02h	1/0	LTPS_DRVP[1:0]		LTPS_DRVN[1:0]		GIP_DRVP[1:0]		GIP_DRVN[1:0]	
			0	1	0	1	1	1	1	1

LTPS_DRVP[1:0]/LTPS_DRVN[1:0]: LTPS SW output driving ability.

LTPS_DRVP[1:0] LTPS_DRVN[1:0]		Function	Note
0	0	67%	-
0	1	100%	Default
1	0	167%	-
1	1	200%	-

GIP_DRVP[1:0]/GIP_DRVN[1:0]: GIP output driving ability.

GIP_DRVP[1:0] GIP_DRVN[1:0]		Function	Note
0	0	67%	-
0	1	100%	-
1	0	167%	-
1	1	200%	Default

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8.2.15. Page0Dh ~ Page13h for GIP function

Please refer to application note for GIP function.
(OTP group 20~26, and can be programmed 2 times.)

8.2.16. Page14h for ESD and SSC function Cont.

The Page14h registers will set for customer's request.
(OTP group 27 can be programmed 1 time. OTP group 28 can be programmed 2 times.)

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8.2.17. Page15h for Verdor ID function

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	01h	1/0	VENDOR_ID1[7:0]							
			0	0	0	0	0	0	0	0
	02h		VENDOR_ID2[7:0]							
			0	0	0	0	0	0	0	0
	03h		VENDOR_ID3[7:0]							
			0	0	0	0	0	0	0	0
	04h		VENDOR_ID4[7:0]							
			0	0	0	0	0	0	0	0
	05h		VENDOR_ID5[7:0]							
			0	0	0	0	0	0	0	0
	06h		VENDOR_ID6[7:0]							
			0	0	0	0	0	0	0	0
	07h		VENDOR_ID7[7:0]							
			0	0	0	0	0	0	0	0
	08h		VENDOR_ID8[7:0]							
			0	0	0	0	0	0	0	0
	09h		VENDOR_ID9[7:0]							
			0	0	0	0	0	0	0	0
	0Ah		VENDOR_ID10[7:0]							
			0	0	0	0	0	0	0	0
	0Bh		VENDOR_ID11[7:0]							
			0	0	0	0	0	0	0	0
	0Ch		VENDOR_ID12[7:0]							
			0	0	0	0	0	0	0	0
	0Dh		VENDOR_ID13[7:0]							
			0	0	0	0	0	0	0	0
	0Eh		VENDOR_ID14[7:0]							
			0	0	0	0	0	0	0	0
	0Fh		VENDOR_ID15[7:0]							
			0	0	0	0	0	0	0	0
	10h		VENDOR_ID16[7:0]							
			0	0	0	0	0	0	0	0
	11h		VENDOR_ID17[7:0]							
			0	0	0	0	0	0	0	0
	12h		VENDOR_ID18[7:0]							
			0	0	0	0	0	0	0	0
	13h		VENDOR_ID19[7:0]							
			0	0	0	0	0	0	0	0
	14h		VENDOR_ID20[7:0]							
			0	0	0	0	0	0	0	0
	15h		VENDOR_ID21[7:0]							
			0	0	0	0	0	0	0	0

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Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	16h	1/0	VENDOR_ID22[7:0]							
			0	0	0	0	0	0	0	0
	17h		VENDOR_ID23[7:0]							
			0	0	0	0	0	0	0	0
	18h		VENDOR_ID24[7:0]							
			0	0	0	0	0	0	0	0
	19h		VENDOR_ID25[7:0]							
			0	0	0	0	0	0	0	0
	1Ah		VENDOR_ID26[7:0]							
			0	0	0	0	0	0	0	0
	1Bh		VENDOR_ID27[7:0]							
			0	0	0	0	0	0	0	0
	1Ch		VENDOR_ID28[7:0]							
			0	0	0	0	0	0	0	0
	1Dh		VENDOR_ID29[7:0]							
			0	0	0	0	0	0	0	0
	1Eh		VENDOR_ID30[7:0]							
			0	0	0	0	0	0	0	0

VENDOR_ID: LCM information for customer defined.

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8.2.18. Page16h for CRC function setting

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
16h	01h	1/0	-	CRC_CNT_OPT	CRC_TYPE	CRC_MODE[1:0]		CRC_INI_SEL	CRC_IN_SWAP[1:0]	
			-	1	0	0	0	0	0	0

CRC_CNT_OPT: Initial value setting.

CRC_CNT_OPT	Function	Note
0	CRC_ERR_SUM will clear only spi_wr_clear / CRC disable	-
1	CRC_ERR_SUM will clear if compare result meet before fail_flag trigger	Default

CRC_TYPE: CRC polo polynomial selection

CRC_TYPE	Function	Note
0	CRC16 mode	Default
1	CRC32 mode	-

CRC_MODE[1:0]: CRC mode selection.

CRC_MODE[1:0]		Function	Note
0	0	CRC check mode	Default
0	1	CRC auto mode	-
1	0	CRC still mode	-
1	1		-

CRC_INI_SEL: Initial value setting.

CRC_INI_SEL	Function	Note
0	24'h000000	Default
1	24'hFFFFFF	-

CRC_IN_SWAP[1:0]: Input data swap function.

CRC_IN_SWAP[1:0]		Function	Note
0	0	R[7:0], G[7:0], B[7:0]	Default
0	1	R[0:7], G[0:7], B[0:7]	-
1	0	B[7:0], G[7:0], R[7:0]	-
1	1	B[0:7], G[0:7], R[0:7]	-

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R02h ~ R19h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
16h	02h	1/0	CRC_WIN1_H1[11:8]				CRC_WIN1_H2[11:8]			
			0	0	0	0	0	0	0	0
16h	03h	1/0	CRC_WIN1_H1[7:0]							
			0	0	0	0	0	0	0	1
16h	04h	1/0	CRC_WIN1_H2[7:0]							
			1	0	1	0	0	0	0	0
16h	05h	1/0	CRC_WIN1_V1[11:8]				CRC_WIN1_V2[11:8]			
			0	0	0	0	0	0	0	0
16h	06h	1/0	CRC_WIN1_V1[7:0]							
			0	0	0	0	0	0	0	1
16h	07h	1/0	CRC_WIN1_V2[7:0]							
			1	0	0	0	0	0	0	0
16h	08h	1/0	CRC_WIN2_H1[11:8]				CRC_WIN2_H2[11:8]			
			0	0	0	0	0	0	0	0
16h	09h	1/0	CRC_WIN2_H1[7:0]							
			0	0	0	0	0	0	0	1
16h	0Ah	1/0	CRC_WIN2_H2[7:0]							
			1	0	1	0	0	0	0	0
16h	0Bh	1/0	CRC_WIN2_V1[11:8]				CRC_WIN2_V2[11:8]			
			0	0	0	0	0	0	0	0
16h	0Ch	1/0	CRC_WIN2_V1[7:0]							
			0	0	0	0	0	0	0	1
16h	0Dh	1/0	CRC_WIN2_V2[7:0]							
			1	0	0	0	0	0	0	0
16h	0Eh	1/0	CRC_WIN3_H1[11:8]				CRC_WIN3_H2[11:8]			
			0	0	0	0	0	0	0	0
16h	0Fh	1/0	CRC_WIN3_H1[7:0]							
			0	0	0	0	0	0	0	1
16h	10h	1/0	CRC_WIN3_H2[7:0]							
			1	0	1	0	0	0	0	0
16h	11h	1/0	CRC_WIN3_V1[11:8]				CRC_WIN3_V2[11:8]			
			0	0	0	0	0	0	0	0
16h	12h	1/0	CRC_WIN3_V1[7:0]							
			0	0	0	0	0	0	0	1
16h	13h	1/0	CRC_WIN3_V2[7:0]							
			1	0	0	0	0	0	0	0
16h	14h	1/0	CRC_WIN4_H1[11:8]				CRC_WIN4_H2[11:8]			
			0	0	0	0	0	0	0	0
16h	15h	1/0	CRC_WIN4_H1[7:0]							
			0	0	0	0	0	0	0	1
16h	16h	1/0	CRC_WIN4_H2[7:0]							
			1	0	1	0	0	0	0	0
16h	17h	1/0	CRC_WIN4_V1[11:8]				CRC_WIN4_V2[11:8]			
			0	0	0	0	0	0	0	0
16h	18h	1/0	CRC_WIN4_V1[7:0]							
			0	0	0	0	0	0	0	1
16h	19h	1/0	CRC_WIN4_V2[7:0]							
			1	0	0	0	0	0	0	0

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CRC_WIN1_H1[11:0]: Define CRC window1 left side X_ordinate.

CRC_WIN1_H2[11:0]: Define CRC window1 right side X_ordinate.

CRC_WIN1_V1[11:0]: Define CRC window1 Top side Y_ordinate.

CRC_WIN1_V2[11:0]: Define CRC window1 Bottom side Y_ordinate.

CRC_WIN2_H1[11:0]: Define CRC window2 left side X_ordinate.

CRC_WIN2_H2[11:0]: Define CRC window2 right side X_ordinate.

CRC_WIN2_V1[11:0]: Define CRC window2 Top side Y_ordinate.

CRC_WIN2_V2[11:0]: Define CRC window2 Bottom side Y_ordinate.

CRC_WIN3_H1[11:0]: Define CRC window3 left side X_ordinate.

CRC_WIN3_H2[11:0]: Define CRC window3 right side X_ordinate.

CRC_WIN3_V1[11:0]: Define CRC window3 Top side Y_ordinate.

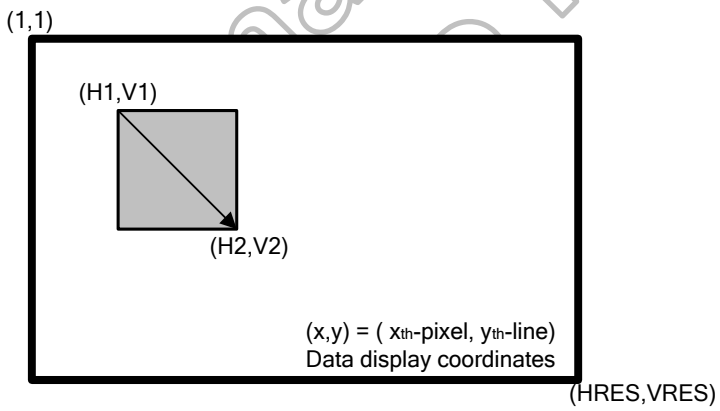
CRC_WIN3_V2[11:0]: Define CRC window3 Bottom side Y_ordinate.

CRC_WIN4_H1[11:0]: Define CRC window4 left side X_ordinate.

CRC_WIN4_H2[11:0]: Define CRC window4 right side X_ordinate.

CRC_WIN4_V1[11:0]: Define CRC window4 Top side Y_ordinate.

CRC_WIN4_V2[11:0]: Define CRC window4 Bottom side Y_ordinate.



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R1Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
16h	1Ah	1/0	CRC_CKSUM_NUM[7:0]							
			0	0	0	0	0	0	1	0

CRC_CKSUM_NUM[7:0]: CRC checksum compare frames .
If still mode disable **(CRC_MODE[1:0]=00)**

CRC_CKSUM_NUM[7:0]								Function		Note
								CRC_CNT_OPT=0	CRC_CNT_OPT=1	
0	0	0	0	0	0	0	0	1 frame	1 frame	-
0	0	0	0	0	0	0	1	32 frames	1 frame	-
0	0	0	0	0	0	1	0	64 frames	2 frames	Default
:	:	:	:	:	:	:	:			-
1	1	1	1	1	1	1	0	254*32 frames	254 frames	-
1	1	1	1	1	1	1	1	255*32 frames	255 frames	-

If still mode enable **(CRC_MODE[1:0]=1x)**

CRC_CKSUM_NUM[7:0]								Function	Note
0	0	0	0	0	0	0	0	1 frame	-
0	0	0	0	0	0	0	1	64 frames	-
0	0	0	0	0	0	1	0	128 frames	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	0	254*64 frames	-
1	1	1	1	1	1	1	1	255*64 frames	-

R1Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
16h	1Bh	1/0	-	-	-	CRC_FUNCTION_EN	CRC4_EN	CRC3_EN	CRC2_EN	CRC1_EN
			-	-	-	0	0	0	0	0

CRC_FUNCTION_EN: CRC function enable.

EXT_CRC_EN Hardware pin	CRC_FUNCTION_EN	Function	Note
L	0	Disable	Default
L	1	Enable	-
H	0	Enable	-
H	1	Disable	-

CRC1_EN/CRC2_EN/CRC3_EN/CRC4_EN: windows function able.

CRC1_EN CRC2_EN CRC3_EN CRC4_EN	Function	Note
0	Disable	Default
1	Enable	-

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8.2.19. Page17h for CRC predict value setting

R01h ~ R10h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
17h	01h	1/0	CRC_PRED_SUM1[31:24]							
			0	0	0	0	0	0	0	0
	02h	1/0	CRC_PRED_SUM1[23:16]							
			0	0	0	0	0	0	0	0
	03h	1/0	CRC_PRED_SUM1[15:8]							
			0	0	0	0	0	0	0	0
	04h	1/0	CRC_PRED_SUM1[7:0]							
			0	0	0	0	0	0	0	0
	05h	1/0	CRC_PRED_SUM2[31:24]							
			0	0	0	0	0	0	0	0
	06h	1/0	CRC_PRED_SUM2[23:16]							
			0	0	0	0	0	0	0	0
	07h	1/0	CRC_PRED_SUM2[15:8]							
			0	0	0	0	0	0	0	0
	08h	1/0	CRC_PRED_SUM2[7:0]							
			0	0	0	0	0	0	0	0
	09h	1/0	CRC_PRED_SUM3[31:24]							
			0	0	0	0	0	0	0	0
	0Ah	1/0	CRC_PRED_SUM3[23:16]							
			0	0	0	0	0	0	0	0
	0Bh	1/0	CRC_PRED_SUM3[15:8]							
			0	0	0	0	0	0	0	0
	0Ch	1/0	CRC_PRED_SUM3[7:0]							
			0	0	0	0	0	0	0	0
	0Dh	1/0	CRC_PRED_SUM4[31:24]							
			0	0	0	0	0	0	0	0
	0Eh	1/0	CRC_PRED_SUM4[23:16]							
			0	0	0	0	0	0	0	0
	0Fh	1/0	CRC_PRED_SUM4[15:8]							
			0	0	0	0	0	0	0	0
	10h	1/0	CRC_PRED_SUM4[7:0]							
			0	0	0	0	0	0	0	0

CRC_PRED_SUM1[31:0]: CRC system predict value for window 1.

CRC_PRED_SUM2[31:0]: CRC system predict value for window 2.

CRC_PRED_SUM3[31:0]: CRC system predict value for window 3.

CRC_PRED_SUM4[31:0]: CRC system predict value for window 4.

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8.2.20. Page18h for CRC calculated value

R01h ~ R10h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
18h	01h	1	CRC_TCON_SUM1[31:24]							
			0	0	0	0	0	0	0	0
	02h	1	CRC_TCON_SUM1[23:16]							
			0	0	0	0	0	0	0	0
	03h	1	CRC_TCON_SUM1[15:8]							
			0	0	0	0	0	0	0	0
	04h	1	CRC_TCON_SUM1[7:0]							
			0	0	0	0	0	0	0	0
	05h	1	CRC_TCON_SUM2[31:24]							
			0	0	0	0	0	0	0	0
	06h	1	CRC_TCON_SUM2[23:16]							
			0	0	0	0	0	0	0	0
	07h	1	CRC_TCON_SUM2[15:8]							
			0	0	0	0	0	0	0	0
	08h	1	CRC_TCON_SUM2[7:0]							
			0	0	0	0	0	0	0	0
	09h	1	CRC_TCON_SUM3[31:24]							
			0	0	0	0	0	0	0	0
	0Ah	1	CRC_TCON_SUM3[23:16]							
			0	0	0	0	0	0	0	0
	0Bh	1	CRC_TCON_SUM3[15:8]							
			0	0	0	0	0	0	0	0
	0Ch	1	CRC_TCON_SUM3[7:0]							
			0	0	0	0	0	0	0	0
	0Dh	1	CRC_TCON_SUM4[31:24]							
			0	0	0	0	0	0	0	0
	0Eh	1	CRC_TCON_SUM4[23:16]							
			0	0	0	0	0	0	0	0
	0Fh	1	CRC_TCON_SUM4[15:8]							
			0	0	0	0	0	0	0	0
	10h	1	CRC_TCON_SUM4[7:0]							
			0	0	0	0	0	0	0	0

CRC_TCON_SUM1[31:0]: CRC TCON calculated value for window 1 **(read only)**.

CRC_TCON_SUM2[31:0]: CRC TCON calculated value for window 2 **(read only)**.

CRC_TCON_SUM3[31:0]: CRC TCON calculated value for window 3 **(read only)**.

CRC_TCON_SUM4[31:0]: CRC TCON calculated value for window 4 **(read only)**.

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R11h ~ R18h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
18h	11h	1	CRC_ERR_CNT1[15:8]							
			0	0	0	0	0	0	0	0
	12h	1	CRC_ERR_CNT1[7:0]							
			0	0	0	0	0	0	0	0
	13h	1	CRC_ERR_CNT2[15:8]							
			0	0	0	0	0	0	0	0
	14h	1	CRC_ERR_CNT2[7:0]							
			0	0	0	0	0	0	0	0
	15h	1	CRC_ERR_CNT3[15:8]							
			0	0	0	0	0	0	0	0
	16h	1	CRC_ERR_CNT3[7:0]							
			0	0	0	0	0	0	0	0
	17h	1	CRC_ERR_CNT4[15:8]							
			0	0	0	0	0	0	0	0
	18h	1	CRC_ERR_CNT4[7:0]							
			0	0	0	0	0	0	0	0

CRC_ERR_CNT1[15:0]: CRC fail accumulated counter for window 1 **(read only)**.

CRC_ERR_CNT2[15:0]: CRC fail accumulated counter for window 2 **(read only)**.

CRC_ERR_CNT3[15:0]: CRC fail accumulated counter for window 3 **(read only)**.

CRC_ERR_CNT4[15:0]: CRC fail accumulated counter for window 4 **(read only)**.

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8.2.21. Page19h for Fail flag (read only)

R01h

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
19h	01h	1/0	PFM NG fail	OTP trim fail	EEPROM fail	No-VIDEO fail	Gate fail	SD_DET fail	OTP full fail	LVDS lock fail
			0	0	0	0	0	0	0	0

R02h

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
19h	02h	1/0	GAS_VGL fail	GAS_PFM fail	GAS_VCC fail	CRC check fail	AGM P/N check sum fail	OTP check sum fail	OTP reload fail	-
			0	0	0	0	0	0	0	-

R03h

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
19h	03h	1/0	OVP VCC fail	OVP VSP fail	OVP VSN fail	OVP VGH fail	OVP VGL fail	OVP VCOM fail	LVD VGH fail	LVD VCOM fail
			0	0	0	0	0	0	0	0

R04h

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
19h	04h	1/0	OVP VGMPL fail	OVP VGMNL fail	OVP VDDD fail	OVP VCL fail	LVD VGMPH fail	LVD VGMNH fail	LVD VSDPN fail	LVD VCL fail
			0	0	0	0	0	0	0	0

Page19h registers are read only for fail flag.

Bit	Function	Note
0	No fail	Default
1	Fail trigglered	-

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8.2.22. Page1Bh for OTP checksum

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1Bh	01h	1/0	OTP_CHECKSUM_GOLD[7:0]							
			0	0	0	0	0	0	0	0

OTP_CHECKSUM_GOLD[7:0]: for OTP checksum comapre.

R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1Bh	02h	1/0	OTP_CHECKSUM[7:0]							
			0	0	0	0	0	0	0	0

OTP_CHECKSUM[7:0]: OTP checksum of group1~29 which calculated by TCON.
(except group9 and group 10)

R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1Bh	03h	1/0	P_CHECKSUM[7:0]							
			0	0	0	0	0	0	0	0

P_CHECKSUM[7:0]: OTP checksum of group 9 which calculated by TCON.

R04h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1Bh	04h	1/0	N_CHECKSUM[7:0]							
			0	0	0	0	0	0	0	0

N_CHECKSUM[7:0]: OTP checksum of group 10 which calculated by TCON.

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8.3. EEPROM mapping table

Index	D7	D6	D5	D4	D3	D2	D1	D0
0	EEP_HEADER = 8'h52							
1	GOA_ENB	PTS[2:0]			ZZS[1:0]		GSEL[1:0]	
2	TR[1:0]		DINT	MODE	HSP	VSP	CLOCKP	NB
3	RL	TB	INV[1:0]		RS[3:0]			
4	RB_INV	DGAMEN	GPOS[1:0]		SD_GND_V[1:0]		PON	POFF
5	GASEN	SPFEN	SPFSEL	BISTEN	SD_CLK_SEL[1:0]		BIST_FNUM[1:0]	
6	VSTS[7:0]							
7	HSTS[7:0]							
8	PWR_SPEED	TS_RHL_OPT	OEW[5:0]					
9	-	-	GEQW[5:0]					
10	PCR[1:0]		EQ0W[5:0]					
11	-	BC[2:0]			POCSD[1:0]		POCGM[1:0]	
12	-	CAS_DEL_OPT[2:0]			RGATE	GM_SWAP	DUAL_F	TP_SYNC_VBLK
13	OSC_BISTS[1:0]		BISTS_CLK_SEL[1:0]		BIST_VFP[3:0]			
14	-	-	ROB[5:0]					
15	-	-	GOB[5:0]					
16	-	-	BOB[5:0]					
17	RGC[7:0]							
18	GGC[7:0]							
19	BGC[7:0]							
20	GATENUM[7:0]							
21	GATEPASS[3:0]				GATENUM[11:8]			
22	HSETNUM[7:0]							
23	HSETPASS[3:0]				HSETNUM[11:8]			
24	BIST_H_OFFSET[7:0]							
25	-	BIST_OSC_SEL_EN	H_ODCLK_SEL[5:0]					
26	-	-	-	-	-	-	-	-
27	-	-	-	-	-	-	-	-
28	POL_INV_FRM[3:0]				EQ0_OPT	-	PRE-SCAN[1:0]	
29	BIST_GRAY[7:0]							
30	DMY_DATA[7:0]							
31	-	PFMFREN	VSPEN	VSNEN	DRVPD[1:0]		DRVND[1:0]	
32	VMONPS[1:0]		T_OCPEN	VSPS[4:0]				
33	VMONNS[1:0]		VCOM_OTP	VSNS[4:0]				
34	-	VGHS[6:0]						
35	-	VGLXS	VGLS[5:0]					
36	VSPON[4]	VSNON[4]	POFF_GAS_EN	VSDPS[4:0]				
37	-	-	CAS_VGHL_OPT	VSDNS[4:0]				
38	VSPON[3:0]				VSPOFF[3:0]			
39	VSNON[3:0]				VSNOFF[3:0]			
40	VSPON_SS2[3:0]				VSPOFF_SS2[3:0]			
41	VSNON_SS2[3:0]				VSNOFF_SS2[3:0]			
42	GAS_VCC_EN	VGHXS[1:0]		VCOMEN	S_VCL_ENB	M_VCL_ENB	VCOMD[1:0]	
43	VGHL_LIMIT	VGHEN	VGLEN	-	PFM_SS_SEL	POL_TOG_VBLK	FCP[1:0]	
44	GAS_VGL_EN	T_SCPEN	T_VGMREGEN	T_VGMPHS[4:0]				
45	GASVCIS[2:0]			T_VGMNHS[4:0]				
46	T_VGMPLS[3:0]				T_VGMNLS[3:0]			
47	DCHG2R[1:0]		DCHG2ON[1:0]		DCHG1R[1:0]		DCHG1ON[1:0]	
48	-	POFF_BLACK_NUM	PON_BLACK_NUM[1:0]		-	VCLS[2:0]		
49	-	-	LTPS_GIP_PWR_OPT	LOAD_OPT	-	-	TFVBAT1[1:0]	
50	VSPON_SS1[3:0]				VSPOFF_SS1[3:0]			

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Index	D7	D6	D5	D4	D3	D2	D1	D0
51	VSNON_SS1[3:0]				VSNOFF_SS1[3:0]			
52	-	-	-	-	-	-	-	-
53	-	-	-	-	-	-	-	-
54	PTSEL[15:8]							
55	PTSEL[7:0]							
56	-	-	-	-	-	-	-	OFF_VCOM[8]
57	OFF_VCOM[7:0]							
58	VCOM_OFST[7:0]							
59	-	-	-	-	-	-	-	VCOMS[8]
60	VCOMS[7:0]							
61	(RT)	-	-	T_VP1_0[4:0]				
62	-	-	T_VP1_2[5:0]					
63	-	-	T_VP1_4[5:0]					
64	-	-	T_VP1_8[5:0]					
65	-	-	T_VP1_14[5:0]					
66	-	-	T_VP1_22[5:0]					
67	-	-	T_VP1_30[5:0]					
68	-	-	T_VP1_47[5:0]					
69	-	-	T_VP1_79[5:0]					
70	-	-	T_VP1_111[5:0]					
71	-	-	T_VP1_143[5:0]					
72	-	-	T_VP1_175[5:0]					
73	-	-	T_VP1_207[5:0]					
74	-	-	T_VP1_224[5:0]					
75	-	-	T_VP1_232[5:0]					
76	-	-	T_VP1_240[5:0]					
77	-	-	T_VP1_246[5:0]					
78	-	-	T_VP1_251[5:0]					
79	-	-	T_VP1_253[5:0]					
80	-	-	T_VP1_255[5:0]					
81	P_checksum[7:0]							
82	(LT)	-	-	T_VP2_0[4:0]				
83	-	-	T_VP2_2[5:0]					
84	-	-	T_VP2_4[5:0]					
85	-	-	T_VP2_8[5:0]					
86	-	-	T_VP2_14[5:0]					
87	-	-	T_VP2_22[5:0]					
88	-	-	T_VP2_30[5:0]					
89	-	-	T_VP2_47[5:0]					
90	-	-	T_VP2_79[5:0]					
91	-	-	T_VP2_111[5:0]					
92	-	-	T_VP2_143[5:0]					
93	-	-	T_VP2_175[5:0]					
94	-	-	T_VP2_207[5:0]					
95	-	-	T_VP2_224[5:0]					
96	-	-	T_VP2_232[5:0]					
97	-	-	T_VP2_240[5:0]					
98	-	-	T_VP2_246[5:0]					
99	-	-	T_VP2_251[5:0]					
100	-	-	T_VP2_253[5:0]					
101	-	-	T_VP2_255[5:0]					
102	P_checksum[7:0]							
103	(HT)	-	-	T_VP3_0[4:0]				
104	-	-	T_VP3_2[5:0]					
105	-	-	T_VP3_4[5:0]					
106	-	-	T_VP3_8[5:0]					
107	-	-	T_VP3_14[5:0]					
108	-	-	T_VP3_22[5:0]					
109	-	-	T_VP3_30[5:0]					
110	-	-	T_VP3_47[5:0]					
111	-	-	T_VP3_79[5:0]					
112	-	-	T_VP3_111[5:0]					
113	-	-	T_VP3_143[5:0]					

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Index	D7	D6	D5	D4	D3	D2	D1	D0
114	-	-	T_VP3_175[5:0]					
115	-	-	T_VP3_207[5:0]					
116	-	-	T_VP3_224[5:0]					
117	-	-	T_VP3_232[5:0]					
118	-	-	T_VP3_240[5:0]					
119	-	-	T_VP3_246[5:0]					
120	-	-	T_VP3_251[5:0]					
121	-	-	T_VP3_253[5:0]					
122	-	-	T_VP3_255[5:0]					
123	P_checksum[7:0]							
124	(RT)	-	-	T_VN1_0[4:0]				
125	-	-	T_VN1_2[5:0]					
126	-	-	T_VN1_4[5:0]					
127	-	-	T_VN1_8[5:0]					
128	-	-	T_VN1_14[5:0]					
129	-	-	T_VN1_22[5:0]					
130	-	-	T_VN1_30[5:0]					
131	-	-	T_VN1_47[5:0]					
132	-	-	T_VN1_79[5:0]					
133	-	-	T_VN1_111[5:0]					
134	-	-	T_VN1_143[5:0]					
135	-	-	T_VN1_175[5:0]					
136	-	-	T_VN1_207[5:0]					
137	-	-	T_VN1_224[5:0]					
138	-	-	T_VN1_232[5:0]					
139	-	-	T_VN1_240[5:0]					
140	-	-	T_VN1_246[5:0]					
141	-	-	T_VN1_251[5:0]					
142	-	-	T_VN1_253[5:0]					
143	-	-	T_VN1_255[5:0]					
144	N_checksum[7:0]							
145	(LT)	-		T_VN2_0[4:0]				
146	-	-	T_VN2_2[5:0]					
147	-	-	T_VN2_4[5:0]					
148	-	-	T_VN2_8[5:0]					
149	-	-	T_VN2_14[5:0]					
150	-	-	T_VN2_22[5:0]					
151	-	-	T_VN2_30[5:0]					
152	-	-	T_VN2_47[5:0]					
153	-	-	T_VN2_79[5:0]					
154	-	-	T_VN2_111[5:0]					
155	-	-	T_VN2_143[5:0]					
156	-	-	T_VN2_175[5:0]					
157	-	-	T_VN2_207[5:0]					
158	-	-	T_VN2_224[5:0]					
159	-	-	T_VN2_232[5:0]					
160	-	-	T_VN2_240[5:0]					
161	-	-	T_VN2_246[5:0]					
162	-	-	T_VN2_251[5:0]					
163	-	-	T_VN2_253[5:0]					
164	-	-	T_VN2_255[5:0]					
165	N_checksum[7:0]							
166	(HT)	-	-	T_VN3_0[4:0]				
167	-	-	T_VN3_2[5:0]					
168	-	-	T_VN3_4[5:0]					
169	-	-	T_VN3_8[5:0]					
170	-	-	T_VN3_14[5:0]					
171	-	-	T_VN3_22[5:0]					
172	-	-	T_VN3_30[5:0]					
173	-	-	T_VN3_47[5:0]					
174	-	-	T_VN3_79[5:0]					
175	-	-	T_VN3_111[5:0]					
176	-	-	T_VN3_143[5:0]					

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Index	D7	D6	D5	D4	D3	D2	D1	D0
177	-	-	T_VN3_175[5:0]					
178	-	-	T_VN3_207[5:0]					
179	-	-	T_VN3_224[5:0]					
180	-	-	T_VN3_232[5:0]					
181	-	-	T_VN3_240[5:0]					
182	-	-	T_VN3_246[5:0]					
183	-	-	T_VN3_251[5:0]					
184	-	-	T_VN3_253[5:0]					
185	-	-	T_VN3_255[5:0]					
186	N_checksum[7:0]							
187	FAIL_DET_SEL	FAIL_DET_INV	ASIL_PRIOR_SEL	ASIL_NOSIG_SEL	ASIL_INV	ASIL_PSEL[2:0]		
188	-	-	SD_DET_EN	PON_FDET_EN	CRC4_FAIL_ENB	CRC3_FAIL_ENB	CRC2_FAIL_ENB	CRC1_FAIL_ENB
189	PFM_NG_FAIL_ENB	OTP_TRIM_FAIL_ENB	EEPROM_FAIL_ENB	NOVIDEO_FAIL_ENB	GATE_FAIL_ENB	SOURCE_FAIL_ENB	OTP_FULL_FAIL_ENB	LVDS_FAIL_ENB
190	GAS_VGL_FAIL_ENB	GAS_PFM_FAIL_ENB	GAS_VCC_FAIL_ENB	CAS_FAIL_ENB	OTP_CKSUM_FAIL2_ENB	OTP_CHKSUM_FAIL_ENB	OTP_RL_FAIL_ENB	GLA_FAIL_ENB
191	OVP_VCC_ENB	OVP_VSP_ENB	OVP_VSN_ENB	OVP_VGH_ENB	OVP_VGL_ENB	OVP_VCOM_ENB	LVD_VGH_ENB	LVD_VCOM_ENB
192	OVP_VGMPL_ENB	OVP_VGMNL_ENB	OVP_VDDD_ENB	OVP_VCL_ENB	LVD_VGMPH_ENB	LVD_VGMNH_ENB	LVD_VSDPN_ENB	LVD_VCL_ENB
193	-	-	-	-	PFM_NG_ACT	OTP_TRIM_FAIL_ACT	EEPROM_OTP_FAIL_ACT	GATE_SD_FAIL_ACT
194	CRC_FAIL_ACT[1:0]		GAS_VGL_FAIL_ACT[1:0]		GAS_PFM_FAIL_ACT[1:0]		GAS_VCC_FAIL_ACT[1:0]	
195	-	-	-	VGMA_PWR_NG_ACT	VCOM_NG_ACT	OVP_PWR_ACT	LVD_PWR_ACT	LVD_VCL_ACT
196	-	-	-	-	-	-	-	-
197	PFM_DET_EN	PFM_DET_OPT	PFM_REDET_OPT	DPFN_OSC_SEL	-	-	-	-
198	CROSS_TALK_GRAY	FLICK_GRAY	GIP_MX_TAB_SEL[1:0]		-	GAS_OTP_SELB	RESET_SLP_OPT	-
199	ENDRVN[1:0]		ENDRVP[1:0]		-	-	-	-
200	PON_FAIL_EN1[7:0]							
201	PON_FAIL_EN2[7:0]							
202	TP_DLY[7:0]							
203	TP_WIDTH[7:0]							
204	TP_SYNC_INV	TP_SYNC1_SEL[2:0]			TP_WIDTH_ENB	TP_SYNC2_SEL[2:0]		
205	GIP_RL_EN_S3[1:0]		GIP_RL_EN_S2[1:0]		GIP_RL_EN_S1[1:0]		GIP_RL_EN_M[1:0]	
206	L_GIP_VGH_SEL[19:16]				R_GIP_VGH_SEL[19:16]			
207	L_GIP_VGH_SEL[15:8]							
208	L_GIP_VGH_SEL[7:0]							
209	R_GIP_VGH_SEL[15:8]							
210	R_GIP_VGH_SEL[7:0]							
211	Pgae0x05/Register0x01							
212	Pgae0x05/Register0x02							
213	Pgae0x05/Register0x03							
214	Pgae0x05/Register0x04							
215	Pgae0x05/Register0x05							
216	Pgae0x05/Register0x06							
217	Pgae0x05/Register0x07							
218	Pgae0x05/Register0x08							
219	Pgae0x05/Register0x09							
220	Pgae0x05/Register0x0A							
221	Pgae0x05/Register0x0B							
222	DGMA1R[7:0]							
223	DGMA2R[7:0]							
224	DGMA3R[7:0]							
225	DGMA4R[7:0]							
226	DGMA5R[7:0]							
227	DGMA6R[7:0]							

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Index	D7	D6	D5	D4	D3	D2	D1	D0
228	DGMA7R[7:0]							
229	DGMA8R[7:0]							
230	DGMA9R[7:0]							
231	DGMA10R[7:0]							
232	DGMA11R[7:0]							
233	DGMA12R[7:0]							
234	DGMA13R[7:0]							
235	DGMA14R[7:0]							
236	DGMA15R[7:0]							
237	DGMA16R[7:0]							
238	DGMA17R[7:0]							
239	DGMA18R[7:0]							
240	DGMA19R[7:0]							
241	DGMA20R[7:0]							
242	DGMA21R[7:0]							
243	DGMA22R[7:0]							
244	DGMA23R[7:0]							
245	DGMA24R[7:0]							
246	DGMA1R[9:8]		DGMA2R[9:8]		DGMA3R[9:8]		DGMA4R[9:8]	
247	DGMA5R[9:8]		DGMA6R[9:8]		DGMA7R[9:8]		DGMA8R[9:8]	
248	DGMA9R[9:8]		DGMA10R[9:8]		DGMA11R[9:8]		DGMA12R[9:8]	
249	DGMA13R[9:8]		DGMA14R[9:8]		DGMA15R[9:8]		DGMA16R[9:8]	
250	DGMA17R[9:8]		DGMA18R[9:8]		DGMA19R[9:8]		DGMA20R[9:8]	
251	DGMA21R[9:8]		DGMA22R[9:8]		DGMA23R[9:8]		DGMA24R[9:8]	
252	DGMA1G[7:0]							
253	DGMA2G[7:0]							
254	DGMA3G[7:0]							
255	DGMA4G[7:0]							
256	DGMA5G[7:0]							
257	DGMA6G[7:0]							
258	DGMA7G[7:0]							
259	DGMA8G[7:0]							
260	DGMA9G[7:0]							
261	DGMA10G[7:0]							
262	DGMA11G[7:0]							
263	DGMA12G[7:0]							
264	DGMA13G[7:0]							
265	DGMA14G[7:0]							
266	DGMA15G[7:0]							
267	DGMA16G[7:0]							
268	DGMA17G[7:0]							
269	DGMA18G[7:0]							
270	DGMA19G[7:0]							
271	DGMA20G[7:0]							
272	DGMA21G[7:0]							
273	DGMA22G[7:0]							
274	DGMA23G[7:0]							
275	DGMA24G[7:0]							
276	DGMA1G[9:8]		DGMA2G[9:8]		DGMA3G[9:8]		DGMA4G[9:8]	
277	DGMA5G[9:8]		DGMA6G[9:8]		DGMA7G[9:8]		DGMA8G[9:8]	
278	DGMA9G[9:8]		DGMA10G[9:8]		DGMA11G[9:8]		DGMA12G[9:8]	
279	DGMA13G[9:8]		DGMA14G[9:8]		DGMA15G[9:8]		DGMA16G[9:8]	
280	DGMA17G[9:8]		DGMA18G[9:8]		DGMA19G[9:8]		DGMA20G[9:8]	
281	DGMA21G[9:8]		DGMA22G[9:8]		DGMA23G[9:8]		DGMA24G[9:8]	
282	DGMA1B[7:0]							
283	DGMA2B[7:0]							
284	DGMA3B[7:0]							
285	DGMA4B[7:0]							
286	DGMA5B[7:0]							
287	DGMA6B[7:0]							
288	DGMA7B[7:0]							
289	DGMA8B[7:0]							
290	DGMA9B[7:0]							
291	DGMA10B[7:0]							

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Index	D7	D6	D5	D4	D3	D2	D1	D0
292	DGMA11B[7:0]							
293	DGMA12B[7:0]							
294	DGMA13B[7:0]							
295	DGMA14B[7:0]							
296	DGMA15B[7:0]							
297	DGMA16B[7:0]							
298	DGMA17B[7:0]							
299	DGMA18B[7:0]							
300	DGMA19B[7:0]							
301	DGMA20B[7:0]							
302	DGMA21B[7:0]							
303	DGMA22B[7:0]							
304	DGMA23B[7:0]							
305	DGMA24B[7:0]							
306	DGMA1B[9:8]		DGMA2B[9:8]		DGMA3B[9:8]		DGMA4B[9:8]	
307	DGMA5B[9:8]		DGMA6B[9:8]		DGMA7B[9:8]		DGMA8B[9:8]	
308	DGMA9B[9:8]		DGMA10B[9:8]		DGMA11B[9:8]		DGMA12B[9:8]	
309	DGMA13B[9:8]		DGMA14B[9:8]		DGMA15B[9:8]		DGMA16B[9:8]	
310	DGMA17B[9:8]		DGMA18B[9:8]		DGMA19B[9:8]		DGMA20B[9:8]	
311	DGMA21B[9:8]		DGMA22B[9:8]		DGMA23B[9:8]		DGMA24B[9:8]	
312	-	DLL_BANK	LVDS_AGING	LVDS_FMT	LANE_SW	LANE_PN	LVDS_PULL[1:0]	
313	-	-	LVDS_BW[1:0]		LVDS_CPB[3:0]			
314	RX_VB[1:0]		LVDS_VBDLL[1:0]		S3_EQ_OPT	S2_EQ_OPT	S1_EQ_OPT	M_EQ_OPT
315	S3_EQ_SW[1:0]		S2_EQ_SW[1:0]		S1_EQ_SW[1:0]		M_EQ_SW[1:0]	
316	-	-	-	-	-	-	VCOMS_HT[8]	VCOMS_LT[8]
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318	VCOMS_LT[7:0]							
319	-	VGHS_HT[6:0]						
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322	DIM_OPT	-	VGLS_LT[5:0]					
323	DIM_EN	DIM_FRAME[1:0]		VGMPHS_HT[4:0]				
324	TS_GOE_EN	TS_GAMMA_EN	-	VGMNHS_HT[4:0]				
325	VGMPLS_HT[3:0]				VGMNLS_HT[3:0]			
326	-	TS_VCOM_EN	TS_VGHL_EN	VGMPHS_LT[4:0]				
327	-	-	-	VGMNHS_LT[4:0]				
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330	LTPS_SWB_PON2[1:0]		LTPS_SWB_PON1[1:0]		LTPS_SW_PON2[1:0]		LTPS_SW_PON1[1:0]	
331	LTPS_SW_EQ_EN	LTPS_SW_EQ_VSN_R[6:0]						
332	-	LTPS_SW_EQ_GND_R[6:0]						
333	-	LTPS_SW_EQ_VSP_R[6:0]						
334	-	LTPS_SW_EQ_VSN_F[6:0]						
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338	H_total_oft[3:0]				LTPS_BANK_F	LTPS_BANK_L[1:0]		LTPS_POL
339	OSC_DEVI_OFST[2:0]			LTPS_SW_VBLK	LTPS_SW_BP[1:0]		LTPS_SW_FP[1:0]	
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341	PRE_WD[7:0]							
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9. DC Characteristics

9.1. Absolute maximum ratings(1)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Main power supply	VCC1/VCC1P	-0.3	-	4.0	V
Power supply for internal reference	VCC2	-0.3	-	4.0	V
I/O power supply	VCCIF	-0.3	-	4.0	V
Power supply for source driver	VSP	-0.3	-	7.7	V
Power supply for source driver	VSN	-7.7	-	0.3	V
Programming voltage (Under 5sec)	VDD_OTP	-0.3	-	8.7	V
VCOM power supply	VCOM	-3.5	-	2.5	V
Power supply for gate driver/MUX	VGH	-0.25	-	24.5	V
Power supply for gate driver/MUX	VGL	-16.5	-	0.25	V
Power supply for VGH-VGL	VGH-VGL	<32			V
Storage temperature	T_{ST}	-55	-	+125	℃
Operating temperature	T_A	-40	-	+105	℃
Junction temperature	T_{JC}	-	-	+125	℃
Digital I/O input signals: Input interface pins Input control pins,group1 Input control pins,group2 Serial interface pins Cascade and gate driver control pins Please refer to Ch. 4.1. Pin description	V_{IO}	-0.3	-	VCC1 + 0.3	V

Note: (1) Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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9.2. Recommended operating conditions and electrical characteristics

9.2.1. For the digital circuit: Normal mode

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40℃ to +105℃)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Operating frequency, TTL mode	F_{TTL}	-	5.25	-	60	MHz
Operating frequency, LVDS mode	F_{LVDS}	1-port	15	-	115	MHz
		2-port	15	-	105	MHz
Supply voltage	VCC1 VCC1P VCC2 VCCIF	-	3.0	3.3	3.6	V
Internal digital operating voltage	VDDD VDDIF	-	1.4	1.5	1.6	V
OTP programming voltage	VDD_OTP	Current loading @10mA	8.5	8.6	8.7	V
Low level input voltage	V_{IL}	-	VSS1-0.3	-	0.3 X VCC1	V
High level input voltage	V_{IH}	-	0.7 X VCC1	-	VCC1+0.3	V
High level output voltage	V_{OH}	-	VCC1-0.4	-	-	V
Low level output voltage	V_{OL}	-	GND	-	GND+0.4	V
Pull low/high resistor	R_I	For I/O circuit	150	350	550	KΩ

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9.2.2. For the digital circuit: LVDS mode

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40℃ to +105℃)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Differential input high Threshold voltage	V_{TH}	V_{CM}=1.2V	+0.10	-	-	V
Differential input low threshold voltage	V_{TL}	V_{CM} =1.2V	-	-	-0.10	V
Differential input common Mode voltage	V_{CM}	-	1	1.2	1.7-|V_{ID}|/2	V
LVDS input voltage	V_{INLV}	-	0.7	-	1.7	V
Differential input voltage	|V_{ID}|	-	0.1	-	0.6	V
Differential input leakage Current	I_{LVLEAK}	-	-10	-	+10	μA

Table 9.1: LVDS mode DC electrical characteristics

Single-ended:
LVCLKP,
LVCLKN,
LVD[3:0]P,
LVD[3:0]N

Differential:
LVCLKP-LVCLKN,
LVD[3:0]P-LVD[3:0]N

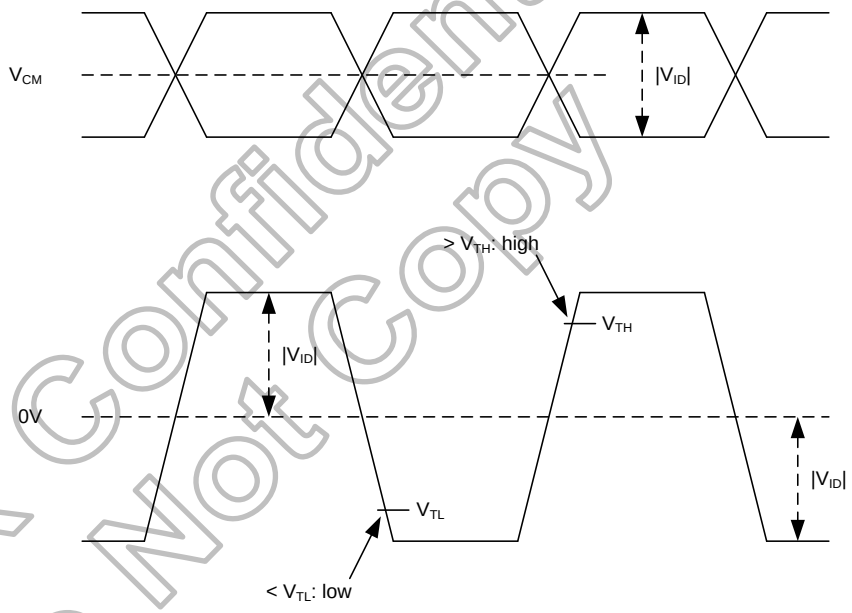

Figure 9.1: LVDS mode DC electrical characteristics

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9.2.3. For the analog circuit: Normal mode

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40℃ to +105℃)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Analog positive supply voltage	VSP	VSP is generated by PFM, VSPS[4:0]=14h, with proper settings and components.	6.7	7	7.3	V
Analog negative supply voltage	VSN	VSN is generated by PFM, VSNS[4:0]=14h, with proper settings and components.	-7.3	-7	-6.7	V
Source driver positive supply voltage	VSDP	VSP≧7V, VSDPS[4:0]=14h, loading current=0	6.65	6.8	6.95	V
Source driver negative supply voltage	VSDN	VSN=-7V, VSDNS[4:0]=14h, loading current=0	-6.95	-6.8	-6.65	V
Internal regulator output for negative level shifter	VCL	-	-2.62	-2.75	-2.88	V
Output for positive gamma reference high voltage	VGMPHO	VSDP≧6.8V, VGMPHS[4:0]=0x1Ah	6.48	6.6	6.72	V
Output for positive gamma reference low voltage	VGMPLO	VGMPLS[4:0]=0x02h	0.12	0.2	0.28	V
Output for negative gamma reference high voltage	VGMNHO	VSDN≦-6.8V, VGMNHS[4:0]=0x1Ah	-6.72	-6.6	-6.48	V
Output for negative gamma reference low voltage	VGMNLO	VGMNLS[4:0]=0x02h	-0.28	-0.2	-0.12	V
VCOM voltage	VCOM	VCOMS[8:0]=0x15Ch	-1.53	-1.48	-1.43	V
Source output voltage, positive polarity	V_{SDOP}	-	0.2	-	VSDP-0.2	V
Source output voltage, negative polarity	V_{SDON}	-	VSDN+0.2	-	-0.2	V
Output for GIP/gate driver positive power supply	VGH	VGH is generated by charge pump, VGHS[6:0]=0x1Ch, loading current=0	11	12	13	V
Output for GIP/gate driver negative power supply	VGL	VGL is generated by charge pump, VGLS[5:0]=0x0Ch, loading current=0	-9	-8	-7	V
Source output voltage deviation	V_{OD}	V_{SDOP}=0.5V to VSDP-0.5V, V_{SDON}=VSDN+0.5V to -0.5V	-	-	10	mV
		V_{SDOP}=0.2V to 0.5V or V_{SDOP}=VSDP-0.5V to VSDP-0.2V, V_{SDON}=VSDN+0.2V to VSDN+0.5V or V_{SDON}=-0.5V to -0.2V	-	-	15	mV
Standby current **(VCC1 + VCC2)**	I_{STBvcc}	STBYB=L and all inputs are default.	-	-	400	μA
Standby current **(VSN or VSP)**	I_{STB}	STBYB=L, VSP or VSN external input	-	-	100	μA

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9.2.4. LVDS mode AC electrical characteristics

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40℃ to +105℃)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock frequency **(1-port/2-port)**	F_{LVCYC}	15	-	115/105	MHz
Clock period **(1-port/2-port)**	T_{LVCYC}	8.69/9.52	-	-	ns
1 data bit time	UI	-	$1/7T_{LVCYC}$	-	ns
Clock high time	T_{LVCH}	-	4	-	UI
Clock low time	T_{LVCL}	-	3	-	UI
Position 1	T_{POS1}	-0.2	0	0.2	UI
Position 0	T_{POS0}	0.8	1	1.2	UI
Position 6	T_{POS6}	1.8	2	2.2	UI
Position 5	T_{POS5}	2.8	3	3.2	UI
Position 4	T_{POS4}	3.8	4	4.2	UI
Position 3	T_{POS3}	4.8	5	5.2	UI
Position 2	T_{POS2}	5.8	6	6.2	UI
Input eye width	T_{EYEW}	0.6	-	-	UI
Input eye border	T_{EX}	-	-	0.2	UI
LVDS wake up time	T_{ENLVDS}	-	-	150	µs
LVDS port to port skew	T_{skew_EO}	-1		1	UI

Table 9.2: LVDS mode AC electrical characteristics

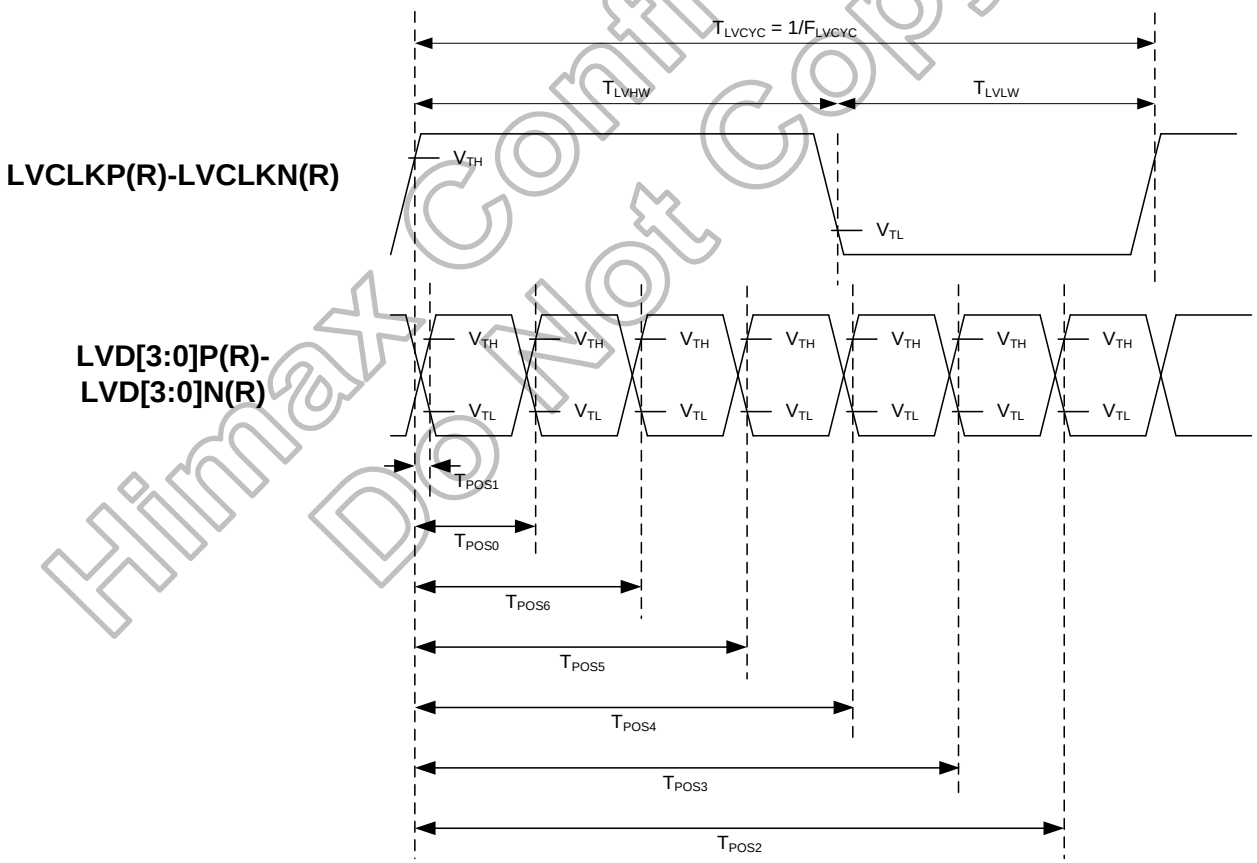

Figure 9.2: LVDS input timing

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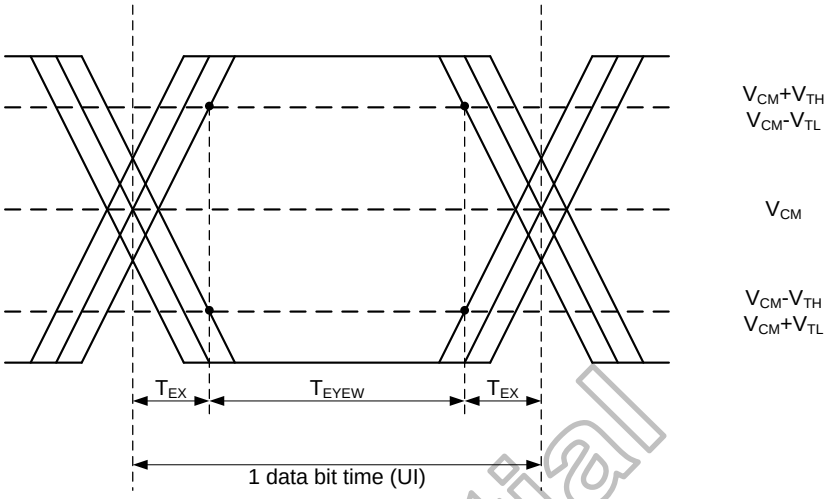
Single-ended:
LVD[3:0]P,
LVD[3:0]N



Differential:
LVD[3:0]P-LVD[3:0]N

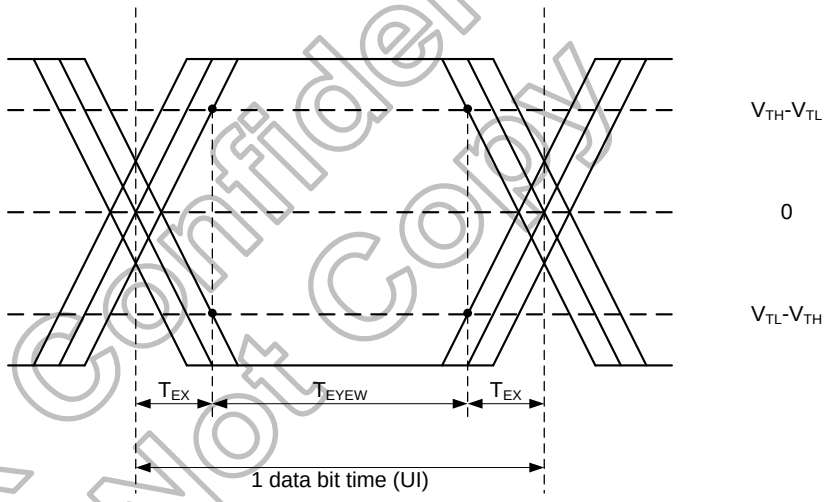


Figure 9.3: LVDS input eye diagram

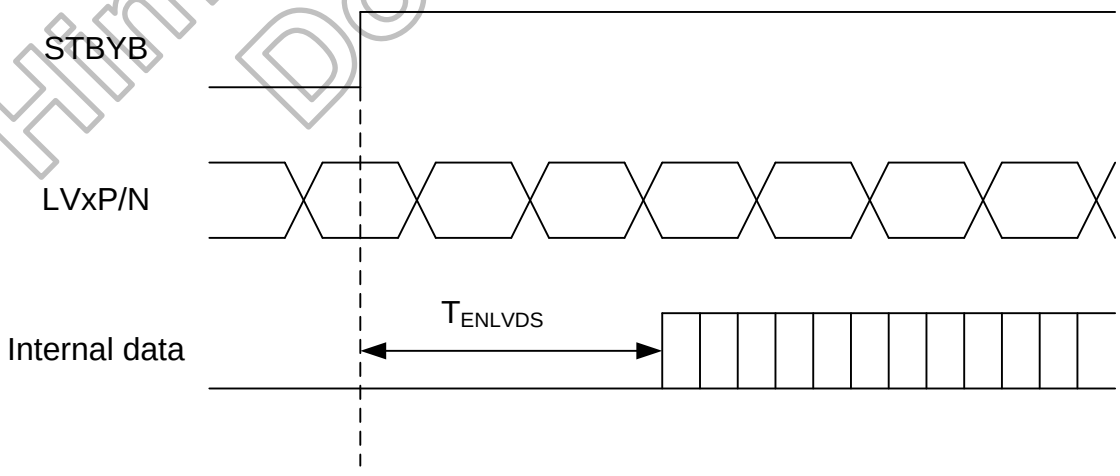


Figure 9.4: LVDS wake up time

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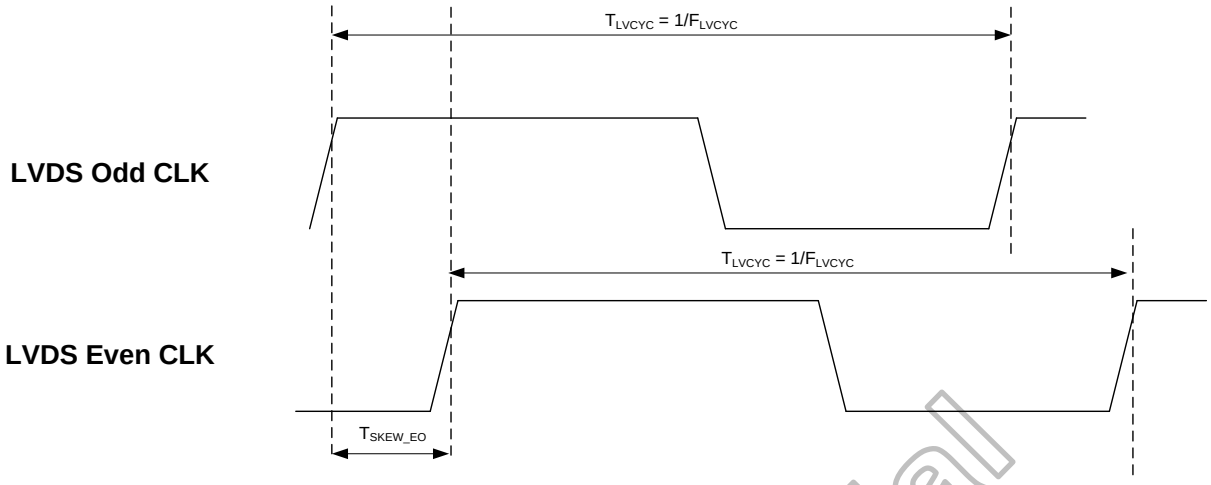

Figure 9.5: LVDS clock to clock skew

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9.2.5. LVDS with SSC

The LVDS receiver can support spread spectrum clock **(SSC)**. Limitation is listed as below.

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Modulation Frequency	SSC_{MF}	LVDS clock frequency center at 110MHz	-	-	200	KHz
		LVDS clock frequency center at 80MHz	-	-	200	KHz
		LVDS clock frequency center at 60MHz	-	-	150	KHz
		LVDS clock frequency center at 40MHz	-	-	100	KHz
		LVDS clock frequency center at 20MHz	-	-	100	KHz
		LVDS clock frequency center at 15MHz	-	-	100	KHz
Modulation Rate	SSC_{MR}	LVDS clock frequency + SSCMR in the range of 15MHZ~105Mhz	-	-	±3	%

Table 9.3: SSC limitation of LVDS interface

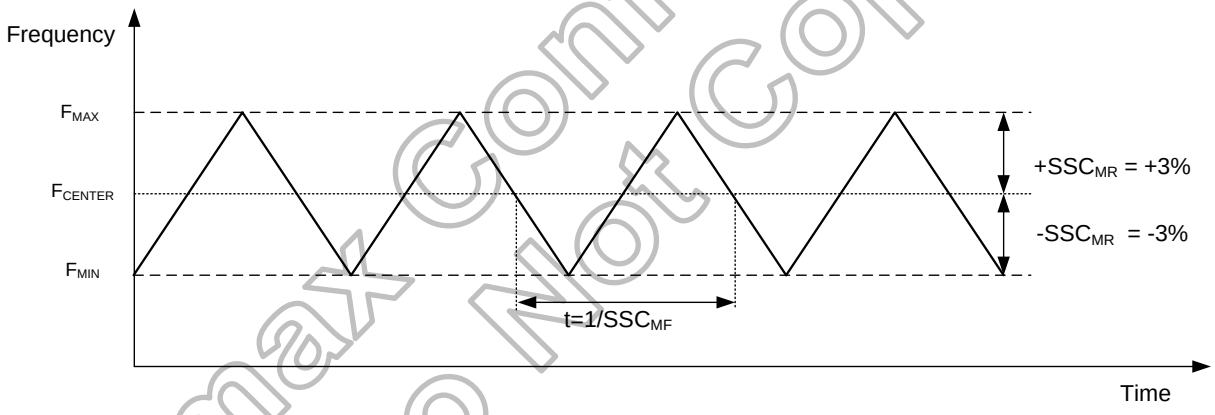

Figure 9.6: SSC figure

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9.2.6. TTL mode AC electrical characteristics

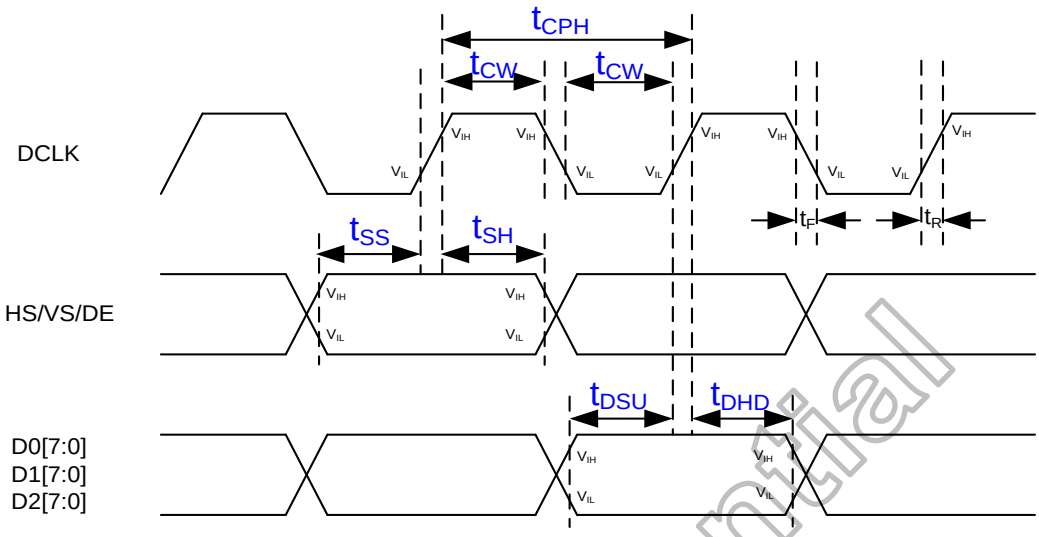

Figure 9.7: Input signal timing

Input data/sync. parameters
(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40℃ to +105℃)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK period	t_{CPH}	16.67	-	-	ns
DCLK clock high/low width	t_{CW}	6	-	-	ns
Data setup time	t_{DSU}	5	-	-	ns
Data hold time	t_{DHD}	5	-	-	ns
HS/VS/DE setup time	t_{SS}	5	-	-	ns
HS/VS/DE hold time	t_{SH}	5	-	-	ns
Input signal rising time	t_R	-	-	10	ns
Input signal falling time	t_F	-	-	10	ns

Table 9.4: Input data/sync. parameters

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9.2.7. Reset timing

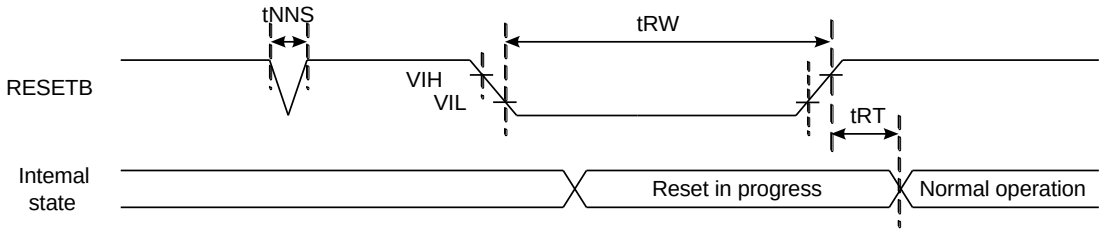

Figure 9.8: Reset timing

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40℃ to +105℃)

Signal	Parameter	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
RESETB	Reset pulse width	tRW	10	-	-	μs
	Reset complete time	tRT	-	-	5	μs
	Negative spike noise width	tNNS	-	-	100	ns

Table 9.5: Reset timing parameter

9.2.8. SPI timing

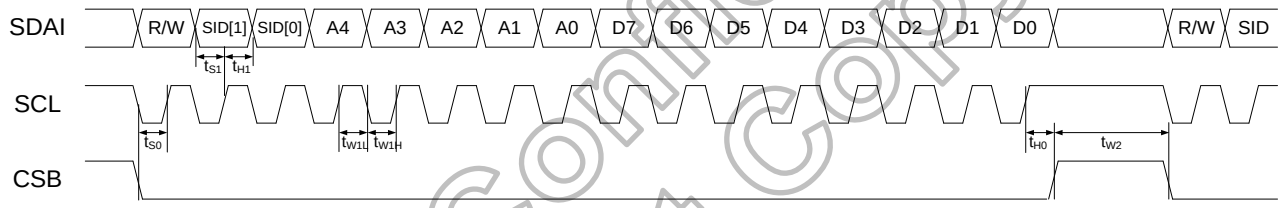

Figure 9.9: SPI signal timing

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40℃ to +105℃)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
SDAI Setup Time	t_{S0}	CSB to SCL	60	-	-	ns
	t_{S1}	SDAI to SCL	60	-	-	ns
SDAI Hold Time	t_{H0}	CSB to SCL	60	-	-	ns
	t_{H1}	SDAI to SCL	60	-	-	ns
Pulse Width	t_{W1L}	SCL pulse width	100	-	-	ns
	t_{W1H}	SCL pulse width	100	-	-	ns
	t_{W2}	CSB pulse width	1	-	-	μs
Clock duty	-	-	40	50	60	%

Table 9.6: SPI timing parameter

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9.2.9. I2C timing

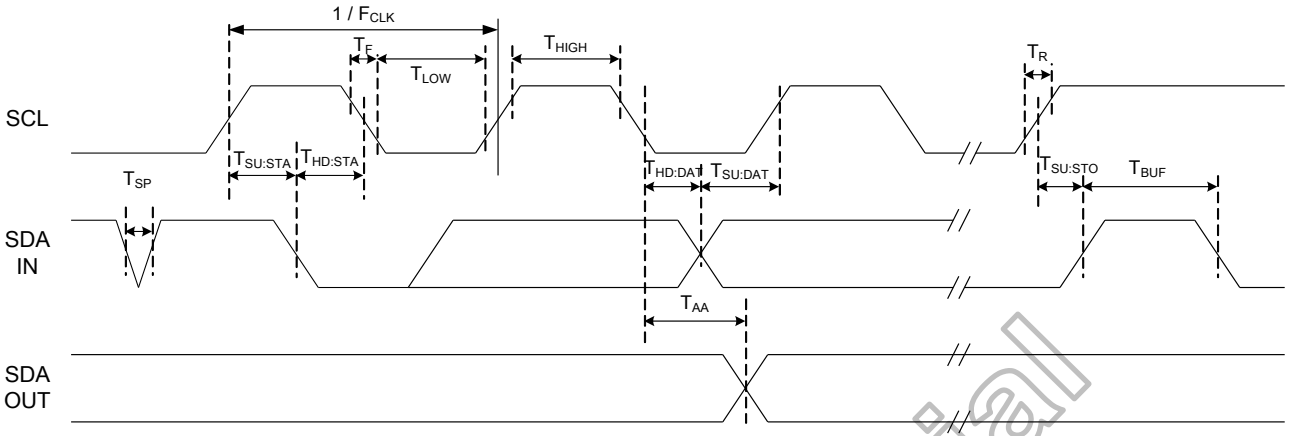

Figure 9.10: I2C signal timing

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40℃ to +105℃)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock frequency	F_{CLK}	-	-	-	400	KHz
Clock high time	T_{HIGH}	-	600	-	-	ns
Clock low time	T_{LOW}	-	1300	-	-	ns
SDA and SCL rise time	T_R	-	-	-	300	ns
SDA and SCL fall time	T_F	-	-	-	300	ns
Start condition hold time	$T_{HD:STA}$	-	600	-	-	ns
Start condition setup time	$T_{SU:STA}$	-	600	-	-	ns
Data input hold time	$T_{HD:DAT}$	-	0	-	-	ns
Data input setup time	$T_{SU:DAT}$	-	100	-	-	ns
Stop condition setup time	$T_{SU:STO}$	-	600	-	-	ns
Output valid from clock	T_{AA}	-	-	-	900	ns
Bus free-time	T_{BUF}	Time the bus must be free before a new transmission can start	1300	-	-	ns
Input filter spike suppression	T_{SP}	SDA and SCL pins	-	-	10	ns

Table 9.7: I2C timing parameter

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10. Pad Information

10.1. Chip information

Parameter	Size		Unit
	X	Y	
Chip size	28500	1150	μm
Chip size (including scribe line)	28580	1220	

Table 10.1: Chip information

10.2. Bump dimension

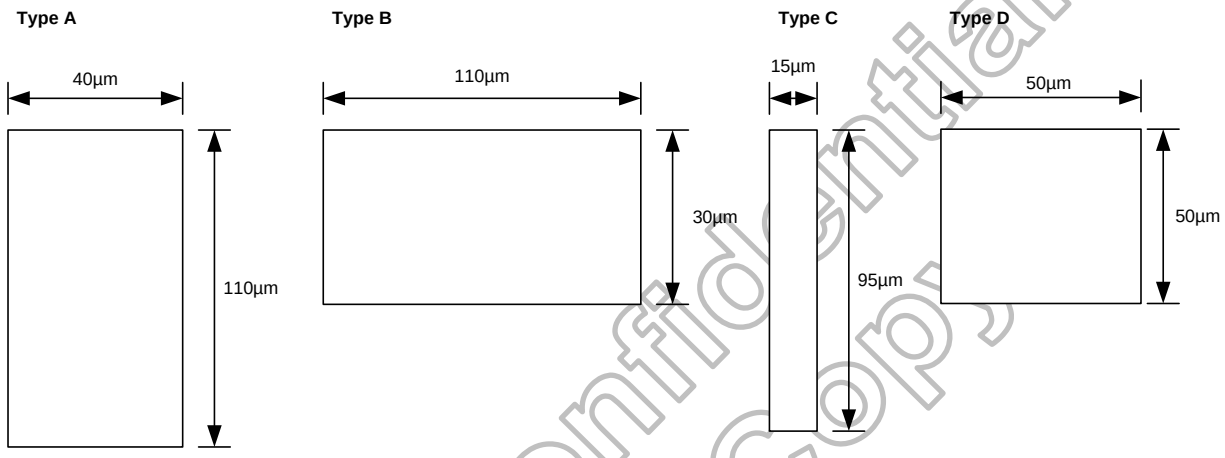

Figure 10.1: Bump dimension

10.3. Bump information

Bump Height: 12±3.0 μm
Bump Height Co-planarity within Die: < 2 μm
Hardness: 90±20 Hv
Shear Stress: > 4.5 g/mil^2

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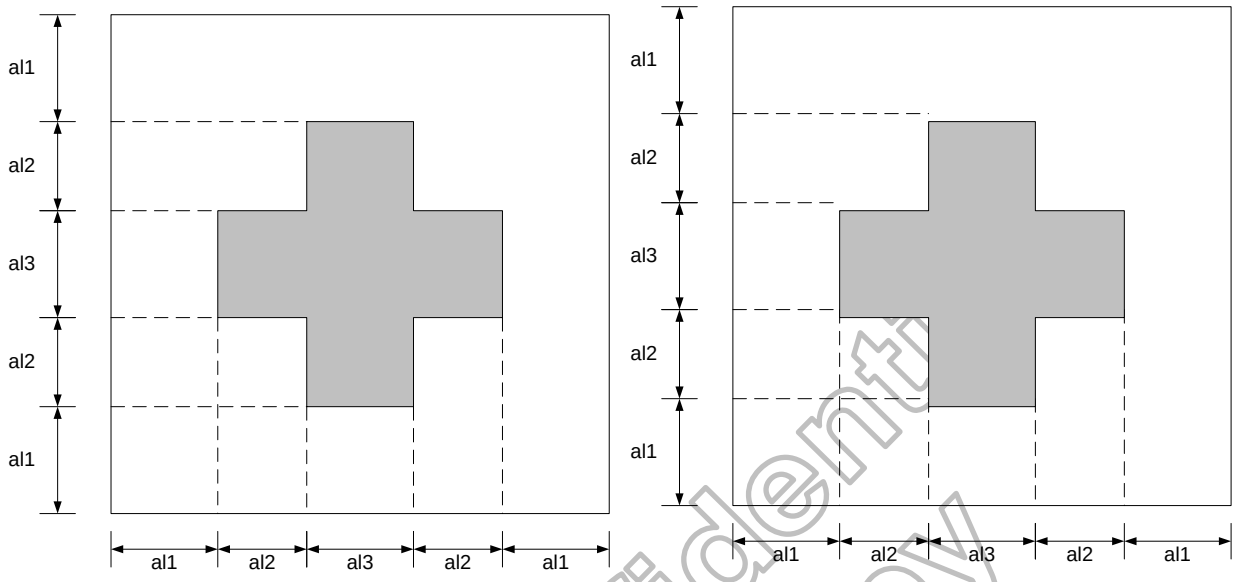
10.4. Alignment mark

Two Alignment marks are center located at (-14167, -492) and (14167, -492).
The cross pattern is top metal layer.



Symbol	Dimension (μm)
al1	20
al2	33
al3	34

Table 10.2: Alignment mark dimension

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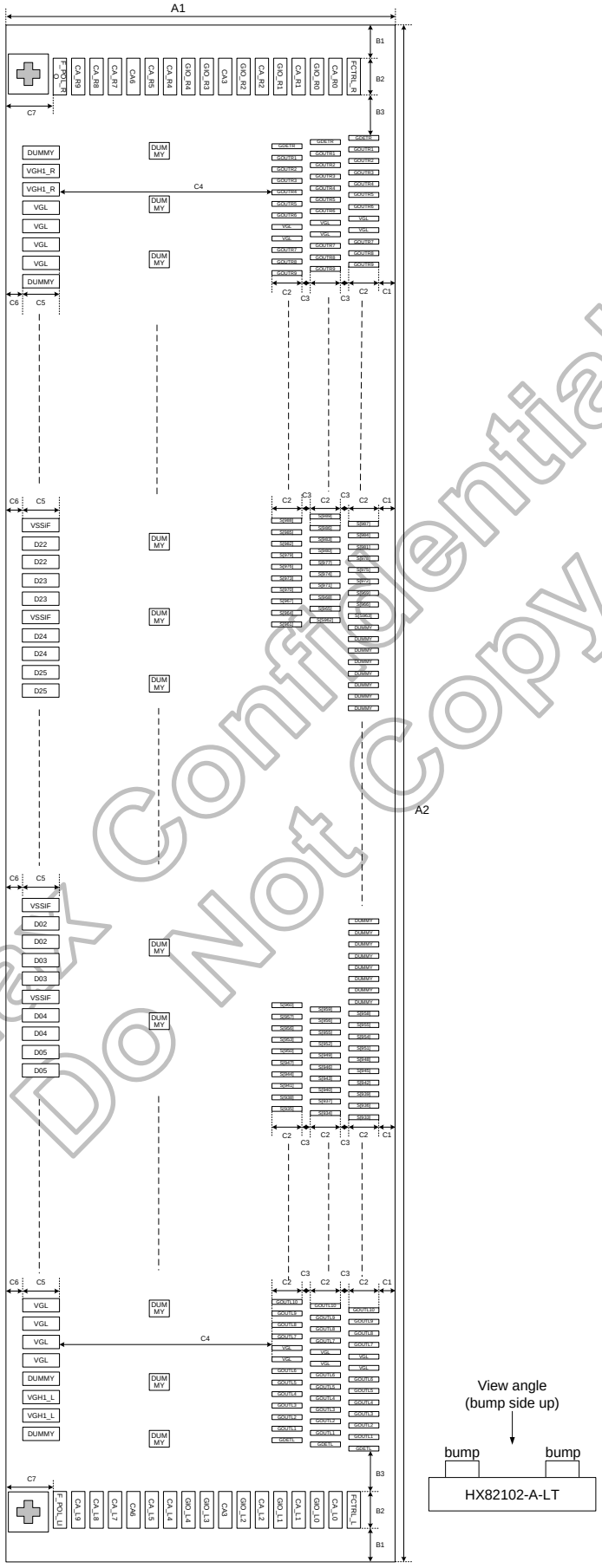
10.5. Chip outline



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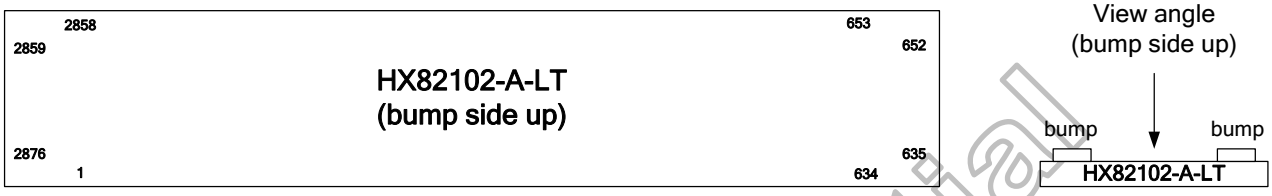
Symbol	Dimension (μm)
a1	1150
b1	50
b2	110
b3	171.3
c1	20
c2	95

Symbol	Dimension (μm)
c3	25
c4	635
c5	110
c6	50
c7	165

Table 10.3: Chip outline dimension



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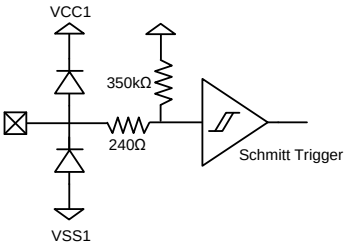
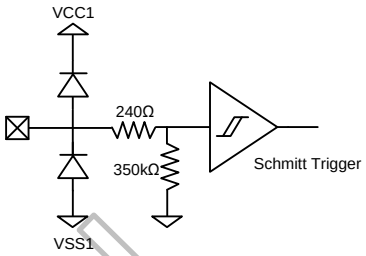
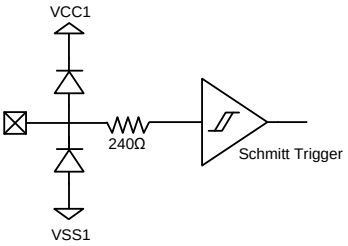
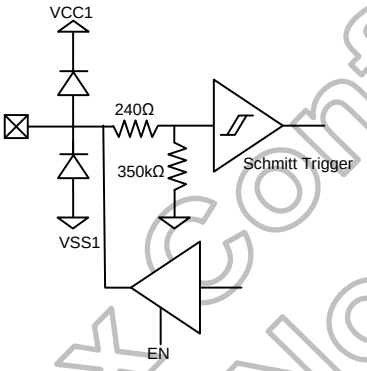
10.6. I/O structure

Signal	Input equivalent circuit	Signal	Input equivalent circuit
RESETB, RESETB_SLP, STBYB, FCS, SIDEN, MODE, NB, RL, TB, INV[1:0], SPI_CSB		DE, GSQ, ATREN, EXT_PWR2, EXT_PWR1, EEPEN, TR[1:0], GDSEL, GPOS[1:0], BISTEN, SPI_SCL, SPI_SDAI, I2C_SCL, I2C_SPI_SEL, ESDAI, F_POL_LI, ZZS[1:0], PTS[2:0], CA_L[2:0], CA_L[6:4], TS_H, TS_L, FMT, LANE_SW, LANE_PN	
SID[1:0], RS[3:0]		-	-
I2C_SDA, GIO_L[4:0], GIO_R[4:0], ECS, ESCL, FCTRL_L, FCTRL_R		-	-

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10.7. Pad coordinates

No.	Name	X	Y	Bump size (μm)
1	DUMMY	-13802	-470	40x110
2	VGH1_R	-13747	-470	40x110
3	VGH1_R	-13692	-470	40x110
4	DUMMY	-13637	-470	40x110
5	DUMMY	-13600	-101.25	50x50
6	VGL	-13582	-470	40x110
7	VGL	-13527	-470	40x110
8	VGL	-13472	-470	40x110
9	VGL	-13417	-470	40x110
10	DUMMY	-13400	-101.25	50x50
11	DUMMY	-13362	-470	40x110
12	VGH2	-13307	-470	40x110
13	VGH2	-13252	-470	40x110
14	DUMMY	-13200	-101.25	50x50
15	VGH2	-13197	-470	40x110
16	VGH2	-13142	-470	40x110
17	DUMMY	-13087	-470	40x110
18	VCOM_R	-13032	-470	40x110
19	DUMMY	-13000	-101.25	50x50
20	VCOM_R	-12977	-470	40x110
21	VCOM_R	-12922	-470	40x110
22	VCOM_R	-12867	-470	40x110
23	VSS1	-12812	-470	40x110
24	DUMMY	-12800	-101.25	50x50
25	VSS1	-12757	-470	40x110
26	VSS1	-12702	-470	40x110
27	VSS1	-12647	-470	40x110
28	DUMMY	-12600	-101.25	50x50
29	THROUGH_1	-12592	-470	40x110
30	THROUGH_1	-12537	-470	40x110
31	VDD_OTP	-12482	-470	40x110
32	VDD_OTP	-12427	-470	40x110
33	VDD_OTP	-12372	-470	40x110
34	VDD_OTP	-12317	-470	40x110
35	VDD_OTP	-12262	-470	40x110
36	VREGN	-12207	-470	40x110
37	VREGN	-12152	-470	40x110
38	VREGN	-12097	-470	40x110
39	VREGN	-12042	-470	40x110
40	CLP1	-11987	-470	40x110
41	CLP1	-11932	-470	40x110
42	DUMMY	-11900	-101.25	50x50
43	CLP1	-11877	-470	40x110
44	CLP1	-11822	-470	40x110
45	CLN1	-11767	-470	40x110
46	CLN1	-11712	-470	40x110
47	DUMMY	-11700	-101.25	50x50
48	CLN1	-11657	-470	40x110
49	CLN1	-11602	-470	40x110
50	CLP2	-11547	-470	40x110

No.	Name	X	Y	Bump size (μm)
51	DUMMY	-11500	-101.25	50x50
52	CLP2	-11492	-470	40x110
53	CLP2	-11437	-470	40x110
54	CLP2	-11382	-470	40x110
55	CLN2	-11327	-470	40x110
56	DUMMY	-11300	-101.25	50x50
57	CLN2	-11272	-470	40x110
58	CLN2	-11217	-470	40x110
59	CLN2	-11162	-470	40x110
60	VGL	-11107	-470	40x110
61	DUMMY	-11100	-101.25	50x50
62	VGL	-11052	-470	40x110
63	VGL	-10997	-470	40x110
64	VGL	-10942	-470	40x110
65	DUMMY	-10900	-101.25	50x50
66	VGL	-10887	-470	40x110
67	VGL	-10832	-470	40x110
68	DUMMY	-10777	-470	40x110
69	VGH1O	-10722	-470	40x110
70	DUMMY	-10700	-101.25	50x50
71	VGH2O	-10667	-470	40x110
72	DUMMY	-10612	-470	40x110
73	VGH1	-10557	-470	40x110
74	VGH1	-10502	-470	40x110
75	DUMMY	-10500	-101.25	50x50
76	DUMMY	-10447	-470	40x110
77	VGH2	-10392	-470	40x110
78	VGH2	-10337	-470	40x110
79	DUMMY	-10300	-101.25	50x50
80	VGH2	-10282	-470	40x110
81	VGH2	-10227	-470	40x110
82	VGH2	-10172	-470	40x110
83	DUMMY	-10117	-470	40x110
84	DUMMY	-10100	-101.25	50x50
85	CHP3	-10062	-470	40x110
86	CHP3	-10007	-470	40x110
87	CHP3	-9952	-470	40x110
88	DUMMY	-9900	-101.25	50x50
89	CHP3	-9897	-470	40x110
90	CHN3	-9842	-470	40x110
91	CHN3	-9787	-470	40x110
92	CHN3	-9732	-470	40x110
93	DUMMY	-9700	-101.25	50x50
94	CHN3	-9677	-470	40x110
95	CHP2	-9622	-470	40x110
96	CHP2	-9567	-470	40x110
97	CHP2	-9512	-470	40x110
98	DUMMY	-9500	-101.25	50x50
99	CHP2	-9457	-470	40x110
100	CHN2	-9402	-470	40x110

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No.	Name	X	Y	Bump size (μm)
101	CHN2	-9347	-470	40x110
102	DUMMY	-9300	-101.25	50x50
103	CHN2	-9292	-470	40x110
104	CHN2	-9237	-470	40x110
105	CHP1	-9182	-470	40x110
106	CHP1	-9127	-470	40x110
107	DUMMY	-9100	-101.25	50x50
108	CHP1	-9072	-470	40x110
109	CHP1	-9017	-470	40x110
110	CHN1	-8962	-470	40x110
111	CHN1	-8907	-470	40x110
112	DUMMY	-8900	-101.25	50x50
113	CHN1	-8852	-470	40x110
114	CHN1	-8797	-470	40x110
115	VREGP	-8742	-470	40x110
116	DUMMY	-8700	-101.25	50x50
117	VREGP	-8687	-470	40x110
118	VREGP	-8632	-470	40x110
119	VREGP	-8577	-470	40x110
120	VSS1P	-8522	-470	40x110
121	DUMMY	-8500	-101.25	50x50
122	VSS1P	-8467	-470	40x110
123	VSS1P	-8412	-470	40x110
124	DUMMY	-8357	-470	40x110
125	VCC1P	-8302	-470	40x110
126	DUMMY	-8300	-101.25	50x50
127	VCC1P	-8247	-470	40x110
128	VCC1P	-8192	-470	40x110
129	VSP	-8137	-470	40x110
130	DUMMY	-8100	-101.25	50x50
131	VSP	-8082	-470	40x110
132	VSP	-8027	-470	40x110
133	VSP	-7972	-470	40x110
134	VSP	-7917	-470	40x110
135	DUMMY	-7900	-101.25	50x50
136	VSP	-7862	-470	40x110
137	VSP	-7807	-470	40x110
138	VSDP	-7752	-470	40x110
139	DUMMY	-7700	-101.25	50x50
140	VSDP	-7697	-470	40x110
141	VSDP	-7642	-470	40x110
142	VSDP	-7587	-470	40x110
143	VSDP	-7532	-470	40x110
144	DUMMY	-7500	-101.25	50x50
145	VSDP	-7477	-470	40x110
146	VSSA	-7422	-470	40x110
147	VSSA	-7367	-470	40x110
148	VSSA	-7312	-470	40x110
149	DUMMY	-7300	-101.25	50x50
150	VSSA	-7257	-470	40x110

No.	Name	X	Y	Bump size (μm)
151	VSSA	-7202	-470	40x110
152	VSSA	-7147	-470	40x110
153	DUMMY	-7100	-101.25	50x50
154	VSSA	-7092	-470	40x110
155	VSSA	-7037	-470	40x110
156	VSSA	-6982	-470	40x110
157	VSDN	-6927	-470	40x110
158	DUMMY	-6900	-101.25	50x50
159	VSDN	-6872	-470	40x110
160	VSDN	-6817	-470	40x110
161	VSDN	-6762	-470	40x110
162	VSDN	-6707	-470	40x110
163	DUMMY	-6700	-101.25	50x50
164	VSDN	-6652	-470	40x110
165	VSN	-6597	-470	40x110
166	VSN	-6542	-470	40x110
167	DUMMY	-6500	-101.25	50x50
168	VSN	-6487	-470	40x110
169	VSN	-6432	-470	40x110
170	VSN	-6377	-470	40x110
171	VSN	-6322	-470	40x110
172	DUMMY	-6300	-101.25	50x50
173	VSN	-6267	-470	40x110
174	DRVN	-6212	-470	40x110
175	DRVN	-6157	-470	40x110
176	DRVN	-6102	-470	40x110
177	DUMMY	-6100	-101.25	50x50
178	DRVN	-6047	-470	40x110
179	VMONN	-5992	-470	40x110
180	VSS1P	-5937	-470	40x110
181	DUMMY	-5900	-101.25	50x50
182	VSS1P	-5882	-470	40x110
183	VSS1P	-5827	-470	40x110
184	VSS1P	-5772	-470	40x110
185	VSS1P	-5717	-470	40x110
186	DUMMY	-5700	-101.25	50x50
187	VCC1P	-5662	-470	40x110
188	VCC1P	-5607	-470	40x110
189	VCC1P	-5552	-470	40x110
190	DUMMY	-5500	-101.25	50x50
191	VCC1P	-5497	-470	40x110
192	VCC1P	-5442	-470	40x110
193	VMONP	-5387	-470	40x110
194	DRVP	-5332	-470	40x110
195	DUMMY	-5300	-101.25	50x50
196	DRVP	-5277	-470	40x110
197	DRVP	-5222	-470	40x110
198	DRVP	-5167	-470	40x110
199	VCL	-5112	-470	40x110
200	DUMMY	-5100	-101.25	50x50

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No.	Name	X	Y	Bump size (μm)
201	VCL	-5057	-470	40x110
202	VCL	-5002	-470	40x110
203	VCL	-4947	-470	40x110
204	DUMMY	-4900	-101.25	50x50
205	VCL	-4892	-470	40x110
206	VCL	-4837	-470	40x110
207	SPI_SDAO	-4782	-470	40x110
208	SPI_SDAO	-4727	-470	40x110
209	DUMMY	-4700	-101.25	50x50
210	SPI_SDAI	-4672	-470	40x110
211	SPI_SCL	-4617	-470	40x110
212	SPI_CSB	-4562	-470	40x110
213	DUMMY	-4507	-470	40x110
214	DUMMY	-4500	-101.25	50x50
215	DUMMY	-4452	-470	40x110
216	DUMMY	-4397	-470	40x110
217	I2C_SDA	-4342	-470	40x110
218	DUMMY	-4300	-101.25	50x50
219	I2C_SDA	-4287	-470	40x110
220	I2C_SDA	-4232	-470	40x110
221	I2C_SCL	-4177	-470	40x110
222	DUMMY	-4122	-470	40x110
223	DUMMY	-4100	-101.25	50x50
224	I2C_SPI_SEL	-4067	-470	40x110
225	EEPEN	-4012	-470	40x110
226	DUMMY	-3957	-470	40x110
227	ECS	-3902	-470	40x110
228	DUMMY	-3900	-101.25	50x50
229	ECS	-3847	-470	40x110
230	ECS	-3792	-470	40x110
231	ESCL	-3737	-470	40x110
232	DUMMY	-3700	-101.25	50x50
233	ESCL	-3682	-470	40x110
234	ESCL	-3627	-470	40x110
235	ESDAO	-3572	-470	40x110
236	ESDAO	-3517	-470	40x110
237	DUMMY	-3500	-101.25	50x50
238	ESDAI	-3462	-470	40x110
239	VCC1	-3407	-470	40x110
240	VCC1	-3352	-470	40x110
241	DUMMY	-3300	-101.25	50x50
242	VCC1	-3297	-470	40x110
243	VCC1	-3242	-470	40x110
244	VCC1	-3187	-470	40x110
245	VCC1	-3132	-470	40x110
246	DUMMY	-3100	-101.25	50x50
247	VSS1	-3077	-470	40x110
248	VSS1	-3022	-470	40x110
249	VSS1	-2967	-470	40x110
250	VSS1	-2912	-470	40x110

No.	Name	X	Y	Bump size (μm)
251	DUMMY	-2900	-101.25	50x50
252	VSS1	-2857	-470	40x110
253	VSS1	-2802	-470	40x110
254	VDDD	-2747	-470	40x110
255	DUMMY	-2700	-101.25	50x50
256	VDDD	-2692	-470	40x110
257	VDDD	-2637	-470	40x110
258	VDDD	-2582	-470	40x110
259	VDDD	-2527	-470	40x110
260	DUMMY	-2500	-101.25	50x50
261	VCCIF	-2472	-470	40x110
262	VCCIF	-2417	-470	40x110
263	VCCIF	-2362	-470	40x110
264	VCCIF	-2307	-470	40x110
265	DUMMY	-2300	-101.25	50x50
266	VDDIF	-2252	-470	40x110
267	VDDIF	-2197	-470	40x110
268	VDDIF	-2142	-470	40x110
269	DUMMY	-2100	-101.25	50x50
270	VDDIF	-2087	-470	40x110
271	VSSIF	-2032	-470	40x110
272	VSSIF	-1977	-470	40x110
273	VSSIF	-1922	-470	40x110
274	DUMMY	-1900	-101.25	50x50
275	VSSIF	-1867	-470	40x110
276	D20	-1812	-470	40x110
277	D20	-1757	-470	40x110
278	D21	-1702	-470	40x110
279	DUMMY	-1700	-101.25	50x50
280	D21	-1647	-470	40x110
281	VSSIF	-1592	-470	40x110
282	D22	-1537	-470	40x110
283	DUMMY	-1500	-101.25	50x50
284	D22	-1482	-470	40x110
285	D23	-1427	-470	40x110
286	D23	-1372	-470	40x110
287	VSSIF	-1317	-470	40x110
288	DUMMY	-1300	-101.25	50x50
289	D24	-1262	-470	40x110
290	D24	-1207	-470	40x110
291	D25	-1152	-470	40x110
292	DUMMY	-1100	-101.25	50x50
293	D25	-1097	-470	40x110
294	VSSIF	-1042	-470	40x110
295	D26	-987	-470	40x110
296	D26	-932	-470	40x110
297	DUMMY	-900	-101.25	50x50
298	D27	-877	-470	40x110
299	D27	-822	-470	40x110
300	VSSIF	-767	-470	40x110

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No.	Name	X	Y	Bump size (μm)
301	D10	-712	-470	40x110
302	DUMMY	-700	-101.25	50x50
303	D10	-657	-470	40x110
304	D11	-602	-470	40x110
305	D11	-547	-470	40x110
306	DUMMY	-500	-101.25	50x50
307	VSSIF	-492	-470	40x110
308	D12	-437	-470	40x110
309	D12	-382	-470	40x110
310	D13	-327	-470	40x110
311	DUMMY	-300	-101.25	50x50
312	D13	-272	-470	40x110
313	VSSIF	-217	-470	40x110
314	D14	-162	-470	40x110
315	D14	-107	-470	40x110
316	DUMMY	-100	-101.25	50x50
317	D15	-52	-470	40x110
318	D15	3	-470	40x110
319	VSSIF	58	-470	40x110
320	DUMMY	100	-101.25	50x50
321	VSSIF	113	-470	40x110
322	VSSIF	168	-470	40x110
323	VSSIF	223	-470	40x110
324	VSSIF	278	-470	40x110
325	DUMMY	300	-101.25	50x50
326	VSSIF	333	-470	40x110
327	VSSIF	388	-470	40x110
328	D16	443	-470	40x110
329	D16	498	-470	40x110
330	DUMMY	500	-101.25	50x50
331	D17	553	-470	40x110
332	D17	608	-470	40x110
333	VSSIF	663	-470	40x110
334	DUMMY	700	-101.25	50x50
335	D00	718	-470	40x110
336	D00	773	-470	40x110
337	D01	828	-470	40x110
338	D01	883	-470	40x110
339	DUMMY	900	-101.25	50x50
340	VSSIF	938	-470	40x110
341	D02	993	-470	40x110
342	D02	1048	-470	40x110
343	DUMMY	1100	-101.25	50x50
344	D03	1103	-470	40x110
345	D03	1158	-470	40x110
346	VSSIF	1213	-470	40x110
347	D04	1268	-470	40x110
348	DUMMY	1300	-101.25	50x50
349	D04	1323	-470	40x110
350	D05	1378	-470	40x110
351	D05	1433	-470	40x110
352	VSSIF	1488	-470	40x110
353	DUMMY	1500	-101.25	50x50
354	D06	1543	-470	40x110
355	D06	1598	-470	40x110
356	D07	1653	-470	40x110
357	DUMMY	1700	-101.25	50x50
358	D07	1708	-470	40x110
359	VSSIF	1763	-470	40x110
360	DCLK	1818	-470	40x110
361	DCLK	1873	-470	40x110
362	DUMMY	1900	-101.25	50x50
363	HS	1928	-470	40x110
364	HS	1983	-470	40x110
365	VS	2038	-470	40x110
366	VS	2093	-470	40x110
367	DUMMY	2100	-101.25	50x50
368	DE	2148	-470	40x110
369	DE	2203	-470	40x110
370	VSSIF	2258	-470	40x110
371	DUMMY	2300	-101.25	50x50
372	VSSIF	2313	-470	40x110
373	VSSIF	2368	-470	40x110
374	VSSIF	2423	-470	40x110
375	VDDIF	2478	-470	40x110
376	DUMMY	2500	-101.25	50x50
377	VDDIF	2533	-470	40x110
378	VDDIF	2588	-470	40x110
379	VDDIF	2643	-470	40x110
380	VCCIF	2698	-470	40x110
381	DUMMY	2700	-101.25	50x50
382	VCCIF	2753	-470	40x110
383	VCCIF	2808	-470	40x110
384	VCCIF	2863	-470	40x110
385	DUMMY	2900	-101.25	50x50
386	VDDD	2918	-470	40x110
387	VDDD	2973	-470	40x110
388	VDDD	3028	-470	40x110
389	VDDD	3083	-470	40x110
390	DUMMY	3100	-101.25	50x50
391	VDDD	3138	-470	40x110
392	VSS1	3193	-470	40x110
393	VSS1	3248	-470	40x110
394	DUMMY	3300	-101.25	50x50
395	VSS1	3303	-470	40x110
396	VSS1	3358	-470	40x110
397	DUMMY	3413	-470	40x110
398	VGMPHI	3468	-470	40x110
399	DUMMY	3500	-101.25	50x50
400	VGMPHI	3523	-470	40x110

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No.	Name	X	Y	Bump size (μm)
401	VGMPHI	3578	-470	40x110
402	VGMPHI	3633	-470	40x110
403	VGMPLI	3688	-470	40x110
404	DUMMY	3700	-101.25	50x50
405	VGMPLI	3743	-470	40x110
406	VGMPLI	3798	-470	40x110
407	VGMPLI	3853	-470	40x110
408	DUMMY	3900	-101.25	50x50
409	VGMNHI	3908	-470	40x110
410	VGMNHI	3963	-470	40x110
411	VGMNHI	4018	-470	40x110
412	VGMNHI	4073	-470	40x110
413	DUMMY	4100	-101.25	50x50
414	VGMNLI	4128	-470	40x110
415	VGMNLI	4183	-470	40x110
416	VGMNLI	4238	-470	40x110
417	VGMNLI	4293	-470	40x110
418	DUMMY	4300	-101.25	50x50
419	DUMMY	4348	-470	40x110
420	VGMPHO	4403	-470	40x110
421	VGMPHO	4458	-470	40x110
422	DUMMY	4500	-101.25	50x50
423	VGMPHO	4513	-470	40x110
424	VGMPHO	4568	-470	40x110
425	VGMPLO	4623	-470	40x110
426	VGMPLO	4678	-470	40x110
427	DUMMY	4700	-101.25	50x50
428	VGMPLO	4733	-470	40x110
429	VGMPLO	4788	-470	40x110
430	VGMNHO	4843	-470	40x110
431	VGMNHO	4898	-470	40x110
432	DUMMY	4900	-101.25	50x50
433	VGMNHO	4953	-470	40x110
434	VGMNHO	5008	-470	40x110
435	VGMNLO	5063	-470	40x110
436	DUMMY	5100	-101.25	50x50
437	VGMNLO	5118	-470	40x110
438	VGMNLO	5173	-470	40x110
439	VGMNLO	5228	-470	40x110
440	DUMMY	5283	-470	40x110
441	DUMMY	5300	-101.25	50x50
442	DUMMY	5338	-470	40x110
443	DUMMY	5393	-470	40x110
444	EXT_CRC_EN	5448	-470	40x110
445	DUMMY	5500	-101.25	50x50
446	TESTI1	5503	-470	40x110
447	TESTI2	5558	-470	40x110
448	TEST7	5613	-470	40x110
449	TEST7	5668	-470	40x110
450	DUMMY	5700	-101.25	50x50

No.	Name	X	Y	Bump size (μm)
451	TEST6	5723	-470	40x110
452	TEST6	5778	-470	40x110
453	TEST5	5833	-470	40x110
454	TEST5	5888	-470	40x110
455	DUMMY	5900	-101.25	50x50
456	VSS1	5943	-470	40x110
457	VSS1	5998	-470	40x110
458	VSS1	6053	-470	40x110
459	DUMMY	6100	-101.25	50x50
460	TEST4	6108	-470	40x110
461	TEST4	6163	-470	40x110
462	TEST3	6218	-470	40x110
463	TEST3	6273	-470	40x110
464	DUMMY	6300	-101.25	50x50
465	TP_SYNC2	6328	-470	40x110
466	TP_SYNC2	6383	-470	40x110
467	TP_SYNC1	6438	-470	40x110
468	TP_SYNC1	6493	-470	40x110
469	DUMMY	6500	-101.25	50x50
470	VSS1	6548	-470	40x110
471	VSS1	6603	-470	40x110
472	FAIL_DET	6658	-470	40x110
473	DUMMY	6700	-101.25	50x50
474	FAIL_DET	6713	-470	40x110
475	TS_H	6768	-470	40x110
476	TS_L	6823	-470	40x110
477	VCC1	6878	-470	40x110
478	DUMMY	6900	-101.25	50x50
479	VCC1	6933	-470	40x110
480	VCC1	6988	-470	40x110
481	VCC1	7043	-470	40x110
482	VSDN	7098	-470	40x110
483	DUMMY	7100	-101.25	50x50
484	VSDN	7153	-470	40x110
485	VSDN	7208	-470	40x110
486	VSDN	7263	-470	40x110
487	DUMMY	7300	-101.25	50x50
488	VSDN	7318	-470	40x110
489	VSDN	7373	-470	40x110
490	VSN	7428	-470	40x110
491	VSN	7483	-470	40x110
492	DUMMY	7500	-101.25	50x50
493	VSN	7538	-470	40x110
494	VSN	7593	-470	40x110
495	VSN	7648	-470	40x110
496	DUMMY	7700	-101.25	50x50
497	VSN	7703	-470	40x110
498	VSN	7758	-470	40x110
499	VSSA	7813	-470	40x110
500	VSSA	7868	-470	40x110

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No.	Name	X	Y	Bump size (μm)
501	DUMMY	7900	-101.25	50x50
502	VSSA	7923	-470	40x110
503	VSSA	7978	-470	40x110
504	VSSA	8033	-470	40x110
505	VSSA	8088	-470	40x110
506	DUMMY	8100	-101.25	50x50
507	VSSA	8143	-470	40x110
508	VSSA	8198	-470	40x110
509	VSDP	8253	-470	40x110
510	DUMMY	8300	-101.25	50x50
511	VSDP	8308	-470	40x110
512	VSDP	8363	-470	40x110
513	VSDP	8418	-470	40x110
514	VSDP	8473	-470	40x110
515	DUMMY	8500	-101.25	50x50
516	VSDP	8528	-470	40x110
517	VSP	8583	-470	40x110
518	VSP	8638	-470	40x110
519	VSP	8693	-470	40x110
520	DUMMY	8700	-101.25	50x50
521	VSP	8748	-470	40x110
522	VSP	8803	-470	40x110
523	VSP	8858	-470	40x110
524	DUMMY	8900	-101.25	50x50
525	VSP	8913	-470	40x110
526	VSS1	8968	-470	40x110
527	VSS1	9023	-470	40x110
528	VSS1	9078	-470	40x110
529	DUMMY	9100	-101.25	50x50
530	VCC2	9133	-470	40x110
531	VCC2	9188	-470	40x110
532	VCC2	9243	-470	40x110
533	VCC2	9298	-470	40x110
534	DUMMY	9300	-101.25	50x50
535	VCC2	9353	-470	40x110
536	VSS2	9408	-470	40x110
537	VSS2	9463	-470	40x110
538	DUMMY	9500	-101.25	50x50
539	VSS2	9518	-470	40x110
540	VSS2	9573	-470	40x110
541	VSS2	9628	-470	40x110
542	TO3	9683	-470	40x110
543	DUMMY	9700	-101.25	50x50
544	TO2	9738	-470	40x110
545	TO1	9793	-470	40x110
546	TO0	9848	-470	40x110
547	DUMMY	9900	-101.25	50x50
548	STBYB	9903	-470	40x110
549	RESETB	9958	-470	40x110
550	RESETB_SLP	10013	-470	40x110

No.	Name	X	Y	Bump size (μm)
551	TB	10068	-470	40x110
552	DUMMY	10100	-101.25	50x50
553	VSS1	10123	-470	40x110
554	VSS1	10178	-470	40x110
555	MODE	10233	-470	40x110
556	DINT	10288	-470	40x110
557	DUMMY	10300	-101.25	50x50
558	TR0	10343	-470	40x110
559	TR1	10398	-470	40x110
560	PTS0	10453	-470	40x110
561	DUMMY	10500	-101.25	50x50
562	PTS1	10508	-470	40x110
563	PTS2	10563	-470	40x110
564	ZZS0	10618	-470	40x110
565	ZZS1	10673	-470	40x110
566	DUMMY	10700	-101.25	50x50
567	EXT_PWR2	10728	-470	40x110
568	VCC1	10783	-470	40x110
569	VCC1	10838	-470	40x110
570	RL	10893	-470	40x110
571	DUMMY	10900	-101.25	50x50
572	INTLB	10948	-470	40x110
573	ATREN	11003	-470	40x110
574	GSQ	11058	-470	40x110
575	DUMMY	11100	-101.25	50x50
576	SIDEN	11113	-470	40x110
577	SID0	11168	-470	40x110
578	SID1	11223	-470	40x110
579	FCS	11278	-470	40x110
580	DUMMY	11300	-101.25	50x50
581	GDSEL	11333	-470	40x110
582	DUMMY	11388	-470	40x110
583	DUMMY	11443	-470	40x110
584	LANE_SW	11498	-470	40x110
585	DUMMY	11500	-101.25	50x50
586	LANE_PN	11553	-470	40x110
587	FMT	11608	-470	40x110
588	BISTEN	11663	-470	40x110
589	DUMMY	11700	-101.25	50x50
590	GPOS0	11718	-470	40x110
591	GPOS1	11773	-470	40x110
592	INV0	11828	-470	40x110
593	INV1	11883	-470	40x110
594	DUMMY	11900	-101.25	50x50
595	EXT_PWR1	11938	-470	40x110
596	VSS1	11993	-470	40x110
597	VSS1	12048	-470	40x110
598	VSS1	12103	-470	40x110
599	VSS1	12158	-470	40x110
600	VSS1	12213	-470	40x110

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No.	Name	X	Y	Bump size (μm)
601	RS0	12268	-470	40x110
602	RS1	12323	-470	40x110
603	RS2	12378	-470	40x110
604	RS3	12433	-470	40x110
605	VCOM	12488	-470	40x110
606	VCOM	12543	-470	40x110
607	VCOM	12598	-470	40x110
608	DUMMY	12600	-101.25	50x50
609	VCOM	12653	-470	40x110
610	THROUGH_2	12708	-470	40x110
611	THROUGH_2	12763	-470	40x110
612	DUMMY	12800	-101.25	50x50
613	VCOM_L	12818	-470	40x110
614	VCOM_L	12873	-470	40x110
615	VCOM_L	12928	-470	40x110
616	VCOM_L	12983	-470	40x110
617	DUMMY	13000	-101.25	50x50
618	DUMMY	13038	-470	40x110
619	VGH2	13093	-470	40x110
620	VGH2	13148	-470	40x110
621	DUMMY	13200	-101.25	50x50
622	VGH2	13203	-470	40x110
623	VGH2	13258	-470	40x110
624	DUMMY	13313	-470	40x110
625	VGL	13368	-470	40x110
626	DUMMY	13400	-101.25	50x50
627	VGL	13423	-470	40x110
628	VGL	13478	-470	40x110
629	VGL	13533	-470	40x110
630	DUMMY	13588	-470	40x110
631	DUMMY	13600	-101.25	50x50
632	VGH1_L	13643	-470	40x110
633	VGH1_L	13698	-470	40x110
634	DUMMY	13753	-470	40x110
635	F_POL_LI	14145	-395	110x30
636	CA_L[9]	14145	-340	110x30
637	CA_L[8]	14145	-285	110x30
638	CA_L[7]	14145	-230	110x30
639	CA6	14145	-175	110x30
640	CA_L[5]	14145	-120	110x30
641	DUMMY	13800	-101.25	50x50
642	CA_L[4]	14145	-65	110x30
643	GIO_L[4]	14145	-10	110x30
644	GIO_L[3]	14145	45	110x30
645	CA3	14145	100	110x30
646	GIO_L[2]	14145	155	110x30
647	CA_L[2]	14145	210	110x30
648	GIO_L[1]	14145	265	110x30
649	CA_L[1]	14145	320	110x30
650	GIO_L[0]	14145	375	110x30

No.	Name	X	Y	Bump size (μm)
651	CA_L[0]	14145	430	110x30
652	FCTRL_L	14145	485	110x30
653	GDETL	13914	507.5	15x95
654	GDETL	13902	387.5	15x95
655	GDETL	13890	267.5	15x95
656	GOUTL1	13878	507.5	15x95
657	GOUTL1	13866	387.5	15x95
658	GOUTL1	13854	267.5	15x95
659	GOUTL2	13842	507.5	15x95
660	GOUTL2	13830	387.5	15x95
661	GOUTL2	13818	267.5	15x95
662	GOUTL3	13806	507.5	15x95
663	GOUTL3	13794	387.5	15x95
664	GOUTL3	13782	267.5	15x95
665	GOUTL4	13770	507.5	15x95
666	GOUTL4	13758	387.5	15x95
667	GOUTL4	13746	267.5	15x95
668	GOUTL5	13734	507.5	15x95
669	GOUTL5	13722	387.5	15x95
670	GOUTL5	13710	267.5	15x95
671	GOUTL6	13698	507.5	15x95
672	GOUTL6	13686	387.5	15x95
673	GOUTL6	13674	267.5	15x95
674	VGL	13662	507.5	15x95
675	VGL	13650	387.5	15x95
676	VGL	13638	267.5	15x95
677	VGL	13626	507.5	15x95
678	VGL	13614	387.5	15x95
679	VGL	13602	267.5	15x95
680	GOUTL7	13590	507.5	15x95
681	GOUTL7	13578	387.5	15x95
682	GOUTL7	13566	267.5	15x95
683	GOUTL8	13554	507.5	15x95
684	GOUTL8	13542	387.5	15x95
685	GOUTL8	13530	267.5	15x95
686	GOUTL9	13518	507.5	15x95
687	GOUTL9	13506	387.5	15x95
688	GOUTL9	13494	267.5	15x95
689	GOUTL10	13482	507.5	15x95
690	GOUTL10	13470	387.5	15x95
691	GOUTL10	13458	267.5	15x95
692	GOUTL11	13446	507.5	15x95
693	GOUTL11	13434	387.5	15x95
694	GOUTL11	13422	267.5	15x95
695	GOUTL12	13410	507.5	15x95
696	GOUTL12	13398	387.5	15x95
697	GOUTL12	13386	267.5	15x95
698	GOUTL13	13374	507.5	15x95
699	GOUTL13	13362	387.5	15x95
700	GOUTL13	13350	267.5	15x95

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No.	Name	X	Y	Bump size (μm)
701	VGH2	13338	507.5	15x95
702	VGH2	13326	387.5	15x95
703	VGH2	13314	267.5	15x95
704	VGH2	13302	507.5	15x95
705	VGH2	13290	387.5	15x95
706	VGH2	13278	267.5	15x95
707	GOUTL14	13266	507.5	15x95
708	GOUTL14	13254	387.5	15x95
709	GOUTL14	13242	267.5	15x95
710	GOUTL15	13230	507.5	15x95
711	GOUTL15	13218	387.5	15x95
712	GOUTL15	13206	267.5	15x95
713	GOUTL16	13194	507.5	15x95
714	GOUTL16	13182	387.5	15x95
715	GOUTL16	13170	267.5	15x95
716	GOUTL17	13158	507.5	15x95
717	GOUTL17	13146	387.5	15x95
718	GOUTL17	13134	267.5	15x95
719	GOUTL18	13122	507.5	15x95
720	GOUTL18	13110	387.5	15x95
721	GOUTL18	13098	267.5	15x95
722	GOUTL19	13086	507.5	15x95
723	GOUTL19	13074	387.5	15x95
724	GOUTL19	13062	267.5	15x95
725	GOUTL20	13050	507.5	15x95
726	GOUTL20	13038	387.5	15x95
727	GOUTL20	13026	267.5	15x95
728	SWL1	13014	507.5	15x95
729	SWL1	13002	387.5	15x95
730	SWL1	12990	267.5	15x95
731	SWL1B	12978	507.5	15x95
732	SWL1B	12966	387.5	15x95
733	SWL1B	12954	267.5	15x95
734	SWL2	12942	507.5	15x95
735	SWL2	12930	387.5	15x95
736	SWL2	12918	267.5	15x95
737	SWL2B	12906	507.5	15x95
738	SWL2B	12894	387.5	15x95
739	SWL2B	12882	267.5	15x95
740	SWL3	12870	507.5	15x95
741	SWL3	12858	387.5	15x95
742	SWL3	12846	267.5	15x95
743	SWL3B	12834	507.5	15x95
744	SWL3B	12822	387.5	15x95
745	SWL3B	12810	267.5	15x95
746	DUMMY	12798	507.5	15x95
747	DUMMY	12786	387.5	15x95
748	DUMMY	12774	267.5	15x95
749	DUMMY	12762	507.5	15x95
750	DUMMY	12750	387.5	15x95

No.	Name	X	Y	Bump size (μm)
751	DUMMY	12738	267.5	15x95
752	VSSA	12726	507.5	15x95
753	VSSA	12714	387.5	15x95
754	VSSA	12702	267.5	15x95
755	VCOM_L	12690	507.5	15x95
756	VCOM_L	12678	387.5	15x95
757	VCOM_L	12666	267.5	15x95
758	VCOM_L	12654	507.5	15x95
759	VCOM_L	12642	387.5	15x95
760	VCOM_L	12630	267.5	15x95
761	VSSA	12618	507.5	15x95
762	VSSA	12606	387.5	15x95
763	VSSA	12594	267.5	15x95
764	DUMMY	12582	507.5	15x95
765	S_DUMMY	12570	387.5	15x95
766	SZ1	12558	267.5	15x95
767	S1	12546	507.5	15x95
768	S2	12534	387.5	15x95
769	S3	12522	267.5	15x95
770	S4	12510	507.5	15x95
771	S5	12498	387.5	15x95
772	S6	12486	267.5	15x95
773	S7	12474	507.5	15x95
774	S8	12462	387.5	15x95
775	S9	12450	267.5	15x95
776	S10	12438	507.5	15x95
777	S11	12426	387.5	15x95
778	S12	12414	267.5	15x95
779	S13	12402	507.5	15x95
780	S14	12390	387.5	15x95
781	S15	12378	267.5	15x95
782	S16	12366	507.5	15x95
783	S17	12354	387.5	15x95
784	S18	12342	267.5	15x95
785	S19	12330	507.5	15x95
786	S20	12318	387.5	15x95
787	S21	12306	267.5	15x95
788	S22	12294	507.5	15x95
789	S23	12282	387.5	15x95
790	S24	12270	267.5	15x95
791	S25	12258	507.5	15x95
792	S26	12246	387.5	15x95
793	S27	12234	267.5	15x95
794	S28	12222	507.5	15x95
795	S29	12210	387.5	15x95
796	S30	12198	267.5	15x95
797	S31	12186	507.5	15x95
798	S32	12174	387.5	15x95
799	S33	12162	267.5	15x95
800	S34	12150	507.5	15x95

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No.	Name	X	Y	Bump size (μm)
801	S35	12138	387.5	15x95
802	S36	12126	267.5	15x95
803	S37	12114	507.5	15x95
804	S38	12102	387.5	15x95
805	S39	12090	267.5	15x95
806	S40	12078	507.5	15x95
807	S41	12066	387.5	15x95
808	S42	12054	267.5	15x95
809	S43	12042	507.5	15x95
810	S44	12030	387.5	15x95
811	S45	12018	267.5	15x95
812	S46	12006	507.5	15x95
813	S47	11994	387.5	15x95
814	S48	11982	267.5	15x95
815	S49	11970	507.5	15x95
816	S50	11958	387.5	15x95
817	S51	11946	267.5	15x95
818	S52	11934	507.5	15x95
819	S53	11922	387.5	15x95
820	S54	11910	267.5	15x95
821	S55	11898	507.5	15x95
822	S56	11886	387.5	15x95
823	S57	11874	267.5	15x95
824	S58	11862	507.5	15x95
825	S59	11850	387.5	15x95
826	S60	11838	267.5	15x95
827	S61	11826	507.5	15x95
828	S62	11814	387.5	15x95
829	S63	11802	267.5	15x95
830	S64	11790	507.5	15x95
831	S65	11778	387.5	15x95
832	S66	11766	267.5	15x95
833	S67	11754	507.5	15x95
834	S68	11742	387.5	15x95
835	S69	11730	267.5	15x95
836	S70	11718	507.5	15x95
837	S71	11706	387.5	15x95
838	S72	11694	267.5	15x95
839	S73	11682	507.5	15x95
840	S74	11670	387.5	15x95
841	S75	11658	267.5	15x95
842	S76	11646	507.5	15x95
843	S77	11634	387.5	15x95
844	S78	11622	267.5	15x95
845	S79	11610	507.5	15x95
846	S80	11598	387.5	15x95
847	S81	11586	267.5	15x95
848	S82	11574	507.5	15x95
849	S83	11562	387.5	15x95
850	S84	11550	267.5	15x95

No.	Name	X	Y	Bump size (μm)
851	S85	11538	507.5	15x95
852	S86	11526	387.5	15x95
853	S87	11514	267.5	15x95
854	S88	11502	507.5	15x95
855	S89	11490	387.5	15x95
856	S90	11478	267.5	15x95
857	S91	11466	507.5	15x95
858	S92	11454	387.5	15x95
859	S93	11442	267.5	15x95
860	S94	11430	507.5	15x95
861	S95	11418	387.5	15x95
862	S96	11406	267.5	15x95
863	S97	11394	507.5	15x95
864	S98	11382	387.5	15x95
865	S99	11370	267.5	15x95
866	S100	11358	507.5	15x95
867	S101	11346	387.5	15x95
868	S102	11334	267.5	15x95
869	S103	11322	507.5	15x95
870	S104	11310	387.5	15x95
871	S105	11298	267.5	15x95
872	S106	11286	507.5	15x95
873	S107	11274	387.5	15x95
874	S108	11262	267.5	15x95
875	S109	11250	507.5	15x95
876	S110	11238	387.5	15x95
877	S111	11226	267.5	15x95
878	S112	11214	507.5	15x95
879	S113	11202	387.5	15x95
880	S114	11190	267.5	15x95
881	S115	11178	507.5	15x95
882	S116	11166	387.5	15x95
883	S117	11154	267.5	15x95
884	S118	11142	507.5	15x95
885	S119	11130	387.5	15x95
886	S120	11118	267.5	15x95
887	S121	11106	507.5	15x95
888	S122	11094	387.5	15x95
889	S123	11082	267.5	15x95
890	S124	11070	507.5	15x95
891	S125	11058	387.5	15x95
892	S126	11046	267.5	15x95
893	S127	11034	507.5	15x95
894	S128	11022	387.5	15x95
895	S129	11010	267.5	15x95
896	S130	10998	507.5	15x95
897	S131	10986	387.5	15x95
898	S132	10974	267.5	15x95
899	S133	10962	507.5	15x95
900	S134	10950	387.5	15x95

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No.	Name	X	Y	Bump size (μm)
901	S135	10938	267.5	15x95
902	S136	10926	507.5	15x95
903	S137	10914	387.5	15x95
904	S138	10902	267.5	15x95
905	S139	10890	507.5	15x95
906	S140	10878	387.5	15x95
907	S141	10866	267.5	15x95
908	S142	10854	507.5	15x95
909	S143	10842	387.5	15x95
910	S144	10830	267.5	15x95
911	S145	10818	507.5	15x95
912	S146	10806	387.5	15x95
913	S147	10794	267.5	15x95
914	S148	10782	507.5	15x95
915	S149	10770	387.5	15x95
916	S150	10758	267.5	15x95
917	S151	10746	507.5	15x95
918	S152	10734	387.5	15x95
919	S153	10722	267.5	15x95
920	S154	10710	507.5	15x95
921	S155	10698	387.5	15x95
922	S156	10686	267.5	15x95
923	S157	10674	507.5	15x95
924	S158	10662	387.5	15x95
925	S159	10650	267.5	15x95
926	S160	10638	507.5	15x95
927	S161	10626	387.5	15x95
928	S162	10614	267.5	15x95
929	S163	10602	507.5	15x95
930	S164	10590	387.5	15x95
931	S165	10578	267.5	15x95
932	S166	10566	507.5	15x95
933	S167	10554	387.5	15x95
934	S168	10542	267.5	15x95
935	S169	10530	507.5	15x95
936	S170	10518	387.5	15x95
937	S171	10506	267.5	15x95
938	S172	10494	507.5	15x95
939	S173	10482	387.5	15x95
940	S174	10470	267.5	15x95
941	S175	10458	507.5	15x95
942	S176	10446	387.5	15x95
943	S177	10434	267.5	15x95
944	S178	10422	507.5	15x95
945	S179	10410	387.5	15x95
946	S180	10398	267.5	15x95
947	S181	10386	507.5	15x95
948	S182	10374	387.5	15x95
949	S183	10362	267.5	15x95
950	S184	10350	507.5	15x95

No.	Name	X	Y	Bump size (μm)
951	S185	10338	387.5	15x95
952	S186	10326	267.5	15x95
953	S187	10314	507.5	15x95
954	S188	10302	387.5	15x95
955	S189	10290	267.5	15x95
956	S190	10278	507.5	15x95
957	S191	10266	387.5	15x95
958	S192	10254	267.5	15x95
959	S193	10242	507.5	15x95
960	S194	10230	387.5	15x95
961	S195	10218	267.5	15x95
962	S196	10206	507.5	15x95
963	S197	10194	387.5	15x95
964	S198	10182	267.5	15x95
965	S199	10170	507.5	15x95
966	S200	10158	387.5	15x95
967	S201	10146	267.5	15x95
968	S202	10134	507.5	15x95
969	S203	10122	387.5	15x95
970	S204	10110	267.5	15x95
971	S205	10098	507.5	15x95
972	S206	10086	387.5	15x95
973	S207	10074	267.5	15x95
974	S208	10062	507.5	15x95
975	S209	10050	387.5	15x95
976	S210	10038	267.5	15x95
977	S211	10026	507.5	15x95
978	S212	10014	387.5	15x95
979	S213	10002	267.5	15x95
980	S214	9990	507.5	15x95
981	S215	9978	387.5	15x95
982	S216	9966	267.5	15x95
983	S217	9954	507.5	15x95
984	S218	9942	387.5	15x95
985	S219	9930	267.5	15x95
986	S220	9918	507.5	15x95
987	S221	9906	387.5	15x95
988	S222	9894	267.5	15x95
989	S223	9882	507.5	15x95
990	S224	9870	387.5	15x95
991	S225	9858	267.5	15x95
992	S226	9846	507.5	15x95
993	S227	9834	387.5	15x95
994	S228	9822	267.5	15x95
995	S229	9810	507.5	15x95
996	S230	9798	387.5	15x95
997	S231	9786	267.5	15x95
998	S232	9774	507.5	15x95
999	S233	9762	387.5	15x95
1000	S234	9750	267.5	15x95

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No.	Name	X	Y	Bump size (μm)
1001	S235	9738	507.5	15x95
1002	S236	9726	387.5	15x95
1003	S237	9714	267.5	15x95
1004	S238	9702	507.5	15x95
1005	S239	9690	387.5	15x95
1006	S240	9678	267.5	15x95
1007	S241	9666	507.5	15x95
1008	S242	9654	387.5	15x95
1009	S243	9642	267.5	15x95
1010	S244	9630	507.5	15x95
1011	S245	9618	387.5	15x95
1012	S246	9606	267.5	15x95
1013	S247	9594	507.5	15x95
1014	S248	9582	387.5	15x95
1015	S249	9570	267.5	15x95
1016	S250	9558	507.5	15x95
1017	S251	9546	387.5	15x95
1018	S252	9534	267.5	15x95
1019	S253	9522	507.5	15x95
1020	S254	9510	387.5	15x95
1021	S255	9498	267.5	15x95
1022	S256	9486	507.5	15x95
1023	S257	9474	387.5	15x95
1024	S258	9462	267.5	15x95
1025	S259	9450	507.5	15x95
1026	S260	9438	387.5	15x95
1027	S261	9426	267.5	15x95
1028	S262	9414	507.5	15x95
1029	S263	9402	387.5	15x95
1030	S264	9390	267.5	15x95
1031	S265	9378	507.5	15x95
1032	S266	9366	387.5	15x95
1033	S267	9354	267.5	15x95
1034	S268	9342	507.5	15x95
1035	S269	9330	387.5	15x95
1036	S270	9318	267.5	15x95
1037	S271	9306	507.5	15x95
1038	S272	9294	387.5	15x95
1039	S273	9282	267.5	15x95
1040	S274	9270	507.5	15x95
1041	S275	9258	387.5	15x95
1042	S276	9246	267.5	15x95
1043	S277	9234	507.5	15x95
1044	S278	9222	387.5	15x95
1045	S279	9210	267.5	15x95
1046	S280	9198	507.5	15x95
1047	S281	9186	387.5	15x95
1048	S282	9174	267.5	15x95
1049	S283	9162	507.5	15x95
1050	S284	9150	387.5	15x95

No.	Name	X	Y	Bump size (μm)
1051	S285	9138	267.5	15x95
1052	S286	9126	507.5	15x95
1053	S287	9114	387.5	15x95
1054	S288	9102	267.5	15x95
1055	S289	9090	507.5	15x95
1056	S290	9078	387.5	15x95
1057	S291	9066	267.5	15x95
1058	S292	9054	507.5	15x95
1059	S293	9042	387.5	15x95
1060	S294	9030	267.5	15x95
1061	S295	9018	507.5	15x95
1062	S296	9006	387.5	15x95
1063	S297	8994	267.5	15x95
1064	S298	8982	507.5	15x95
1065	S299	8970	387.5	15x95
1066	S300	8958	267.5	15x95
1067	S301	8946	507.5	15x95
1068	S302	8934	387.5	15x95
1069	S303	8922	267.5	15x95
1070	S304	8910	507.5	15x95
1071	S305	8898	387.5	15x95
1072	S306	8886	267.5	15x95
1073	S307	8874	507.5	15x95
1074	S308	8862	387.5	15x95
1075	S309	8850	267.5	15x95
1076	S310	8838	507.5	15x95
1077	S311	8826	387.5	15x95
1078	S312	8814	267.5	15x95
1079	S313	8802	507.5	15x95
1080	S314	8790	387.5	15x95
1081	S315	8778	267.5	15x95
1082	S316	8766	507.5	15x95
1083	S317	8754	387.5	15x95
1084	S318	8742	267.5	15x95
1085	S319	8730	507.5	15x95
1086	S320	8718	387.5	15x95
1087	S321	8706	267.5	15x95
1088	S322	8694	507.5	15x95
1089	S323	8682	387.5	15x95
1090	S324	8670	267.5	15x95
1091	S325	8658	507.5	15x95
1092	S326	8646	387.5	15x95
1093	S327	8634	267.5	15x95
1094	S328	8622	507.5	15x95
1095	S329	8610	387.5	15x95
1096	S330	8598	267.5	15x95
1097	S331	8586	507.5	15x95
1098	S332	8574	387.5	15x95
1099	S333	8562	267.5	15x95
1100	S334	8550	507.5	15x95

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No.	Name	X	Y	Bump size (μm)
1101	S335	8538	387.5	15x95
1102	S336	8526	267.5	15x95
1103	S337	8514	507.5	15x95
1104	S338	8502	387.5	15x95
1105	S339	8490	267.5	15x95
1106	S340	8478	507.5	15x95
1107	S341	8466	387.5	15x95
1108	S342	8454	267.5	15x95
1109	S343	8442	507.5	15x95
1110	S344	8430	387.5	15x95
1111	S345	8418	267.5	15x95
1112	S346	8406	507.5	15x95
1113	S347	8394	387.5	15x95
1114	S348	8382	267.5	15x95
1115	S349	8370	507.5	15x95
1116	S350	8358	387.5	15x95
1117	S351	8346	267.5	15x95
1118	S352	8334	507.5	15x95
1119	S353	8322	387.5	15x95
1120	S354	8310	267.5	15x95
1121	S355	8298	507.5	15x95
1122	S356	8286	387.5	15x95
1123	S357	8274	267.5	15x95
1124	S358	8262	507.5	15x95
1125	S359	8250	387.5	15x95
1126	S360	8238	267.5	15x95
1127	S361	8226	507.5	15x95
1128	S362	8214	387.5	15x95
1129	S363	8202	267.5	15x95
1130	S364	8190	507.5	15x95
1131	S365	8178	387.5	15x95
1132	S366	8166	267.5	15x95
1133	S367	8154	507.5	15x95
1134	S368	8142	387.5	15x95
1135	S369	8130	267.5	15x95
1136	S370	8118	507.5	15x95
1137	S371	8106	387.5	15x95
1138	S372	8094	267.5	15x95
1139	S373	8082	507.5	15x95
1140	S374	8070	387.5	15x95
1141	S375	8058	267.5	15x95
1142	S376	8046	507.5	15x95
1143	S377	8034	387.5	15x95
1144	S378	8022	267.5	15x95
1145	S379	8010	507.5	15x95
1146	S380	7998	387.5	15x95
1147	S381	7986	267.5	15x95
1148	S382	7974	507.5	15x95
1149	S383	7962	387.5	15x95
1150	S384	7950	267.5	15x95

No.	Name	X	Y	Bump size (μm)
1151	S385	7938	507.5	15x95
1152	S386	7926	387.5	15x95
1153	S387	7914	267.5	15x95
1154	S388	7902	507.5	15x95
1155	S389	7890	387.5	15x95
1156	S390	7878	267.5	15x95
1157	S391	7866	507.5	15x95
1158	S392	7854	387.5	15x95
1159	S393	7842	267.5	15x95
1160	S394	7830	507.5	15x95
1161	S395	7818	387.5	15x95
1162	S396	7806	267.5	15x95
1163	S397	7794	507.5	15x95
1164	S398	7782	387.5	15x95
1165	S399	7770	267.5	15x95
1166	S400	7758	507.5	15x95
1167	S401	7746	387.5	15x95
1168	S402	7734	267.5	15x95
1169	S403	7722	507.5	15x95
1170	S404	7710	387.5	15x95
1171	S405	7698	267.5	15x95
1172	S406	7686	507.5	15x95
1173	S407	7674	387.5	15x95
1174	S408	7662	267.5	15x95
1175	S409	7650	507.5	15x95
1176	S410	7638	387.5	15x95
1177	S411	7626	267.5	15x95
1178	S412	7614	507.5	15x95
1179	S413	7602	387.5	15x95
1180	S414	7590	267.5	15x95
1181	S415	7578	507.5	15x95
1182	S416	7566	387.5	15x95
1183	S417	7554	267.5	15x95
1184	S418	7542	507.5	15x95
1185	S419	7530	387.5	15x95
1186	S420	7518	267.5	15x95
1187	S421	7506	507.5	15x95
1188	S422	7494	387.5	15x95
1189	S423	7482	267.5	15x95
1190	S424	7470	507.5	15x95
1191	S425	7458	387.5	15x95
1192	S426	7446	267.5	15x95
1193	S427	7434	507.5	15x95
1194	S428	7422	387.5	15x95
1195	S429	7410	267.5	15x95
1196	S430	7398	507.5	15x95
1197	S431	7386	387.5	15x95
1198	S432	7374	267.5	15x95
1199	S433	7362	507.5	15x95
1200	S434	7350	387.5	15x95

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No.	Name	X	Y	Bump size (μm)
1201	S435	7338	267.5	15x95
1202	S436	7326	507.5	15x95
1203	S437	7314	387.5	15x95
1204	S438	7302	267.5	15x95
1205	S439	7290	507.5	15x95
1206	S440	7278	387.5	15x95
1207	S441	7266	267.5	15x95
1208	S442	7254	507.5	15x95
1209	S443	7242	387.5	15x95
1210	S444	7230	267.5	15x95
1211	S445	7218	507.5	15x95
1212	S446	7206	387.5	15x95
1213	S447	7194	267.5	15x95
1214	S448	7182	507.5	15x95
1215	S449	7170	387.5	15x95
1216	S450	7158	267.5	15x95
1217	S451	7146	507.5	15x95
1218	S452	7134	387.5	15x95
1219	S453	7122	267.5	15x95
1220	S454	7110	507.5	15x95
1221	S455	7098	387.5	15x95
1222	S456	7086	267.5	15x95
1223	S457	7074	507.5	15x95
1224	S458	7062	387.5	15x95
1225	S459	7050	267.5	15x95
1226	S460	7038	507.5	15x95
1227	S461	7026	387.5	15x95
1228	S462	7014	267.5	15x95
1229	S463	7002	507.5	15x95
1230	S464	6990	387.5	15x95
1231	S465	6978	267.5	15x95
1232	S466	6966	507.5	15x95
1233	S467	6954	387.5	15x95
1234	S468	6942	267.5	15x95
1235	S469	6930	507.5	15x95
1236	S470	6918	387.5	15x95
1237	S471	6906	267.5	15x95
1238	S472	6894	507.5	15x95
1239	S473	6882	387.5	15x95
1240	S474	6870	267.5	15x95
1241	S475	6858	507.5	15x95
1242	S476	6846	387.5	15x95
1243	S477	6834	267.5	15x95
1244	S478	6822	507.5	15x95
1245	S479	6810	387.5	15x95
1246	S480	6798	267.5	15x95
1247	S481	6786	507.5	15x95
1248	S482	6774	387.5	15x95
1249	S483	6762	267.5	15x95
1250	S484	6750	507.5	15x95

No.	Name	X	Y	Bump size (μm)
1251	S485	6738	387.5	15x95
1252	S486	6726	267.5	15x95
1253	S487	6714	507.5	15x95
1254	S488	6702	387.5	15x95
1255	S489	6690	267.5	15x95
1256	S490	6678	507.5	15x95
1257	S491	6666	387.5	15x95
1258	S492	6654	267.5	15x95
1259	S493	6642	507.5	15x95
1260	S494	6630	387.5	15x95
1261	S495	6618	267.5	15x95
1262	S496	6606	507.5	15x95
1263	S497	6594	387.5	15x95
1264	S498	6582	267.5	15x95
1265	S499	6570	507.5	15x95
1266	S500	6558	387.5	15x95
1267	S501	6546	267.5	15x95
1268	S502	6534	507.5	15x95
1269	S503	6522	387.5	15x95
1270	S504	6510	267.5	15x95
1271	S505	6498	507.5	15x95
1272	S506	6486	387.5	15x95
1273	S507	6474	267.5	15x95
1274	S508	6462	507.5	15x95
1275	S509	6450	387.5	15x95
1276	S510	6438	267.5	15x95
1277	S511	6426	507.5	15x95
1278	S512	6414	387.5	15x95
1279	S513	6402	267.5	15x95
1280	S514	6390	507.5	15x95
1281	S515	6378	387.5	15x95
1282	S516	6366	267.5	15x95
1283	S517	6354	507.5	15x95
1284	S518	6342	387.5	15x95
1285	S519	6330	267.5	15x95
1286	S520	6318	507.5	15x95
1287	S521	6306	387.5	15x95
1288	S522	6294	267.5	15x95
1289	S523	6282	507.5	15x95
1290	S524	6270	387.5	15x95
1291	S525	6258	267.5	15x95
1292	S526	6246	507.5	15x95
1293	S527	6234	387.5	15x95
1294	S528	6222	267.5	15x95
1295	S529	6210	507.5	15x95
1296	S530	6198	387.5	15x95
1297	S531	6186	267.5	15x95
1298	S532	6174	507.5	15x95
1299	S533	6162	387.5	15x95
1300	S534	6150	267.5	15x95

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No.	Name	X	Y	Bump size (μm)
1301	S535	6138	507.5	15x95
1302	S536	6126	387.5	15x95
1303	S537	6114	267.5	15x95
1304	S538	6102	507.5	15x95
1305	S539	6090	387.5	15x95
1306	S540	6078	267.5	15x95
1307	S541	6066	507.5	15x95
1308	S542	6054	387.5	15x95
1309	S543	6042	267.5	15x95
1310	S544	6030	507.5	15x95
1311	S545	6018	387.5	15x95
1312	S546	6006	267.5	15x95
1313	S547	5994	507.5	15x95
1314	S548	5982	387.5	15x95
1315	S549	5970	267.5	15x95
1316	S550	5958	507.5	15x95
1317	S551	5946	387.5	15x95
1318	S552	5934	267.5	15x95
1319	S553	5922	507.5	15x95
1320	S554	5910	387.5	15x95
1321	S555	5898	267.5	15x95
1322	S556	5886	507.5	15x95
1323	S557	5874	387.5	15x95
1324	S558	5862	267.5	15x95
1325	S559	5850	507.5	15x95
1326	S560	5838	387.5	15x95
1327	S561	5826	267.5	15x95
1328	S562	5814	507.5	15x95
1329	S563	5802	387.5	15x95
1330	S564	5790	267.5	15x95
1331	S565	5778	507.5	15x95
1332	S566	5766	387.5	15x95
1333	S567	5754	267.5	15x95
1334	S568	5742	507.5	15x95
1335	S569	5730	387.5	15x95
1336	S570	5718	267.5	15x95
1337	S571	5706	507.5	15x95
1338	S572	5694	387.5	15x95
1339	S573	5682	267.5	15x95
1340	S574	5670	507.5	15x95
1341	S575	5658	387.5	15x95
1342	S576	5646	267.5	15x95
1343	S577	5634	507.5	15x95
1344	S578	5622	387.5	15x95
1345	S579	5610	267.5	15x95
1346	S580	5598	507.5	15x95
1347	S581	5586	387.5	15x95
1348	S582	5574	267.5	15x95
1349	S583	5562	507.5	15x95
1350	S584	5550	387.5	15x95

No.	Name	X	Y	Bump size (μm)
1351	S585	5538	267.5	15x95
1352	S586	5526	507.5	15x95
1353	S587	5514	387.5	15x95
1354	S588	5502	267.5	15x95
1355	S589	5490	507.5	15x95
1356	S590	5478	387.5	15x95
1357	S591	5466	267.5	15x95
1358	S592	5454	507.5	15x95
1359	S593	5442	387.5	15x95
1360	S594	5430	267.5	15x95
1361	S595	5418	507.5	15x95
1362	S596	5406	387.5	15x95
1363	S597	5394	267.5	15x95
1364	S598	5382	507.5	15x95
1365	S599	5370	387.5	15x95
1366	S600	5358	267.5	15x95
1367	S601	5346	507.5	15x95
1368	S602	5334	387.5	15x95
1369	S603	5322	267.5	15x95
1370	S604	5310	507.5	15x95
1371	S605	5298	387.5	15x95
1372	S606	5286	267.5	15x95
1373	S607	5274	507.5	15x95
1374	S608	5262	387.5	15x95
1375	S609	5250	267.5	15x95
1376	S610	5238	507.5	15x95
1377	S611	5226	387.5	15x95
1378	S612	5214	267.5	15x95
1379	S613	5202	507.5	15x95
1380	S614	5190	387.5	15x95
1381	S615	5178	267.5	15x95
1382	S616	5166	507.5	15x95
1383	S617	5154	387.5	15x95
1384	S618	5142	267.5	15x95
1385	S619	5130	507.5	15x95
1386	S620	5118	387.5	15x95
1387	S621	5106	267.5	15x95
1388	S622	5094	507.5	15x95
1389	S623	5082	387.5	15x95
1390	S624	5070	267.5	15x95
1391	S625	5058	507.5	15x95
1392	S626	5046	387.5	15x95
1393	S627	5034	267.5	15x95
1394	S628	5022	507.5	15x95
1395	S629	5010	387.5	15x95
1396	S630	4998	267.5	15x95
1397	S631	4986	507.5	15x95
1398	S632	4974	387.5	15x95
1399	S633	4962	267.5	15x95
1400	S634	4950	507.5	15x95

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No.	Name	X	Y	Bump size (μm)
1401	S635	4938	387.5	15x95
1402	S636	4926	267.5	15x95
1403	S637	4914	507.5	15x95
1404	S638	4902	387.5	15x95
1405	S639	4890	267.5	15x95
1406	S640	4878	507.5	15x95
1407	S641	4866	387.5	15x95
1408	S642	4854	267.5	15x95
1409	S643	4842	507.5	15x95
1410	S644	4830	387.5	15x95
1411	S645	4818	267.5	15x95
1412	S646	4806	507.5	15x95
1413	S647	4794	387.5	15x95
1414	S648	4782	267.5	15x95
1415	S649	4770	507.5	15x95
1416	S650	4758	387.5	15x95
1417	S651	4746	267.5	15x95
1418	S652	4734	507.5	15x95
1419	S653	4722	387.5	15x95
1420	S654	4710	267.5	15x95
1421	S655	4698	507.5	15x95
1422	S656	4686	387.5	15x95
1423	S657	4674	267.5	15x95
1424	S658	4662	507.5	15x95
1425	S659	4650	387.5	15x95
1426	S660	4638	267.5	15x95
1427	S661	4626	507.5	15x95
1428	S662	4614	387.5	15x95
1429	S663	4602	267.5	15x95
1430	S664	4590	507.5	15x95
1431	S665	4578	387.5	15x95
1432	S666	4566	267.5	15x95
1433	S667	4554	507.5	15x95
1434	S668	4542	387.5	15x95
1435	S669	4530	267.5	15x95
1436	S670	4518	507.5	15x95
1437	S671	4506	387.5	15x95
1438	S672	4494	267.5	15x95
1439	S673	4482	507.5	15x95
1440	S674	4470	387.5	15x95
1441	S675	4458	267.5	15x95
1442	S676	4446	507.5	15x95
1443	S677	4434	387.5	15x95
1444	S678	4422	267.5	15x95
1445	S679	4410	507.5	15x95
1446	S680	4398	387.5	15x95
1447	S681	4386	267.5	15x95
1448	S682	4374	507.5	15x95
1449	S683	4362	387.5	15x95
1450	S684	4350	267.5	15x95

No.	Name	X	Y	Bump size (μm)
1451	S685	4338	507.5	15x95
1452	S686	4326	387.5	15x95
1453	S687	4314	267.5	15x95
1454	S688	4302	507.5	15x95
1455	S689	4290	387.5	15x95
1456	S690	4278	267.5	15x95
1457	S691	4266	507.5	15x95
1458	S692	4254	387.5	15x95
1459	S693	4242	267.5	15x95
1460	S694	4230	507.5	15x95
1461	S695	4218	387.5	15x95
1462	S696	4206	267.5	15x95
1463	S697	4194	507.5	15x95
1464	S698	4182	387.5	15x95
1465	S699	4170	267.5	15x95
1466	S700	4158	507.5	15x95
1467	S701	4146	387.5	15x95
1468	S702	4134	267.5	15x95
1469	S703	4122	507.5	15x95
1470	S704	4110	387.5	15x95
1471	S705	4098	267.5	15x95
1472	S706	4086	507.5	15x95
1473	S707	4074	387.5	15x95
1474	S708	4062	267.5	15x95
1475	S709	4050	507.5	15x95
1476	S710	4038	387.5	15x95
1477	S711	4026	267.5	15x95
1478	S712	4014	507.5	15x95
1479	S713	4002	387.5	15x95
1480	S714	3990	267.5	15x95
1481	S715	3978	507.5	15x95
1482	S716	3966	387.5	15x95
1483	S717	3954	267.5	15x95
1484	S718	3942	507.5	15x95
1485	S719	3930	387.5	15x95
1486	S720	3918	267.5	15x95
1487	S721	3906	507.5	15x95
1488	S722	3894	387.5	15x95
1489	S723	3882	267.5	15x95
1490	S724	3870	507.5	15x95
1491	S725	3858	387.5	15x95
1492	S726	3846	267.5	15x95
1493	S727	3834	507.5	15x95
1494	S728	3822	387.5	15x95
1495	S729	3810	267.5	15x95
1496	S730	3798	507.5	15x95
1497	S731	3786	387.5	15x95
1498	S732	3774	267.5	15x95
1499	S733	3762	507.5	15x95
1500	S734	3750	387.5	15x95

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No.	Name	X	Y	Bump size (μm)
1501	S735	3738	267.5	15x95
1502	S736	3726	507.5	15x95
1503	S737	3714	387.5	15x95
1504	S738	3702	267.5	15x95
1505	S739	3690	507.5	15x95
1506	S740	3678	387.5	15x95
1507	S741	3666	267.5	15x95
1508	S742	3654	507.5	15x95
1509	S743	3642	387.5	15x95
1510	S744	3630	267.5	15x95
1511	S745	3618	507.5	15x95
1512	S746	3606	387.5	15x95
1513	S747	3594	267.5	15x95
1514	S748	3582	507.5	15x95
1515	S749	3570	387.5	15x95
1516	S750	3558	267.5	15x95
1517	S751	3546	507.5	15x95
1518	S752	3534	387.5	15x95
1519	S753	3522	267.5	15x95
1520	S754	3510	507.5	15x95
1521	S755	3498	387.5	15x95
1522	S756	3486	267.5	15x95
1523	S757	3474	507.5	15x95
1524	S758	3462	387.5	15x95
1525	S759	3450	267.5	15x95
1526	S760	3438	507.5	15x95
1527	S761	3426	387.5	15x95
1528	S762	3414	267.5	15x95
1529	S763	3402	507.5	15x95
1530	S764	3390	387.5	15x95
1531	S765	3378	267.5	15x95
1532	S766	3366	507.5	15x95
1533	S767	3354	387.5	15x95
1534	S768	3342	267.5	15x95
1535	S769	3330	507.5	15x95
1536	S770	3318	387.5	15x95
1537	S771	3306	267.5	15x95
1538	S772	3294	507.5	15x95
1539	S773	3282	387.5	15x95
1540	S774	3270	267.5	15x95
1541	S775	3258	507.5	15x95
1542	S776	3246	387.5	15x95
1543	S777	3234	267.5	15x95
1544	S778	3222	507.5	15x95
1545	S779	3210	387.5	15x95
1546	S780	3198	267.5	15x95
1547	S781	3186	507.5	15x95
1548	S782	3174	387.5	15x95
1549	S783	3162	267.5	15x95
1550	S784	3150	507.5	15x95

No.	Name	X	Y	Bump size (μm)
1551	S785	3138	387.5	15x95
1552	S786	3126	267.5	15x95
1553	S787	3114	507.5	15x95
1554	S788	3102	387.5	15x95
1555	S789	3090	267.5	15x95
1556	S790	3078	507.5	15x95
1557	S791	3066	387.5	15x95
1558	S792	3054	267.5	15x95
1559	S793	3042	507.5	15x95
1560	S794	3030	387.5	15x95
1561	S795	3018	267.5	15x95
1562	S796	3006	507.5	15x95
1563	S797	2994	387.5	15x95
1564	S798	2982	267.5	15x95
1565	S799	2970	507.5	15x95
1566	S800	2958	387.5	15x95
1567	S801	2946	267.5	15x95
1568	S802	2934	507.5	15x95
1569	S803	2922	387.5	15x95
1570	S804	2910	267.5	15x95
1571	S805	2898	507.5	15x95
1572	S806	2886	387.5	15x95
1573	S807	2874	267.5	15x95
1574	S808	2862	507.5	15x95
1575	S809	2850	387.5	15x95
1576	S810	2838	267.5	15x95
1577	S811	2826	507.5	15x95
1578	S812	2814	387.5	15x95
1579	S813	2802	267.5	15x95
1580	S814	2790	507.5	15x95
1581	S815	2778	387.5	15x95
1582	S816	2766	267.5	15x95
1583	S817	2754	507.5	15x95
1584	S818	2742	387.5	15x95
1585	S819	2730	267.5	15x95
1586	S820	2718	507.5	15x95
1587	S821	2706	387.5	15x95
1588	S822	2694	267.5	15x95
1589	S823	2682	507.5	15x95
1590	S824	2670	387.5	15x95
1591	S825	2658	267.5	15x95
1592	S826	2646	507.5	15x95
1593	S827	2634	387.5	15x95
1594	S828	2622	267.5	15x95
1595	S829	2610	507.5	15x95
1596	S830	2598	387.5	15x95
1597	S831	2586	267.5	15x95
1598	S832	2574	507.5	15x95
1599	S833	2562	387.5	15x95
1600	S834	2550	267.5	15x95

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No.	Name	X	Y	Bump size (μm)
1601	S835	2538	507.5	15x95
1602	S836	2526	387.5	15x95
1603	S837	2514	267.5	15x95
1604	S838	2502	507.5	15x95
1605	S839	2490	387.5	15x95
1606	S840	2478	267.5	15x95
1607	S841	2466	507.5	15x95
1608	S842	2454	387.5	15x95
1609	S843	2442	267.5	15x95
1610	S844	2430	507.5	15x95
1611	S845	2418	387.5	15x95
1612	S846	2406	267.5	15x95
1613	S847	2394	507.5	15x95
1614	S848	2382	387.5	15x95
1615	S849	2370	267.5	15x95
1616	S850	2358	507.5	15x95
1617	S851	2346	387.5	15x95
1618	S852	2334	267.5	15x95
1619	S853	2322	507.5	15x95
1620	S854	2310	387.5	15x95
1621	S855	2298	267.5	15x95
1622	S856	2286	507.5	15x95
1623	S857	2274	387.5	15x95
1624	S858	2262	267.5	15x95
1625	S859	2250	507.5	15x95
1626	S860	2238	387.5	15x95
1627	S861	2226	267.5	15x95
1628	S862	2214	507.5	15x95
1629	S863	2202	387.5	15x95
1630	S864	2190	267.5	15x95
1631	S865	2178	507.5	15x95
1632	S866	2166	387.5	15x95
1633	S867	2154	267.5	15x95
1634	S868	2142	507.5	15x95
1635	S869	2130	387.5	15x95
1636	S870	2118	267.5	15x95
1637	S871	2106	507.5	15x95
1638	S872	2094	387.5	15x95
1639	S873	2082	267.5	15x95
1640	S874	2070	507.5	15x95
1641	S875	2058	387.5	15x95
1642	S876	2046	267.5	15x95
1643	S877	2034	507.5	15x95
1644	S878	2022	387.5	15x95
1645	S879	2010	267.5	15x95
1646	S880	1998	507.5	15x95
1647	S881	1986	387.5	15x95
1648	S882	1974	267.5	15x95
1649	S883	1962	507.5	15x95
1650	S884	1950	387.5	15x95

No.	Name	X	Y	Bump size (μm)
1651	S885	1938	267.5	15x95
1652	S886	1926	507.5	15x95
1653	S887	1914	387.5	15x95
1654	S888	1902	267.5	15x95
1655	S889	1890	507.5	15x95
1656	S890	1878	387.5	15x95
1657	S891	1866	267.5	15x95
1658	S892	1854	507.5	15x95
1659	S893	1842	387.5	15x95
1660	S894	1830	267.5	15x95
1661	S895	1818	507.5	15x95
1662	S896	1806	387.5	15x95
1663	S897	1794	267.5	15x95
1664	S898	1782	507.5	15x95
1665	S899	1770	387.5	15x95
1666	S900	1758	267.5	15x95
1667	S901	1746	507.5	15x95
1668	S902	1734	387.5	15x95
1669	S903	1722	267.5	15x95
1670	S904	1710	507.5	15x95
1671	S905	1698	387.5	15x95
1672	S906	1686	267.5	15x95
1673	S907	1674	507.5	15x95
1674	S908	1662	387.5	15x95
1675	S909	1650	267.5	15x95
1676	S910	1638	507.5	15x95
1677	S911	1626	387.5	15x95
1678	S912	1614	267.5	15x95
1679	S913	1602	507.5	15x95
1680	S914	1590	387.5	15x95
1681	S915	1578	267.5	15x95
1682	S916	1566	507.5	15x95
1683	S917	1554	387.5	15x95
1684	S918	1542	267.5	15x95
1685	S919	1530	507.5	15x95
1686	S920	1518	387.5	15x95
1687	S921	1506	267.5	15x95
1688	S922	1494	507.5	15x95
1689	S923	1482	387.5	15x95
1690	S924	1470	267.5	15x95
1691	S925	1458	507.5	15x95
1692	S926	1446	387.5	15x95
1693	S927	1434	267.5	15x95
1694	S928	1422	507.5	15x95
1695	S929	1410	387.5	15x95
1696	S930	1398	267.5	15x95
1697	S931	1386	507.5	15x95
1698	S932	1374	387.5	15x95
1699	S933	1362	267.5	15x95
1700	S934	1350	507.5	15x95

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No.	Name	X	Y	Bump size (μm)
1701	S935	1338	387.5	15x95
1702	S936	1326	267.5	15x95
1703	S937	1314	507.5	15x95
1704	S938	1302	387.5	15x95
1705	S939	1290	267.5	15x95
1706	S940	1278	507.5	15x95
1707	S941	1266	387.5	15x95
1708	S942	1254	267.5	15x95
1709	S943	1242	507.5	15x95
1710	S944	1230	387.5	15x95
1711	S945	1218	267.5	15x95
1712	S946	1206	507.5	15x95
1713	S947	1194	387.5	15x95
1714	S948	1182	267.5	15x95
1715	S949	1170	507.5	15x95
1716	S950	1158	387.5	15x95
1717	S951	1146	267.5	15x95
1718	S952	1134	507.5	15x95
1719	S953	1122	387.5	15x95
1720	S954	1110	267.5	15x95
1721	S955	1098	507.5	15x95
1722	S956	1086	387.5	15x95
1723	S957	1074	267.5	15x95
1724	S958	1062	507.5	15x95
1725	S959	1050	387.5	15x95
1726	S960	1038	267.5	15x95
1727	DUMMY	1026	507.5	15x95
1728	DUMMY	990	507.5	15x95
1729	DUMMY	954	507.5	15x95
1730	DUMMY	918	507.5	15x95
1731	DUMMY	882	507.5	15x95
1732	DUMMY	846	507.5	15x95
1733	DUMMY	810	507.5	15x95
1734	DUMMY	774	507.5	15x95
1735	DUMMY	738	507.5	15x95
1736	DUMMY	702	507.5	15x95
1737	DUMMY	666	507.5	15x95
1738	DUMMY	630	507.5	15x95
1739	DUMMY	594	507.5	15x95
1740	DUMMY	558	507.5	15x95
1741	DUMMY	522	507.5	15x95
1742	DUMMY	486	507.5	15x95
1743	DUMMY	450	507.5	15x95
1744	DUMMY	414	507.5	15x95
1745	DUMMY	378	507.5	15x95
1746	DUMMY	342	507.5	15x95
1747	DUMMY	306	507.5	15x95
1748	DUMMY	270	507.5	15x95
1749	DUMMY	234	507.5	15x95
1750	DUMMY	198	507.5	15x95

No.	Name	X	Y	Bump size (μm)
1751	DUMMY	162	507.5	15x95
1752	DUMMY	126	507.5	15x95
1753	DUMMY	90	507.5	15x95
1754	DUMMY	54	507.5	15x95
1755	DUMMY	18	507.5	15x95
1756	DUMMY	-18	507.5	15x95
1757	DUMMY	-54	507.5	15x95
1758	DUMMY	-90	507.5	15x95
1759	DUMMY	-126	507.5	15x95
1760	DUMMY	-162	507.5	15x95
1761	DUMMY	-198	507.5	15x95
1762	DUMMY	-234	507.5	15x95
1763	DUMMY	-270	507.5	15x95
1764	DUMMY	-306	507.5	15x95
1765	DUMMY	-342	507.5	15x95
1766	DUMMY	-378	507.5	15x95
1767	DUMMY	-414	507.5	15x95
1768	DUMMY	-450	507.5	15x95
1769	DUMMY	-486	507.5	15x95
1770	DUMMY	-522	507.5	15x95
1771	DUMMY	-558	507.5	15x95
1772	DUMMY	-594	507.5	15x95
1773	DUMMY	-630	507.5	15x95
1774	DUMMY	-666	507.5	15x95
1775	DUMMY	-702	507.5	15x95
1776	DUMMY	-738	507.5	15x95
1777	DUMMY	-774	507.5	15x95
1778	DUMMY	-810	507.5	15x95
1779	DUMMY	-846	507.5	15x95
1780	DUMMY	-882	507.5	15x95
1781	DUMMY	-918	507.5	15x95
1782	DUMMY	-954	507.5	15x95
1783	DUMMY	-990	507.5	15x95
1784	DUMMY	-1026	507.5	15x95
1785	S961	-1038	267.5	15x95
1786	S962	-1050	387.5	15x95
1787	S963	-1062	507.5	15x95
1788	S964	-1074	267.5	15x95
1789	S965	-1086	387.5	15x95
1790	S966	-1098	507.5	15x95
1791	S967	-1110	267.5	15x95
1792	S968	-1122	387.5	15x95
1793	S969	-1134	507.5	15x95
1794	S970	-1146	267.5	15x95
1795	S971	-1158	387.5	15x95
1796	S972	-1170	507.5	15x95
1797	S973	-1182	267.5	15x95
1798	S974	-1194	387.5	15x95
1799	S975	-1206	507.5	15x95
1800	S976	-1218	267.5	15x95

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No.	Name	X	Y	Bump size (μm)
1801	S977	-1230	387.5	15x95
1802	S978	-1242	507.5	15x95
1803	S979	-1254	267.5	15x95
1804	S980	-1266	387.5	15x95
1805	S981	-1278	507.5	15x95
1806	S982	-1290	267.5	15x95
1807	S983	-1302	387.5	15x95
1808	S984	-1314	507.5	15x95
1809	S985	-1326	267.5	15x95
1810	S986	-1338	387.5	15x95
1811	S987	-1350	507.5	15x95
1812	S988	-1362	267.5	15x95
1813	S989	-1374	387.5	15x95
1814	S990	-1386	507.5	15x95
1815	S991	-1398	267.5	15x95
1816	S992	-1410	387.5	15x95
1817	S993	-1422	507.5	15x95
1818	S994	-1434	267.5	15x95
1819	S995	-1446	387.5	15x95
1820	S996	-1458	507.5	15x95
1821	S997	-1470	267.5	15x95
1822	S998	-1482	387.5	15x95
1823	S999	-1494	507.5	15x95
1824	S1000	-1506	267.5	15x95
1825	S1001	-1518	387.5	15x95
1826	S1002	-1530	507.5	15x95
1827	S1003	-1542	267.5	15x95
1828	S1004	-1554	387.5	15x95
1829	S1005	-1566	507.5	15x95
1830	S1006	-1578	267.5	15x95
1831	S1007	-1590	387.5	15x95
1832	S1008	-1602	507.5	15x95
1833	S1009	-1614	267.5	15x95
1834	S1010	-1626	387.5	15x95
1835	S1011	-1638	507.5	15x95
1836	S1012	-1650	267.5	15x95
1837	S1013	-1662	387.5	15x95
1838	S1014	-1674	507.5	15x95
1839	S1015	-1686	267.5	15x95
1840	S1016	-1698	387.5	15x95
1841	S1017	-1710	507.5	15x95
1842	S1018	-1722	267.5	15x95
1843	S1019	-1734	387.5	15x95
1844	S1020	-1746	507.5	15x95
1845	S1021	-1758	267.5	15x95
1846	S1022	-1770	387.5	15x95
1847	S1023	-1782	507.5	15x95
1848	S1024	-1794	267.5	15x95
1849	S1025	-1806	387.5	15x95
1850	S1026	-1818	507.5	15x95

No.	Name	X	Y	Bump size (μm)
1851	S1027	-1830	267.5	15x95
1852	S1028	-1842	387.5	15x95
1853	S1029	-1854	507.5	15x95
1854	S1030	-1866	267.5	15x95
1855	S1031	-1878	387.5	15x95
1856	S1032	-1890	507.5	15x95
1857	S1033	-1902	267.5	15x95
1858	S1034	-1914	387.5	15x95
1859	S1035	-1926	507.5	15x95
1860	S1036	-1938	267.5	15x95
1861	S1037	-1950	387.5	15x95
1862	S1038	-1962	507.5	15x95
1863	S1039	-1974	267.5	15x95
1864	S1040	-1986	387.5	15x95
1865	S1041	-1998	507.5	15x95
1866	S1042	-2010	267.5	15x95
1867	S1043	-2022	387.5	15x95
1868	S1044	-2034	507.5	15x95
1869	S1045	-2046	267.5	15x95
1870	S1046	-2058	387.5	15x95
1871	S1047	-2070	507.5	15x95
1872	S1048	-2082	267.5	15x95
1873	S1049	-2094	387.5	15x95
1874	S1050	-2106	507.5	15x95
1875	S1051	-2118	267.5	15x95
1876	S1052	-2130	387.5	15x95
1877	S1053	-2142	507.5	15x95
1878	S1054	-2154	267.5	15x95
1879	S1055	-2166	387.5	15x95
1880	S1056	-2178	507.5	15x95
1881	S1057	-2190	267.5	15x95
1882	S1058	-2202	387.5	15x95
1883	S1059	-2214	507.5	15x95
1884	S1060	-2226	267.5	15x95
1885	S1061	-2238	387.5	15x95
1886	S1062	-2250	507.5	15x95
1887	S1063	-2262	267.5	15x95
1888	S1064	-2274	387.5	15x95
1889	S1065	-2286	507.5	15x95
1890	S1066	-2298	267.5	15x95
1891	S1067	-2310	387.5	15x95
1892	S1068	-2322	507.5	15x95
1893	S1069	-2334	267.5	15x95
1894	S1070	-2346	387.5	15x95
1895	S1071	-2358	507.5	15x95
1896	S1072	-2370	267.5	15x95
1897	S1073	-2382	387.5	15x95
1898	S1074	-2394	507.5	15x95
1899	S1075	-2406	267.5	15x95
1900	S1076	-2418	387.5	15x95

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No.	Name	X	Y	Bump size (μm)
1901	S1077	-2430	507.5	15x95
1902	S1078	-2442	267.5	15x95
1903	S1079	-2454	387.5	15x95
1904	S1080	-2466	507.5	15x95
1905	S1081	-2478	267.5	15x95
1906	S1082	-2490	387.5	15x95
1907	S1083	-2502	507.5	15x95
1908	S1084	-2514	267.5	15x95
1909	S1085	-2526	387.5	15x95
1910	S1086	-2538	507.5	15x95
1911	S1087	-2550	267.5	15x95
1912	S1088	-2562	387.5	15x95
1913	S1089	-2574	507.5	15x95
1914	S1090	-2586	267.5	15x95
1915	S1091	-2598	387.5	15x95
1916	S1092	-2610	507.5	15x95
1917	S1093	-2622	267.5	15x95
1918	S1094	-2634	387.5	15x95
1919	S1095	-2646	507.5	15x95
1920	S1096	-2658	267.5	15x95
1921	S1097	-2670	387.5	15x95
1922	S1098	-2682	507.5	15x95
1923	S1099	-2694	267.5	15x95
1924	S1100	-2706	387.5	15x95
1925	S1101	-2718	507.5	15x95
1926	S1102	-2730	267.5	15x95
1927	S1103	-2742	387.5	15x95
1928	S1104	-2754	507.5	15x95
1929	S1105	-2766	267.5	15x95
1930	S1106	-2778	387.5	15x95
1931	S1107	-2790	507.5	15x95
1932	S1108	-2802	267.5	15x95
1933	S1109	-2814	387.5	15x95
1934	S1110	-2826	507.5	15x95
1935	S1111	-2838	267.5	15x95
1936	S1112	-2850	387.5	15x95
1937	S1113	-2862	507.5	15x95
1938	S1114	-2874	267.5	15x95
1939	S1115	-2886	387.5	15x95
1940	S1116	-2898	507.5	15x95
1941	S1117	-2910	267.5	15x95
1942	S1118	-2922	387.5	15x95
1943	S1119	-2934	507.5	15x95
1944	S1120	-2946	267.5	15x95
1945	S1121	-2958	387.5	15x95
1946	S1122	-2970	507.5	15x95
1947	S1123	-2982	267.5	15x95
1948	S1124	-2994	387.5	15x95
1949	S1125	-3006	507.5	15x95
1950	S1126	-3018	267.5	15x95

No.	Name	X	Y	Bump size (μm)
1951	S1127	-3030	387.5	15x95
1952	S1128	-3042	507.5	15x95
1953	S1129	-3054	267.5	15x95
1954	S1130	-3066	387.5	15x95
1955	S1131	-3078	507.5	15x95
1956	S1132	-3090	267.5	15x95
1957	S1133	-3102	387.5	15x95
1958	S1134	-3114	507.5	15x95
1959	S1135	-3126	267.5	15x95
1960	S1136	-3138	387.5	15x95
1961	S1137	-3150	507.5	15x95
1962	S1138	-3162	267.5	15x95
1963	S1139	-3174	387.5	15x95
1964	S1140	-3186	507.5	15x95
1965	S1141	-3198	267.5	15x95
1966	S1142	-3210	387.5	15x95
1967	S1143	-3222	507.5	15x95
1968	S1144	-3234	267.5	15x95
1969	S1145	-3246	387.5	15x95
1970	S1146	-3258	507.5	15x95
1971	S1147	-3270	267.5	15x95
1972	S1148	-3282	387.5	15x95
1973	S1149	-3294	507.5	15x95
1974	S1150	-3306	267.5	15x95
1975	S1151	-3318	387.5	15x95
1976	S1152	-3330	507.5	15x95
1977	S1153	-3342	267.5	15x95
1978	S1154	-3354	387.5	15x95
1979	S1155	-3366	507.5	15x95
1980	S1156	-3378	267.5	15x95
1981	S1157	-3390	387.5	15x95
1982	S1158	-3402	507.5	15x95
1983	S1159	-3414	267.5	15x95
1984	S1160	-3426	387.5	15x95
1985	S1161	-3438	507.5	15x95
1986	S1162	-3450	267.5	15x95
1987	S1163	-3462	387.5	15x95
1988	S1164	-3474	507.5	15x95
1989	S1165	-3486	267.5	15x95
1990	S1166	-3498	387.5	15x95
1991	S1167	-3510	507.5	15x95
1992	S1168	-3522	267.5	15x95
1993	S1169	-3534	387.5	15x95
1994	S1170	-3546	507.5	15x95
1995	S1171	-3558	267.5	15x95
1996	S1172	-3570	387.5	15x95
1997	S1173	-3582	507.5	15x95
1998	S1174	-3594	267.5	15x95
1999	S1175	-3606	387.5	15x95
2000	S1176	-3618	507.5	15x95

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No.	Name	X	Y	Bump size (μm)
2001	S1177	-3630	267.5	15x95
2002	S1178	-3642	387.5	15x95
2003	S1179	-3654	507.5	15x95
2004	S1180	-3666	267.5	15x95
2005	S1181	-3678	387.5	15x95
2006	S1182	-3690	507.5	15x95
2007	S1183	-3702	267.5	15x95
2008	S1184	-3714	387.5	15x95
2009	S1185	-3726	507.5	15x95
2010	S1186	-3738	267.5	15x95
2011	S1187	-3750	387.5	15x95
2012	S1188	-3762	507.5	15x95
2013	S1189	-3774	267.5	15x95
2014	S1190	-3786	387.5	15x95
2015	S1191	-3798	507.5	15x95
2016	S1192	-3810	267.5	15x95
2017	S1193	-3822	387.5	15x95
2018	S1194	-3834	507.5	15x95
2019	S1195	-3846	267.5	15x95
2020	S1196	-3858	387.5	15x95
2021	S1197	-3870	507.5	15x95
2022	S1198	-3882	267.5	15x95
2023	S1199	-3894	387.5	15x95
2024	S1200	-3906	507.5	15x95
2025	S1201	-3918	267.5	15x95
2026	S1202	-3930	387.5	15x95
2027	S1203	-3942	507.5	15x95
2028	S1204	-3954	267.5	15x95
2029	S1205	-3966	387.5	15x95
2030	S1206	-3978	507.5	15x95
2031	S1207	-3990	267.5	15x95
2032	S1208	-4002	387.5	15x95
2033	S1209	-4014	507.5	15x95
2034	S1210	-4026	267.5	15x95
2035	S1211	-4038	387.5	15x95
2036	S1212	-4050	507.5	15x95
2037	S1213	-4062	267.5	15x95
2038	S1214	-4074	387.5	15x95
2039	S1215	-4086	507.5	15x95
2040	S1216	-4098	267.5	15x95
2041	S1217	-4110	387.5	15x95
2042	S1218	-4122	507.5	15x95
2043	S1219	-4134	267.5	15x95
2044	S1220	-4146	387.5	15x95
2045	S1221	-4158	507.5	15x95
2046	S1222	-4170	267.5	15x95
2047	S1223	-4182	387.5	15x95
2048	S1224	-4194	507.5	15x95
2049	S1225	-4206	267.5	15x95
2050	S1226	-4218	387.5	15x95

No.	Name	X	Y	Bump size (μm)
2051	S1227	-4230	507.5	15x95
2052	S1228	-4242	267.5	15x95
2053	S1229	-4254	387.5	15x95
2054	S1230	-4266	507.5	15x95
2055	S1231	-4278	267.5	15x95
2056	S1232	-4290	387.5	15x95
2057	S1233	-4302	507.5	15x95
2058	S1234	-4314	267.5	15x95
2059	S1235	-4326	387.5	15x95
2060	S1236	-4338	507.5	15x95
2061	S1237	-4350	267.5	15x95
2062	S1238	-4362	387.5	15x95
2063	S1239	-4374	507.5	15x95
2064	S1240	-4386	267.5	15x95
2065	S1241	-4398	387.5	15x95
2066	S1242	-4410	507.5	15x95
2067	S1243	-4422	267.5	15x95
2068	S1244	-4434	387.5	15x95
2069	S1245	-4446	507.5	15x95
2070	S1246	-4458	267.5	15x95
2071	S1247	-4470	387.5	15x95
2072	S1248	-4482	507.5	15x95
2073	S1249	-4494	267.5	15x95
2074	S1250	-4506	387.5	15x95
2075	S1251	-4518	507.5	15x95
2076	S1252	-4530	267.5	15x95
2077	S1253	-4542	387.5	15x95
2078	S1254	-4554	507.5	15x95
2079	S1255	-4566	267.5	15x95
2080	S1256	-4578	387.5	15x95
2081	S1257	-4590	507.5	15x95
2082	S1258	-4602	267.5	15x95
2083	S1259	-4614	387.5	15x95
2084	S1260	-4626	507.5	15x95
2085	S1261	-4638	267.5	15x95
2086	S1262	-4650	387.5	15x95
2087	S1263	-4662	507.5	15x95
2088	S1264	-4674	267.5	15x95
2089	S1265	-4686	387.5	15x95
2090	S1266	-4698	507.5	15x95
2091	S1267	-4710	267.5	15x95
2092	S1268	-4722	387.5	15x95
2093	S1269	-4734	507.5	15x95
2094	S1270	-4746	267.5	15x95
2095	S1271	-4758	387.5	15x95
2096	S1272	-4770	507.5	15x95
2097	S1273	-4782	267.5	15x95
2098	S1274	-4794	387.5	15x95
2099	S1275	-4806	507.5	15x95
2100	S1276	-4818	267.5	15x95

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No.	Name	X	Y	Bump size (μm)
2101	S1277	-4830	387.5	15x95
2102	S1278	-4842	507.5	15x95
2103	S1279	-4854	267.5	15x95
2104	S1280	-4866	387.5	15x95
2105	S1281	-4878	507.5	15x95
2106	S1282	-4890	267.5	15x95
2107	S1283	-4902	387.5	15x95
2108	S1284	-4914	507.5	15x95
2109	S1285	-4926	267.5	15x95
2110	S1286	-4938	387.5	15x95
2111	S1287	-4950	507.5	15x95
2112	S1288	-4962	267.5	15x95
2113	S1289	-4974	387.5	15x95
2114	S1290	-4986	507.5	15x95
2115	S1291	-4998	267.5	15x95
2116	S1292	-5010	387.5	15x95
2117	S1293	-5022	507.5	15x95
2118	S1294	-5034	267.5	15x95
2119	S1295	-5046	387.5	15x95
2120	S1296	-5058	507.5	15x95
2121	S1297	-5070	267.5	15x95
2122	S1298	-5082	387.5	15x95
2123	S1299	-5094	507.5	15x95
2124	S1300	-5106	267.5	15x95
2125	S1301	-5118	387.5	15x95
2126	S1302	-5130	507.5	15x95
2127	S1303	-5142	267.5	15x95
2128	S1304	-5154	387.5	15x95
2129	S1305	-5166	507.5	15x95
2130	S1306	-5178	267.5	15x95
2131	S1307	-5190	387.5	15x95
2132	S1308	-5202	507.5	15x95
2133	S1309	-5214	267.5	15x95
2134	S1310	-5226	387.5	15x95
2135	S1311	-5238	507.5	15x95
2136	S1312	-5250	267.5	15x95
2137	S1313	-5262	387.5	15x95
2138	S1314	-5274	507.5	15x95
2139	S1315	-5286	267.5	15x95
2140	S1316	-5298	387.5	15x95
2141	S1317	-5310	507.5	15x95
2142	S1318	-5322	267.5	15x95
2143	S1319	-5334	387.5	15x95
2144	S1320	-5346	507.5	15x95
2145	S1321	-5358	267.5	15x95
2146	S1322	-5370	387.5	15x95
2147	S1323	-5382	507.5	15x95
2148	S1324	-5394	267.5	15x95
2149	S1325	-5406	387.5	15x95
2150	S1326	-5418	507.5	15x95

No.	Name	X	Y	Bump size (μm)
2151	S1327	-5430	267.5	15x95
2152	S1328	-5442	387.5	15x95
2153	S1329	-5454	507.5	15x95
2154	S1330	-5466	267.5	15x95
2155	S1331	-5478	387.5	15x95
2156	S1332	-5490	507.5	15x95
2157	S1333	-5502	267.5	15x95
2158	S1334	-5514	387.5	15x95
2159	S1335	-5526	507.5	15x95
2160	S1336	-5538	267.5	15x95
2161	S1337	-5550	387.5	15x95
2162	S1338	-5562	507.5	15x95
2163	S1339	-5574	267.5	15x95
2164	S1340	-5586	387.5	15x95
2165	S1341	-5598	507.5	15x95
2166	S1342	-5610	267.5	15x95
2167	S1343	-5622	387.5	15x95
2168	S1344	-5634	507.5	15x95
2169	S1345	-5646	267.5	15x95
2170	S1346	-5658	387.5	15x95
2171	S1347	-5670	507.5	15x95
2172	S1348	-5682	267.5	15x95
2173	S1349	-5694	387.5	15x95
2174	S1350	-5706	507.5	15x95
2175	S1351	-5718	267.5	15x95
2176	S1352	-5730	387.5	15x95
2177	S1353	-5742	507.5	15x95
2178	S1354	-5754	267.5	15x95
2179	S1355	-5766	387.5	15x95
2180	S1356	-5778	507.5	15x95
2181	S1357	-5790	267.5	15x95
2182	S1358	-5802	387.5	15x95
2183	S1359	-5814	507.5	15x95
2184	S1360	-5826	267.5	15x95
2185	S1361	-5838	387.5	15x95
2186	S1362	-5850	507.5	15x95
2187	S1363	-5862	267.5	15x95
2188	S1364	-5874	387.5	15x95
2189	S1365	-5886	507.5	15x95
2190	S1366	-5898	267.5	15x95
2191	S1367	-5910	387.5	15x95
2192	S1368	-5922	507.5	15x95
2193	S1369	-5934	267.5	15x95
2194	S1370	-5946	387.5	15x95
2195	S1371	-5958	507.5	15x95
2196	S1372	-5970	267.5	15x95
2197	S1373	-5982	387.5	15x95
2198	S1374	-5994	507.5	15x95
2199	S1375	-6006	267.5	15x95
2200	S1376	-6018	387.5	15x95

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No.	Name	X	Y	Bump size (μm)
2201	S1377	-6030	507.5	15x95
2202	S1378	-6042	267.5	15x95
2203	S1379	-6054	387.5	15x95
2204	S1380	-6066	507.5	15x95
2205	S1381	-6078	267.5	15x95
2206	S1382	-6090	387.5	15x95
2207	S1383	-6102	507.5	15x95
2208	S1384	-6114	267.5	15x95
2209	S1385	-6126	387.5	15x95
2210	S1386	-6138	507.5	15x95
2211	S1387	-6150	267.5	15x95
2212	S1388	-6162	387.5	15x95
2213	S1389	-6174	507.5	15x95
2214	S1390	-6186	267.5	15x95
2215	S1391	-6198	387.5	15x95
2216	S1392	-6210	507.5	15x95
2217	S1393	-6222	267.5	15x95
2218	S1394	-6234	387.5	15x95
2219	S1395	-6246	507.5	15x95
2220	S1396	-6258	267.5	15x95
2221	S1397	-6270	387.5	15x95
2222	S1398	-6282	507.5	15x95
2223	S1399	-6294	267.5	15x95
2224	S1400	-6306	387.5	15x95
2225	S1401	-6318	507.5	15x95
2226	S1402	-6330	267.5	15x95
2227	S1403	-6342	387.5	15x95
2228	S1404	-6354	507.5	15x95
2229	S1405	-6366	267.5	15x95
2230	S1406	-6378	387.5	15x95
2231	S1407	-6390	507.5	15x95
2232	S1408	-6402	267.5	15x95
2233	S1409	-6414	387.5	15x95
2234	S1410	-6426	507.5	15x95
2235	S1411	-6438	267.5	15x95
2236	S1412	-6450	387.5	15x95
2237	S1413	-6462	507.5	15x95
2238	S1414	-6474	267.5	15x95
2239	S1415	-6486	387.5	15x95
2240	S1416	-6498	507.5	15x95
2241	S1417	-6510	267.5	15x95
2242	S1418	-6522	387.5	15x95
2243	S1419	-6534	507.5	15x95
2244	S1420	-6546	267.5	15x95
2245	S1421	-6558	387.5	15x95
2246	S1422	-6570	507.5	15x95
2247	S1423	-6582	267.5	15x95
2248	S1424	-6594	387.5	15x95
2249	S1425	-6606	507.5	15x95
2250	S1426	-6618	267.5	15x95

No.	Name	X	Y	Bump size (μm)
2251	S1427	-6630	387.5	15x95
2252	S1428	-6642	507.5	15x95
2253	S1429	-6654	267.5	15x95
2254	S1430	-6666	387.5	15x95
2255	S1431	-6678	507.5	15x95
2256	S1432	-6690	267.5	15x95
2257	S1433	-6702	387.5	15x95
2258	S1434	-6714	507.5	15x95
2259	S1435	-6726	267.5	15x95
2260	S1436	-6738	387.5	15x95
2261	S1437	-6750	507.5	15x95
2262	S1438	-6762	267.5	15x95
2263	S1439	-6774	387.5	15x95
2264	S1440	-6786	507.5	15x95
2265	S1441	-6798	267.5	15x95
2266	S1442	-6810	387.5	15x95
2267	S1443	-6822	507.5	15x95
2268	S1444	-6834	267.5	15x95
2269	S1445	-6846	387.5	15x95
2270	S1446	-6858	507.5	15x95
2271	S1447	-6870	267.5	15x95
2272	S1448	-6882	387.5	15x95
2273	S1449	-6894	507.5	15x95
2274	S1450	-6906	267.5	15x95
2275	S1451	-6918	387.5	15x95
2276	S1452	-6930	507.5	15x95
2277	S1453	-6942	267.5	15x95
2278	S1454	-6954	387.5	15x95
2279	S1455	-6966	507.5	15x95
2280	S1456	-6978	267.5	15x95
2281	S1457	-6990	387.5	15x95
2282	S1458	-7002	507.5	15x95
2283	S1459	-7014	267.5	15x95
2284	S1460	-7026	387.5	15x95
2285	S1461	-7038	507.5	15x95
2286	S1462	-7050	267.5	15x95
2287	S1463	-7062	387.5	15x95
2288	S1464	-7074	507.5	15x95
2289	S1465	-7086	267.5	15x95
2290	S1466	-7098	387.5	15x95
2291	S1467	-7110	507.5	15x95
2292	S1468	-7122	267.5	15x95
2293	S1469	-7134	387.5	15x95
2294	S1470	-7146	507.5	15x95
2295	S1471	-7158	267.5	15x95
2296	S1472	-7170	387.5	15x95
2297	S1473	-7182	507.5	15x95
2298	S1474	-7194	267.5	15x95
2299	S1475	-7206	387.5	15x95
2300	S1476	-7218	507.5	15x95

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No.	Name	X	Y	Bump size (μm)
2301	S1477	-7230	267.5	15x95
2302	S1478	-7242	387.5	15x95
2303	S1479	-7254	507.5	15x95
2304	S1480	-7266	267.5	15x95
2305	S1481	-7278	387.5	15x95
2306	S1482	-7290	507.5	15x95
2307	S1483	-7302	267.5	15x95
2308	S1484	-7314	387.5	15x95
2309	S1485	-7326	507.5	15x95
2310	S1486	-7338	267.5	15x95
2311	S1487	-7350	387.5	15x95
2312	S1488	-7362	507.5	15x95
2313	S1489	-7374	267.5	15x95
2314	S1490	-7386	387.5	15x95
2315	S1491	-7398	507.5	15x95
2316	S1492	-7410	267.5	15x95
2317	S1493	-7422	387.5	15x95
2318	S1494	-7434	507.5	15x95
2319	S1495	-7446	267.5	15x95
2320	S1496	-7458	387.5	15x95
2321	S1497	-7470	507.5	15x95
2322	S1498	-7482	267.5	15x95
2323	S1499	-7494	387.5	15x95
2324	S1500	-7506	507.5	15x95
2325	S1501	-7518	267.5	15x95
2326	S1502	-7530	387.5	15x95
2327	S1503	-7542	507.5	15x95
2328	S1504	-7554	267.5	15x95
2329	S1505	-7566	387.5	15x95
2330	S1506	-7578	507.5	15x95
2331	S1507	-7590	267.5	15x95
2332	S1508	-7602	387.5	15x95
2333	S1509	-7614	507.5	15x95
2334	S1510	-7626	267.5	15x95
2335	S1511	-7638	387.5	15x95
2336	S1512	-7650	507.5	15x95
2337	S1513	-7662	267.5	15x95
2338	S1514	-7674	387.5	15x95
2339	S1515	-7686	507.5	15x95
2340	S1516	-7698	267.5	15x95
2341	S1517	-7710	387.5	15x95
2342	S1518	-7722	507.5	15x95
2343	S1519	-7734	267.5	15x95
2344	S1520	-7746	387.5	15x95
2345	S1521	-7758	507.5	15x95
2346	S1522	-7770	267.5	15x95
2347	S1523	-7782	387.5	15x95
2348	S1524	-7794	507.5	15x95
2349	S1525	-7806	267.5	15x95
2350	S1526	-7818	387.5	15x95

No.	Name	X	Y	Bump size (μm)
2351	S1527	-7830	507.5	15x95
2352	S1528	-7842	267.5	15x95
2353	S1529	-7854	387.5	15x95
2354	S1530	-7866	507.5	15x95
2355	S1531	-7878	267.5	15x95
2356	S1532	-7890	387.5	15x95
2357	S1533	-7902	507.5	15x95
2358	S1534	-7914	267.5	15x95
2359	S1535	-7926	387.5	15x95
2360	S1536	-7938	507.5	15x95
2361	S1537	-7950	267.5	15x95
2362	S1538	-7962	387.5	15x95
2363	S1539	-7974	507.5	15x95
2364	S1540	-7986	267.5	15x95
2365	S1541	-7998	387.5	15x95
2366	S1542	-8010	507.5	15x95
2367	S1543	-8022	267.5	15x95
2368	S1544	-8034	387.5	15x95
2369	S1545	-8046	507.5	15x95
2370	S1546	-8058	267.5	15x95
2371	S1547	-8070	387.5	15x95
2372	S1548	-8082	507.5	15x95
2373	S1549	-8094	267.5	15x95
2374	S1550	-8106	387.5	15x95
2375	S1551	-8118	507.5	15x95
2376	S1552	-8130	267.5	15x95
2377	S1553	-8142	387.5	15x95
2378	S1554	-8154	507.5	15x95
2379	S1555	-8166	267.5	15x95
2380	S1556	-8178	387.5	15x95
2381	S1557	-8190	507.5	15x95
2382	S1558	-8202	267.5	15x95
2383	S1559	-8214	387.5	15x95
2384	S1560	-8226	507.5	15x95
2385	S1561	-8238	267.5	15x95
2386	S1562	-8250	387.5	15x95
2387	S1563	-8262	507.5	15x95
2388	S1564	-8274	267.5	15x95
2389	S1565	-8286	387.5	15x95
2390	S1566	-8298	507.5	15x95
2391	S1567	-8310	267.5	15x95
2392	S1568	-8322	387.5	15x95
2393	S1569	-8334	507.5	15x95
2394	S1570	-8346	267.5	15x95
2395	S1571	-8358	387.5	15x95
2396	S1572	-8370	507.5	15x95
2397	S1573	-8382	267.5	15x95
2398	S1574	-8394	387.5	15x95
2399	S1575	-8406	507.5	15x95
2400	S1576	-8418	267.5	15x95

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No.	Name	X	Y	Bump size (μm)
2401	S1577	-8430	387.5	15x95
2402	S1578	-8442	507.5	15x95
2403	S1579	-8454	267.5	15x95
2404	S1580	-8466	387.5	15x95
2405	S1581	-8478	507.5	15x95
2406	S1582	-8490	267.5	15x95
2407	S1583	-8502	387.5	15x95
2408	S1584	-8514	507.5	15x95
2409	S1585	-8526	267.5	15x95
2410	S1586	-8538	387.5	15x95
2411	S1587	-8550	507.5	15x95
2412	S1588	-8562	267.5	15x95
2413	S1589	-8574	387.5	15x95
2414	S1590	-8586	507.5	15x95
2415	S1591	-8598	267.5	15x95
2416	S1592	-8610	387.5	15x95
2417	S1593	-8622	507.5	15x95
2418	S1594	-8634	267.5	15x95
2419	S1595	-8646	387.5	15x95
2420	S1596	-8658	507.5	15x95
2421	S1597	-8670	267.5	15x95
2422	S1598	-8682	387.5	15x95
2423	S1599	-8694	507.5	15x95
2424	S1600	-8706	267.5	15x95
2425	S1601	-8718	387.5	15x95
2426	S1602	-8730	507.5	15x95
2427	S1603	-8742	267.5	15x95
2428	S1604	-8754	387.5	15x95
2429	S1605	-8766	507.5	15x95
2430	S1606	-8778	267.5	15x95
2431	S1607	-8790	387.5	15x95
2432	S1608	-8802	507.5	15x95
2433	S1609	-8814	267.5	15x95
2434	S1610	-8826	387.5	15x95
2435	S1611	-8838	507.5	15x95
2436	S1612	-8850	267.5	15x95
2437	S1613	-8862	387.5	15x95
2438	S1614	-8874	507.5	15x95
2439	S1615	-8886	267.5	15x95
2440	S1616	-8898	387.5	15x95
2441	S1617	-8910	507.5	15x95
2442	S1618	-8922	267.5	15x95
2443	S1619	-8934	387.5	15x95
2444	S1620	-8946	507.5	15x95
2445	S1621	-8958	267.5	15x95
2446	S1622	-8970	387.5	15x95
2447	S1623	-8982	507.5	15x95
2448	S1624	-8994	267.5	15x95
2449	S1625	-9006	387.5	15x95
2450	S1626	-9018	507.5	15x95

No.	Name	X	Y	Bump size (μm)
2451	S1627	-9030	267.5	15x95
2452	S1628	-9042	387.5	15x95
2453	S1629	-9054	507.5	15x95
2454	S1630	-9066	267.5	15x95
2455	S1631	-9078	387.5	15x95
2456	S1632	-9090	507.5	15x95
2457	S1633	-9102	267.5	15x95
2458	S1634	-9114	387.5	15x95
2459	S1635	-9126	507.5	15x95
2460	S1636	-9138	267.5	15x95
2461	S1637	-9150	387.5	15x95
2462	S1638	-9162	507.5	15x95
2463	S1639	-9174	267.5	15x95
2464	S1640	-9186	387.5	15x95
2465	S1641	-9198	507.5	15x95
2466	S1642	-9210	267.5	15x95
2467	S1643	-9222	387.5	15x95
2468	S1644	-9234	507.5	15x95
2469	S1645	-9246	267.5	15x95
2470	S1646	-9258	387.5	15x95
2471	S1647	-9270	507.5	15x95
2472	S1648	-9282	267.5	15x95
2473	S1649	-9294	387.5	15x95
2474	S1650	-9306	507.5	15x95
2475	S1651	-9318	267.5	15x95
2476	S1652	-9330	387.5	15x95
2477	S1653	-9342	507.5	15x95
2478	S1654	-9354	267.5	15x95
2479	S1655	-9366	387.5	15x95
2480	S1656	-9378	507.5	15x95
2481	S1657	-9390	267.5	15x95
2482	S1658	-9402	387.5	15x95
2483	S1659	-9414	507.5	15x95
2484	S1660	-9426	267.5	15x95
2485	S1661	-9438	387.5	15x95
2486	S1662	-9450	507.5	15x95
2487	S1663	-9462	267.5	15x95
2488	S1664	-9474	387.5	15x95
2489	S1665	-9486	507.5	15x95
2490	S1666	-9498	267.5	15x95
2491	S1667	-9510	387.5	15x95
2492	S1668	-9522	507.5	15x95
2493	S1669	-9534	267.5	15x95
2494	S1670	-9546	387.5	15x95
2495	S1671	-9558	507.5	15x95
2496	S1672	-9570	267.5	15x95
2497	S1673	-9582	387.5	15x95
2498	S1674	-9594	507.5	15x95
2499	S1675	-9606	267.5	15x95
2500	S1676	-9618	387.5	15x95

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No.	Name	X	Y	Bump size (μm)
2501	S1677	-9630	507.5	15x95
2502	S1678	-9642	267.5	15x95
2503	S1679	-9654	387.5	15x95
2504	S1680	-9666	507.5	15x95
2505	S1681	-9678	267.5	15x95
2506	S1682	-9690	387.5	15x95
2507	S1683	-9702	507.5	15x95
2508	S1684	-9714	267.5	15x95
2509	S1685	-9726	387.5	15x95
2510	S1686	-9738	507.5	15x95
2511	S1687	-9750	267.5	15x95
2512	S1688	-9762	387.5	15x95
2513	S1689	-9774	507.5	15x95
2514	S1690	-9786	267.5	15x95
2515	S1691	-9798	387.5	15x95
2516	S1692	-9810	507.5	15x95
2517	S1693	-9822	267.5	15x95
2518	S1694	-9834	387.5	15x95
2519	S1695	-9846	507.5	15x95
2520	S1696	-9858	267.5	15x95
2521	S1697	-9870	387.5	15x95
2522	S1698	-9882	507.5	15x95
2523	S1699	-9894	267.5	15x95
2524	S1700	-9906	387.5	15x95
2525	S1701	-9918	507.5	15x95
2526	S1702	-9930	267.5	15x95
2527	S1703	-9942	387.5	15x95
2528	S1704	-9954	507.5	15x95
2529	S1705	-9966	267.5	15x95
2530	S1706	-9978	387.5	15x95
2531	S1707	-9990	507.5	15x95
2532	S1708	-10002	267.5	15x95
2533	S1709	-10014	387.5	15x95
2534	S1710	-10026	507.5	15x95
2535	S1711	-10038	267.5	15x95
2536	S1712	-10050	387.5	15x95
2537	S1713	-10062	507.5	15x95
2538	S1714	-10074	267.5	15x95
2539	S1715	-10086	387.5	15x95
2540	S1716	-10098	507.5	15x95
2541	S1717	-10110	267.5	15x95
2542	S1718	-10122	387.5	15x95
2543	S1719	-10134	507.5	15x95
2544	S1720	-10146	267.5	15x95
2545	S1721	-10158	387.5	15x95
2546	S1722	-10170	507.5	15x95
2547	S1723	-10182	267.5	15x95
2548	S1724	-10194	387.5	15x95
2549	S1725	-10206	507.5	15x95
2550	S1726	-10218	267.5	15x95

No.	Name	X	Y	Bump size (μm)
2551	S1727	-10230	387.5	15x95
2552	S1728	-10242	507.5	15x95
2553	S1729	-10254	267.5	15x95
2554	S1730	-10266	387.5	15x95
2555	S1731	-10278	507.5	15x95
2556	S1732	-10290	267.5	15x95
2557	S1733	-10302	387.5	15x95
2558	S1734	-10314	507.5	15x95
2559	S1735	-10326	267.5	15x95
2560	S1736	-10338	387.5	15x95
2561	S1737	-10350	507.5	15x95
2562	S1738	-10362	267.5	15x95
2563	S1739	-10374	387.5	15x95
2564	S1740	-10386	507.5	15x95
2565	S1741	-10398	267.5	15x95
2566	S1742	-10410	387.5	15x95
2567	S1743	-10422	507.5	15x95
2568	S1744	-10434	267.5	15x95
2569	S1745	-10446	387.5	15x95
2570	S1746	-10458	507.5	15x95
2571	S1747	-10470	267.5	15x95
2572	S1748	-10482	387.5	15x95
2573	S1749	-10494	507.5	15x95
2574	S1750	-10506	267.5	15x95
2575	S1751	-10518	387.5	15x95
2576	S1752	-10530	507.5	15x95
2577	S1753	-10542	267.5	15x95
2578	S1754	-10554	387.5	15x95
2579	S1755	-10566	507.5	15x95
2580	S1756	-10578	267.5	15x95
2581	S1757	-10590	387.5	15x95
2582	S1758	-10602	507.5	15x95
2583	S1759	-10614	267.5	15x95
2584	S1760	-10626	387.5	15x95
2585	S1761	-10638	507.5	15x95
2586	S1762	-10650	267.5	15x95
2587	S1763	-10662	387.5	15x95
2588	S1764	-10674	507.5	15x95
2589	S1765	-10686	267.5	15x95
2590	S1766	-10698	387.5	15x95
2591	S1767	-10710	507.5	15x95
2592	S1768	-10722	267.5	15x95
2593	S1769	-10734	387.5	15x95
2594	S1770	-10746	507.5	15x95
2595	S1771	-10758	267.5	15x95
2596	S1772	-10770	387.5	15x95
2597	S1773	-10782	507.5	15x95
2598	S1774	-10794	267.5	15x95
2599	S1775	-10806	387.5	15x95
2600	S1776	-10818	507.5	15x95

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No.	Name	X	Y	Bump size (μm)
2601	S1777	-10830	267.5	15x95
2602	S1778	-10842	387.5	15x95
2603	S1779	-10854	507.5	15x95
2604	S1780	-10866	267.5	15x95
2605	S1781	-10878	387.5	15x95
2606	S1782	-10890	507.5	15x95
2607	S1783	-10902	267.5	15x95
2608	S1784	-10914	387.5	15x95
2609	S1785	-10926	507.5	15x95
2610	S1786	-10938	267.5	15x95
2611	S1787	-10950	387.5	15x95
2612	S1788	-10962	507.5	15x95
2613	S1789	-10974	267.5	15x95
2614	S1790	-10986	387.5	15x95
2615	S1791	-10998	507.5	15x95
2616	S1792	-11010	267.5	15x95
2617	S1793	-11022	387.5	15x95
2618	S1794	-11034	507.5	15x95
2619	S1795	-11046	267.5	15x95
2620	S1796	-11058	387.5	15x95
2621	S1797	-11070	507.5	15x95
2622	S1798	-11082	267.5	15x95
2623	S1799	-11094	387.5	15x95
2624	S1800	-11106	507.5	15x95
2625	S1801	-11118	267.5	15x95
2626	S1802	-11130	387.5	15x95
2627	S1803	-11142	507.5	15x95
2628	S1804	-11154	267.5	15x95
2629	S1805	-11166	387.5	15x95
2630	S1806	-11178	507.5	15x95
2631	S1807	-11190	267.5	15x95
2632	S1808	-11202	387.5	15x95
2633	S1809	-11214	507.5	15x95
2634	S1810	-11226	267.5	15x95
2635	S1811	-11238	387.5	15x95
2636	S1812	-11250	507.5	15x95
2637	S1813	-11262	267.5	15x95
2638	S1814	-11274	387.5	15x95
2639	S1815	-11286	507.5	15x95
2640	S1816	-11298	267.5	15x95
2641	S1817	-11310	387.5	15x95
2642	S1818	-11322	507.5	15x95
2643	S1819	-11334	267.5	15x95
2644	S1820	-11346	387.5	15x95
2645	S1821	-11358	507.5	15x95
2646	S1822	-11370	267.5	15x95
2647	S1823	-11382	387.5	15x95
2648	S1824	-11394	507.5	15x95
2649	S1825	-11406	267.5	15x95
2650	S1826	-11418	387.5	15x95

No.	Name	X	Y	Bump size (μm)
2651	S1827	-11430	507.5	15x95
2652	S1828	-11442	267.5	15x95
2653	S1829	-11454	387.5	15x95
2654	S1830	-11466	507.5	15x95
2655	S1831	-11478	267.5	15x95
2656	S1832	-11490	387.5	15x95
2657	S1833	-11502	507.5	15x95
2658	S1834	-11514	267.5	15x95
2659	S1835	-11526	387.5	15x95
2660	S1836	-11538	507.5	15x95
2661	S1837	-11550	267.5	15x95
2662	S1838	-11562	387.5	15x95
2663	S1839	-11574	507.5	15x95
2664	S1840	-11586	267.5	15x95
2665	S1841	-11598	387.5	15x95
2666	S1842	-11610	507.5	15x95
2667	S1843	-11622	267.5	15x95
2668	S1844	-11634	387.5	15x95
2669	S1845	-11646	507.5	15x95
2670	S1846	-11658	267.5	15x95
2671	S1847	-11670	387.5	15x95
2672	S1848	-11682	507.5	15x95
2673	S1849	-11694	267.5	15x95
2674	S1850	-11706	387.5	15x95
2675	S1851	-11718	507.5	15x95
2676	S1852	-11730	267.5	15x95
2677	S1853	-11742	387.5	15x95
2678	S1854	-11754	507.5	15x95
2679	S1855	-11766	267.5	15x95
2680	S1856	-11778	387.5	15x95
2681	S1857	-11790	507.5	15x95
2682	S1858	-11802	267.5	15x95
2683	S1859	-11814	387.5	15x95
2684	S1860	-11826	507.5	15x95
2685	S1861	-11838	267.5	15x95
2686	S1862	-11850	387.5	15x95
2687	S1863	-11862	507.5	15x95
2688	S1864	-11874	267.5	15x95
2689	S1865	-11886	387.5	15x95
2690	S1866	-11898	507.5	15x95
2691	S1867	-11910	267.5	15x95
2692	S1868	-11922	387.5	15x95
2693	S1869	-11934	507.5	15x95
2694	S1870	-11946	267.5	15x95
2695	S1871	-11958	387.5	15x95
2696	S1872	-11970	507.5	15x95
2697	S1873	-11982	267.5	15x95
2698	S1874	-11994	387.5	15x95
2699	S1875	-12006	507.5	15x95
2700	S1876	-12018	267.5	15x95

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No.	Name	X	Y	Bump size (μm)
2701	S1877	-12030	387.5	15x95
2702	S1878	-12042	507.5	15x95
2703	S1879	-12054	267.5	15x95
2704	S1880	-12066	387.5	15x95
2705	S1881	-12078	507.5	15x95
2706	S1882	-12090	267.5	15x95
2707	S1883	-12102	387.5	15x95
2708	S1884	-12114	507.5	15x95
2709	S1885	-12126	267.5	15x95
2710	S1886	-12138	387.5	15x95
2711	S1887	-12150	507.5	15x95
2712	S1888	-12162	267.5	15x95
2713	S1889	-12174	387.5	15x95
2714	S1890	-12186	507.5	15x95
2715	S1891	-12198	267.5	15x95
2716	S1892	-12210	387.5	15x95
2717	S1893	-12222	507.5	15x95
2718	S1894	-12234	267.5	15x95
2719	S1895	-12246	387.5	15x95
2720	S1896	-12258	507.5	15x95
2721	S1897	-12270	267.5	15x95
2722	S1898	-12282	387.5	15x95
2723	S1899	-12294	507.5	15x95
2724	S1900	-12306	267.5	15x95
2725	S1901	-12318	387.5	15x95
2726	S1902	-12330	507.5	15x95
2727	S1903	-12342	267.5	15x95
2728	S1904	-12354	387.5	15x95
2729	S1905	-12366	507.5	15x95
2730	S1906	-12378	267.5	15x95
2731	S1907	-12390	387.5	15x95
2732	S1908	-12402	507.5	15x95
2733	S1909	-12414	267.5	15x95
2734	S1910	-12426	387.5	15x95
2735	S1911	-12438	507.5	15x95
2736	S1912	-12450	267.5	15x95
2737	S1913	-12462	387.5	15x95
2738	S1914	-12474	507.5	15x95
2739	S1915	-12486	267.5	15x95
2740	S1916	-12498	387.5	15x95
2741	S1917	-12510	507.5	15x95
2742	S1918	-12522	267.5	15x95
2743	S1919	-12534	387.5	15x95
2744	S1920	-12546	507.5	15x95
2745	SZ2	-12558	267.5	15x95
2746	SZ3	-12570	387.5	15x95
2747	DUMMY	-12582	507.5	15x95
2748	VSSA	-12594	267.5	15x95
2749	VSSA	-12606	387.5	15x95
2750	VSSA	-12618	507.5	15x95

No.	Name	X	Y	Bump size (μm)
2751	VCOM_R	-12630	267.5	15x95
2752	VCOM_R	-12642	387.5	15x95
2753	VCOM_R	-12654	507.5	15x95
2754	VCOM_R	-12666	267.5	15x95
2755	VCOM_R	-12678	387.5	15x95
2756	VCOM_R	-12690	507.5	15x95
2757	VSSA	-12702	267.5	15x95
2758	VSSA	-12714	387.5	15x95
2759	VSSA	-12726	507.5	15x95
2760	DUMMY	-12738	267.5	15x95
2761	DUMMY	-12750	387.5	15x95
2762	DUMMY	-12762	507.5	15x95
2763	DUMMY	-12774	267.5	15x95
2764	DUMMY	-12786	387.5	15x95
2765	DUMMY	-12798	507.5	15x95
2766	SWR3B	-12810	267.5	15x95
2767	SWR3B	-12822	387.5	15x95
2768	SWR3B	-12834	507.5	15x95
2769	SWR3	-12846	267.5	15x95
2770	SWR3	-12858	387.5	15x95
2771	SWR3	-12870	507.5	15x95
2772	SWR2B	-12882	267.5	15x95
2773	SWR2B	-12894	387.5	15x95
2774	SWR2B	-12906	507.5	15x95
2775	SWR2	-12918	267.5	15x95
2776	SWR2	-12930	387.5	15x95
2777	SWR2	-12942	507.5	15x95
2778	SWR1B	-12954	267.5	15x95
2779	SWR1B	-12966	387.5	15x95
2780	SWR1B	-12978	507.5	15x95
2781	SWR1	-12990	267.5	15x95
2782	SWR1	-13002	387.5	15x95
2783	SWR1	-13014	507.5	15x95
2784	GOUTR20	-13026	267.5	15x95
2785	GOUTR20	-13038	387.5	15x95
2786	GOUTR20	-13050	507.5	15x95
2787	GOUTR19	-13062	267.5	15x95
2788	GOUTR19	-13074	387.5	15x95
2789	GOUTR19	-13086	507.5	15x95
2790	GOUTR18	-13098	267.5	15x95
2791	GOUTR18	-13110	387.5	15x95
2792	GOUTR18	-13122	507.5	15x95
2793	GOUTR17	-13134	267.5	15x95
2794	GOUTR17	-13146	387.5	15x95
2795	GOUTR17	-13158	507.5	15x95
2796	GOUTR16	-13170	267.5	15x95
2797	GOUTR16	-13182	387.5	15x95
2798	GOUTR16	-13194	507.5	15x95
2799	GOUTR15	-13206	267.5	15x95
2800	GOUTR15	-13218	387.5	15x95

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No.	Name	X	Y	Bump size (μm)
2801	GOUTR15	-13230	507.5	15x95
2802	GOUTR14	-13242	267.5	15x95
2803	GOUTR14	-13254	387.5	15x95
2804	GOUTR14	-13266	507.5	15x95
2805	VGH2	-13278	267.5	15x95
2806	VGH2	-13290	387.5	15x95
2807	VGH2	-13302	507.5	15x95
2808	VGH2	-13314	267.5	15x95
2809	VGH2	-13326	387.5	15x95
2810	VGH2	-13338	507.5	15x95
2811	GOUTR13	-13350	267.5	15x95
2812	GOUTR13	-13362	387.5	15x95
2813	GOUTR13	-13374	507.5	15x95
2814	GOUTR12	-13386	267.5	15x95
2815	GOUTR12	-13398	387.5	15x95
2816	GOUTR12	-13410	507.5	15x95
2817	GOUTR11	-13422	267.5	15x95
2818	GOUTR11	-13434	387.5	15x95
2819	GOUTR11	-13446	507.5	15x95
2820	GOUTR10	-13458	267.5	15x95
2821	GOUTR10	-13470	387.5	15x95
2822	GOUTR10	-13482	507.5	15x95
2823	GOUTR9	-13494	267.5	15x95
2824	GOUTR9	-13506	387.5	15x95
2825	GOUTR9	-13518	507.5	15x95
2826	GOUTR8	-13530	267.5	15x95
2827	GOUTR8	-13542	387.5	15x95
2828	GOUTR8	-13554	507.5	15x95
2829	GOUTR7	-13566	267.5	15x95
2830	GOUTR7	-13578	387.5	15x95
2831	GOUTR7	-13590	507.5	15x95
2832	VGL	-13602	267.5	15x95
2833	VGL	-13614	387.5	15x95
2834	VGL	-13626	507.5	15x95
2835	VGL	-13638	267.5	15x95
2836	VGL	-13650	387.5	15x95
2837	VGL	-13662	507.5	15x95
2838	GOUTR6	-13674	267.5	15x95
2839	GOUTR6	-13686	387.5	15x95
2840	GOUTR6	-13698	507.5	15x95
2841	GOUTR5	-13710	267.5	15x95
2842	GOUTR5	-13722	387.5	15x95
2843	GOUTR5	-13734	507.5	15x95
2844	GOUTR4	-13746	267.5	15x95
2845	GOUTR4	-13758	387.5	15x95
2846	GOUTR4	-13770	507.5	15x95
2847	GOUTR3	-13782	267.5	15x95
2848	GOUTR3	-13794	387.5	15x95
2849	GOUTR3	-13806	507.5	15x95
2850	GOUTR2	-13818	267.5	15x95

No.	Name	X	Y	Bump size (μm)
2851	GOUTR2	-13830	387.5	15x95
2852	GOUTR2	-13842	507.5	15x95
2853	GOUTR1	-13854	267.5	15x95
2854	GOUTR1	-13866	387.5	15x95
2855	GOUTR1	-13878	507.5	15x95
2856	GDETR	-13890	267.5	15x95
2857	GDETR	-13902	387.5	15x95
2858	GDETR	-13914	507.5	15x95
2859	FCTRL_R	-14145	485	110x30
2860	CA_R[0]	-14145	430	110x30
2861	GIO_R[0]	-14145	375	110x30
2862	CA_R[1]	-14145	320	110x30
2863	GIO_R[1]	-14145	265	110x30
2864	CA_R[2]	-14145	210	110x30
2865	GIO_R[2]	-14145	155	110x30
2866	CA3	-14145	100	110x30
2867	GIO_R[3]	-14145	45	110x30
2868	GIO_R[4]	-14145	-10	110x30
2869	CA_R[4]	-14145	-65	110x30
2870	DUMMY	-13800	-101.25	50x50
2871	CA_R[5]	-14145	-120	110x30
2872	CA6	-14145	-175	110x30
2873	CA_R[7]	-14145	-230	110x30
2874	CA_R[8]	-14145	-285	110x30
2875	CA_R[9]	-14145	-340	110x30
2876	F_POL_RO	-14145	-395	110x30

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11. Ordering Information

Part no.	Package
HX82102-A00DPDxxxy-LTP	00: mean chip version D: mean fab code PD: mean COG xxx: mean chip thickness **(μm)** y: mean value of bump compensation LT: mean low temperature P: mean polish

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