# PRODUCT SPECIFICATION

**CDTECH Model:** **S080BWX25NP**

**CUSTOMER Model:** -

**Description:** **8.0” TFT-LCD Module**

**Version:** **1.0**

| CDTECH | PREPARED BY | CHECKED BY | APPROVED BY |
|---|---|---|---|
| SIGNATURE | | | |
| DATE | 2022.12.2 | 2022.12.2 | 2022.12.2 |

| CUSTOMER APPROVAL | SIGNATURE | DATE |
|---|---|---|
| | | |

## Record of Revisions

| Version | Revise Date | Description | Page |
|---|---|---|---|
| 1.0 | 2022-12-02 | First Release | - |
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# Contents

# 1. General Specifications

## 1.1 LCM General Information

| Item | Specification | Unit |
|---|---|---|
| LCD Size | 8.0 | inch |
| Number of Pixels | 800 (H) RGB x 1280 (V) | pixels |
| Display Mode | Normally Black | - |
| Viewing Direction | Free | o' clock |
| Interface | MIPI | - |
| Display Colors | 16.7M | colors |
| Outline Dimension | 114.60 (H) x 184.10 (V) x 2.65 (D) | mm |
| Active Area | 107.64 (H) x 172.22 (V) | mm |
| Pixel Pitch | 0.1345 (H) x 0.1345 (V) | mm |
| Driver IC | ILI9881C | - |
| Operation Temperature | 0~50 | ℃ |
| Storage Temperature | -10~60 | ℃ |

Note1:Requirements on environmental protection RoHS compliant.

# 2. Absolute Maximum Ratings

| Item | Symbol | MIN. | MAX. | Unit | Note |
|---|---|---|---|---|---|
| Analog Supply voltage | VCI | -0.3 | 5.0 | V | Note 1 |
| Digital supply voltage | IOVCC | -0.3 | 3.6 | V | Note 1 |

Note 1:Permanent damage may occur to the LCD module if beyond this specification.
Functional operation should be restricted to the conditions described under normal operating conditions.

# 3. Elecrical Characteristics

### 3.1 Recommended Operating Condition for TFT LCD

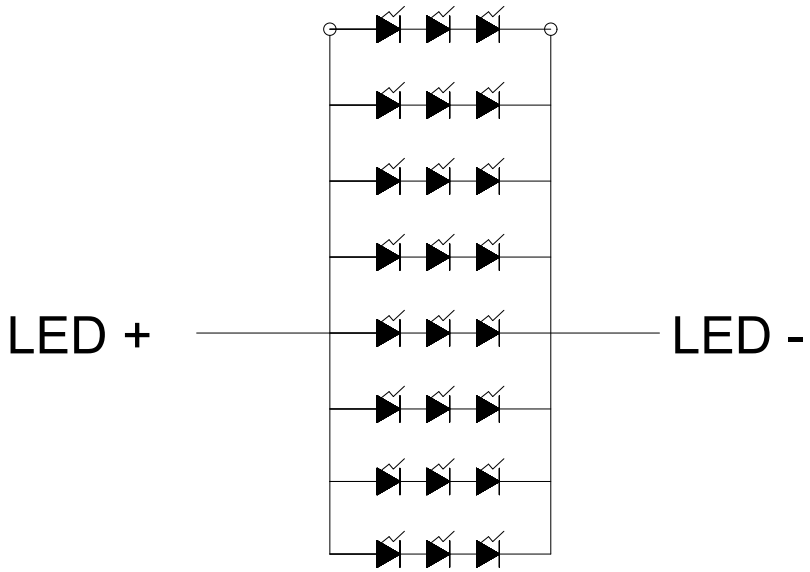
| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Analog Supply voltage | VCI | 3.0 | 3.3 | 3.6 | V | |
| Analog supply current | $I_{VCI}$ | - | TBD | - | mA | VCI=3.3V |
| Logic supply voltage | IOVCC | 1.65 | 1.8 | 3.3 | V | |
| Logic supply current | $I_{IOVCC}$ | - | TBD | - | mA | IOVCC=1.8V |
| Logic input voltage | VIH | 0.7*IOVCC | - | IOVCC | V | |
| | VIL | GND | - | 0.3*IOVCC | V | |

### 3.2 Recommended Driving Condition for Backlight

| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Driving Current | $I_F$ | - | 160 | - | mA | |
| Driving Voltage | $V_F$ | 8.1 | - | 10.2 | V | |
| Power consumption | $W_{BL}$ | 1.296 | - | 1.632 | W | |
| LED Life-Time | N/A | 30,000 | - | - | Hours | Ta=25℃<br>Note 1 |

Note 1:LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :



# 4. Interface Pin Assignment

## 4.1 LCM Pin Assignment

| No. | Symbol | Description |
|---|---|---|
| 1 | LEDA | Power for LED backlight (Anode) |
| 2 | LEDA | Power for LED backlight (Anode) |
| 3 | LEDA | Power for LED backlight (Anode) |
| 4 | NC | No connection |
| 5 | LEDK | Power for LED backlight (Cathode) |
| 6 | LEDK | Power for LED backlight (Cathode) |
| 7 | LEDK | Power for LED backlight (Cathode) |
| 8 | LEDK | Power for LED backlight (Cathode) |
| 9 | GND | Ground |
| 10 | GND | Ground |
| 11 | D2P | MIPI Positive data signal(+) |
| 12 | D2N | MIPI Negative data signal(-) |
| 13 | GND | Ground |
| 14 | D1P | MIPI Positive data signal(+) |
| 15 | D1N | MIPI Negative data signal(-) |
| 16 | GND | Ground |
| 17 | CLKP | MIPI Positive clock signal(+) |
| 18 | CLKN | MIPI Negative clock signal(-) |
| 19 | GND | Ground |
| 20 | D0P | MIPI Positive data signal(+) |
| 21 | D0N | MIPI Negative data signal(-) |
| 22 | GND | Ground |
| 23 | D3P | MIPI Positive data signal(+) |
| 24 | D3N | MIPI Negative data signal(-) |
| 25 | GND | Ground |
| 26 | NC | No connection |
| 27 | RESET | Global reset pin |
| 28 | NC | No connection |
| 29 | IOVCC(1.8V) | Power supply(1.8V) |
| 30 | VCI(3.3V) | Power supply(3.3V) |
| 31 | VCI(3.3V) | Power supply(3.3V) |

# 5. Interface Characteristics

## 5.1 Interface Timing

5.1.1 High Speed Mode

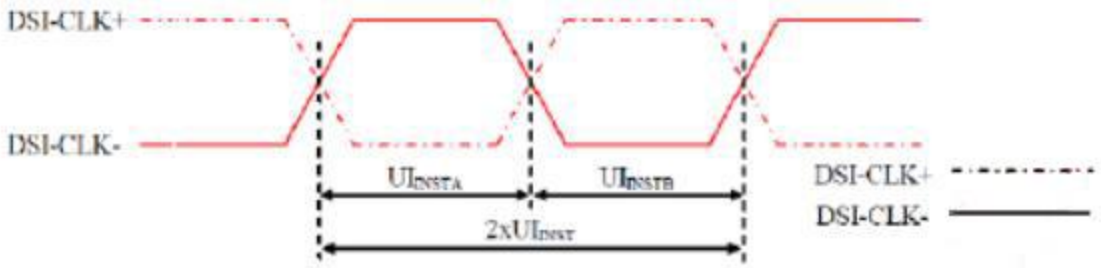
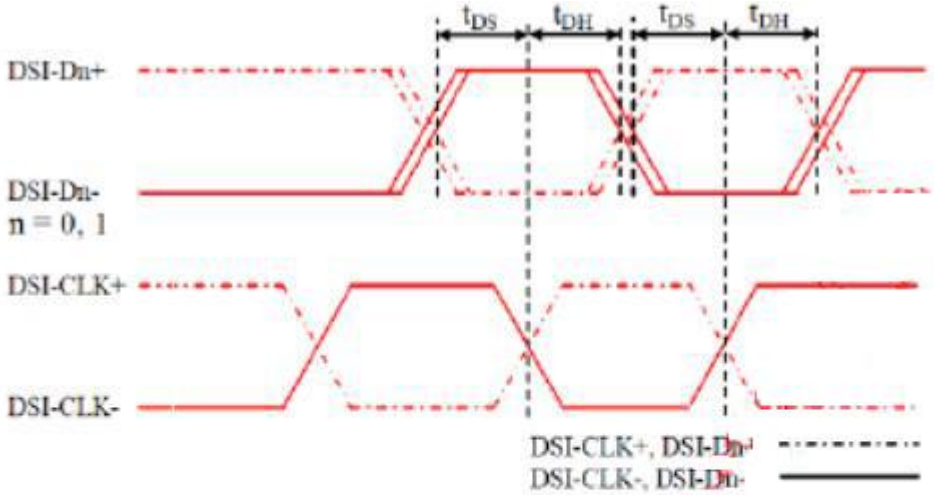



Figure 4: DSI Clock Channel Timing

DSI Clock Channel Timing

| Signal | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| CLKP/N | 2xUIINST | Double UI instantaneous | TBD | TBD | ns |
| CLKP/N | UIINSTA, UIINSTB (Note 1) | UI instantaneous Half | TBD (Note 2) | TBD | ns |

5.1.2 High Speed Mode – Data Clock Channel Timing

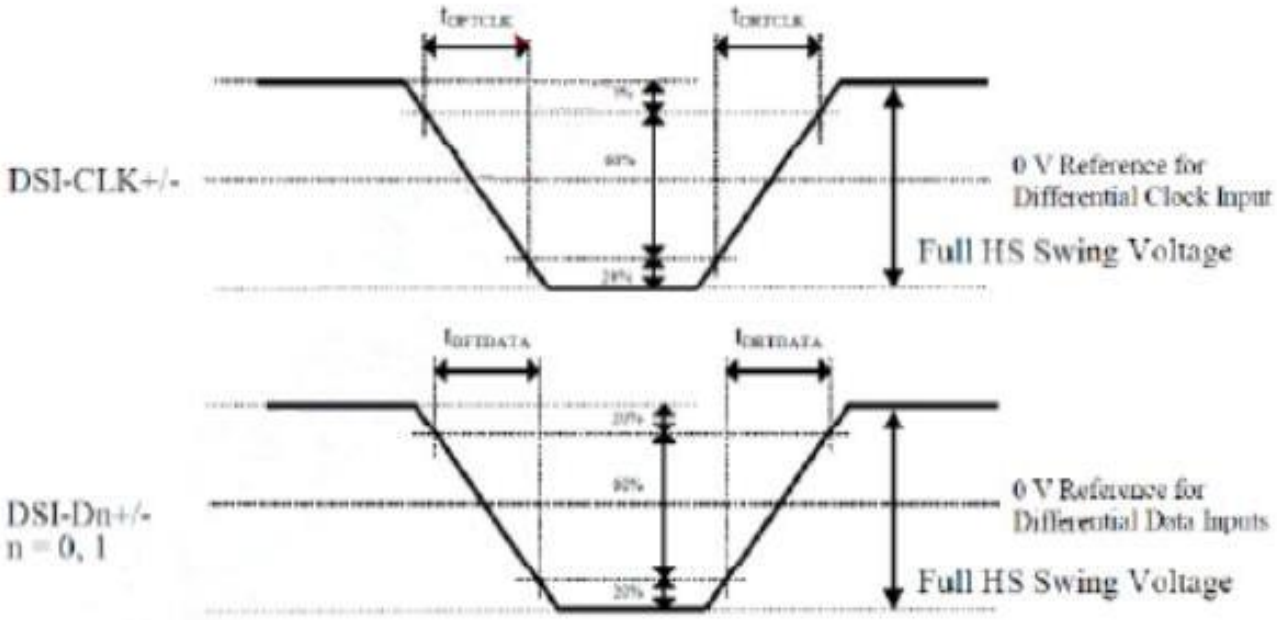



DSI Data to Clock Channel Timings

DSI Data to Clock Channel Timings

| Signal | Symbol | Parameter | Min | Max |
|---|---|---|---|---|
| DnP/N , n=0 and 1 | tDS | Data to Clock Setup time | TBD | - |
| | tDH | Clock to Data Hold Time | TBD | - |

5.1.3 High Speed Mode – Rising and Falling Timings




**Rising and Falling Timings on Clock and Data Channels**

**Rise and Fall Timings on Clock and Data Channels**

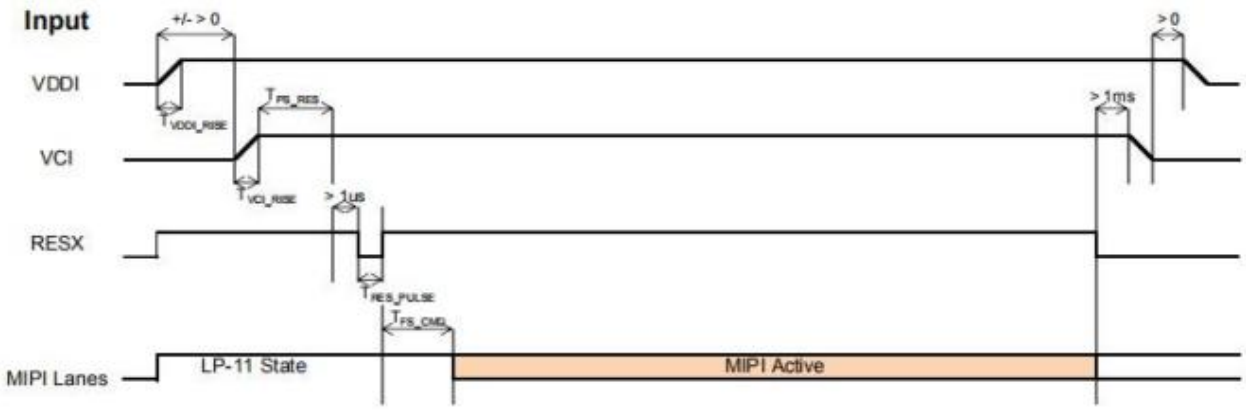
| Parameter | Symbol | Condition | Specification | | |
|---|---|---|---|---|---|
| | | | Min | Typ | Max |
| Differential Rise Time for Clock | $t_{DRTCLK}$ | CLKP/N | TBD | - | TBD (Note) |
| Differential Rise Time for Data | $t_{DRTDATA}$ | DnP/N n=0 and 1 | TBD | - | TBD (Note) |
| Differential Fall Time for Clock | $t_{DFTCLK}$ | CLKP/N | TBD | - | TBD (Note) |
| Differential Fall Time for Data | $t_{DFTDATA}$ | DnP/N n=0 and 1 | TBD | - | TBD (Note) |

**Note:** The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

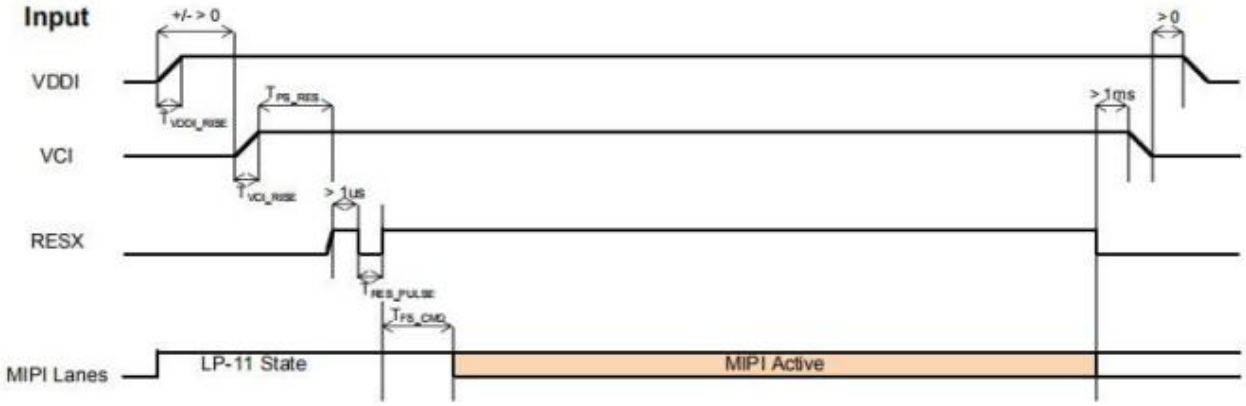
## 5.2 Power On/Off Sequence

To prevent the device damage from latch up and Improve subjective display effect,the power ON/OFF sequence shown below must be followed.

**Case A:**




**Case B:**




| Symbol | Characteristics | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $T_{VDDI\_RISE}$ | VDDI Rise time | 10 | - | - | us |
| $T_{VCI\_RISE}$ | Case A: VCI Rise time | 130 | - | - | us |
| | Case B: VCI Rise time | 40 | | | |
| $T_{PS\_RES}$ | VDDI/VCI on to Reset high | 5 | - | - | ms |
| $T_{RES\_PULSE}$ | Reset low pulse time | 10 | - | - | us |
| $T_{FS\_CMD}$ | Reset to first command | 10 | - | - | ms |

**Figure 93: Power on/off sequence with Power Mode 3**

## 5.3 Reset Timing Characteristics

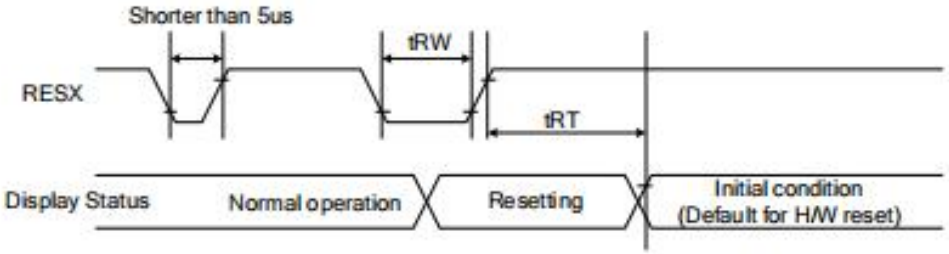



**Figure 124: Reset Timing**

**Table 47: Reset Timing**

| Signal | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| RESX | tRW | Reset pulse duration | 10 | | uS |
| | tRT | Reset cancel | | 5 (note 1,5) | mS |
| | | | | 120 (note 1,6,7) | mS |

***Notes:***

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

**Table 48: Reset Descript**

| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 10us | Reset |
| Between 5us and 10us | Reset starts |

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

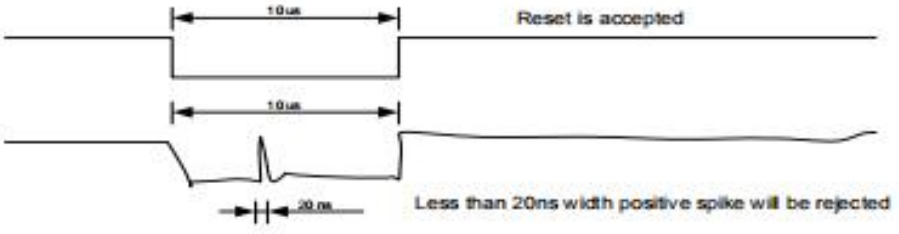
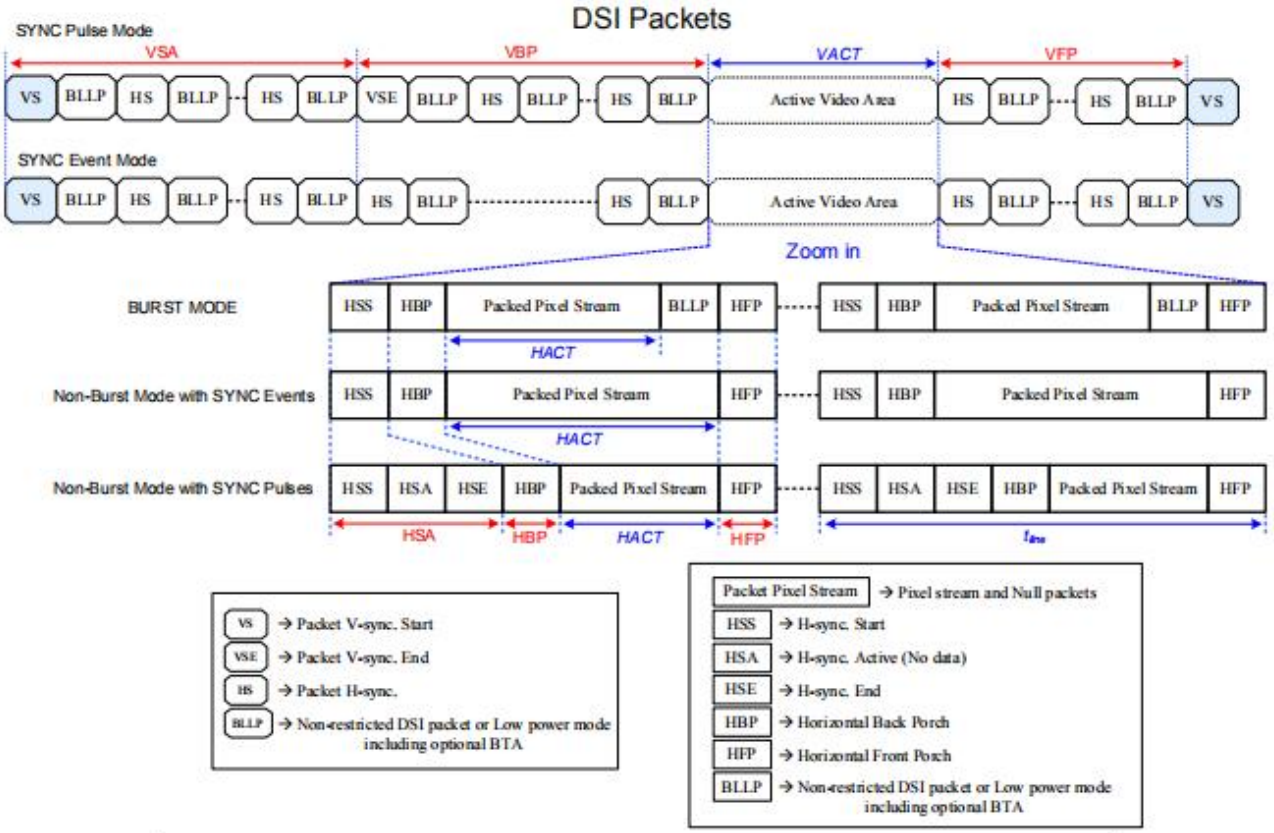



**Figure 125: Positive Noise Pulse during Reset Low**

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

## 5.4 Timing for DSI Video Mode




| Parameters | Symbols | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Vertical sync. active | VSA | 2 (Note 6) | - | - | Line |
| Vertical Back Porch | VBP | 14 (Note 6) | - | - | Line |
| Vertical Front Porch | VFP | 8 (Note 6) | - | - | Line |
| Active lines per frame | VACT | - | 1280 | - | Line |
| Horizontal sync. active | HSA | 2 | - | - | Pixel |
| Horizontal Porch period | HSA + HBP + HFP | 1.6 | - | - | us |
| Active pixels per line | HACT | - | 720 | - | Pixel |
| Bit rate | $BR_{bps}$ | 385 | | Note 5 | Mbps/lane |

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number ) / (UI* pixel format )

HBP(pixel)= (tHBP*lane number ) / (UI* pixel format )

HFP(pixel)= (tHFP*lane number ) / (UI* pixel format )

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

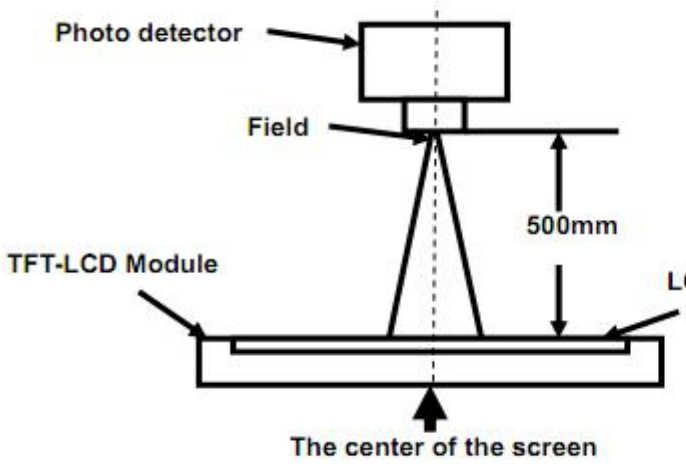
Example : $BR_{bps}$ = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

# 6. Optical Specifications

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Viewing Angle (CR≥10) B/L ON | $\theta_T$ | Φ=90°(12 o'clock) | - | 80 | - | deg | Note2 |
| | $\theta_B$ | Φ=270°(6 o'clock) | - | 80 | - | deg | Note2 |
| | $\theta_L$ | Φ=180°(9 o'clock) | - | 80 | - | deg | Note2 |
| | $\theta_R$ | Φ=0°(3 o'clock) | - | 80 | - | deg | Note2 |
| Response Time | $T_{ON}$ | Normal θ=Φ=0° | - | - | 17 | msec | Note4 |
| | $T_{OFF}$ | | - | - | 17 | msec | Note4 |
| Contrast Ratio | CR | | 900 | 1200 | - | - | Note1 Note3 |
| Color Chromaticity | $W_X$ | | 0.256 | 0.306 | 0.356 | - | Note1 Note5 |
| | $W_Y$ | | 0.310 | 0.360 | 0.410 | - | Note1 Note5 |
| Luminance | L | | 300 | 400 | - | cd/m² | Note1 Note7 |
| Luminance Uniformity | $Y_U$ | | 75 | 80 | - | % | Note1 Note6 |
| NTSC | - | | - | 60 | - | % | - |

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.




| Item | Photo detector | Field |
|---|---|---|
| Contrast Ratio | SR-3A | 1° |
| Luminance | | |
| Chromaticity | | |
| Lum Uniformity | | |
| Response Time | BM-7A | 2° |

Note 2:Definition of viewing angle range and measurement system
Viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

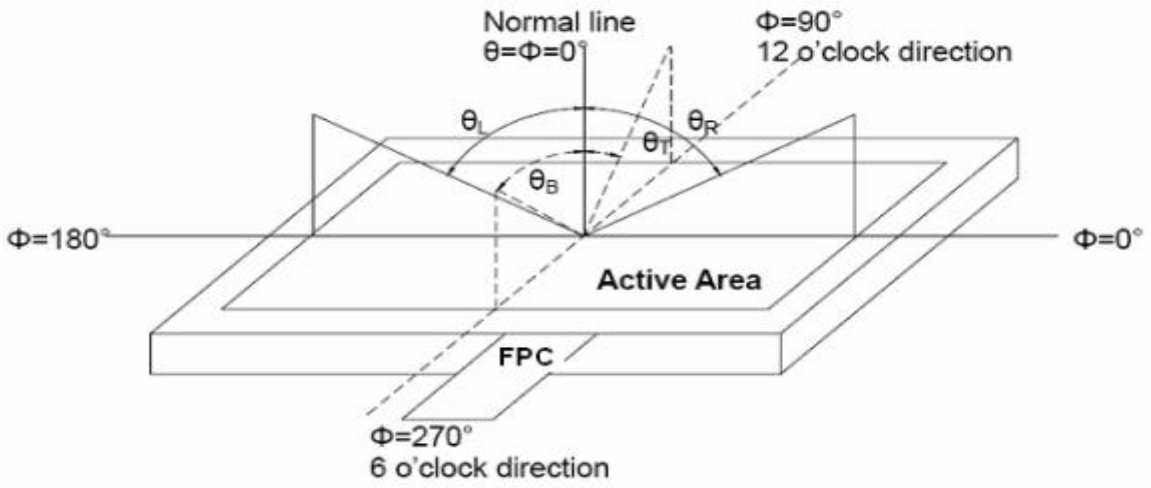


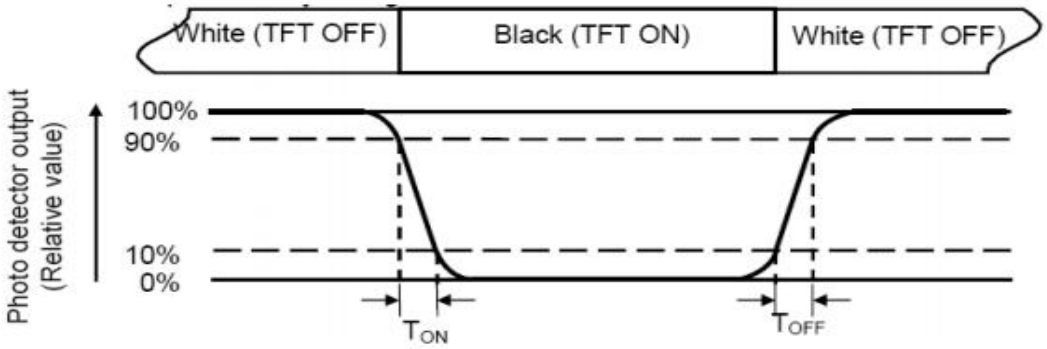

Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.




Note 5:Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6:Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

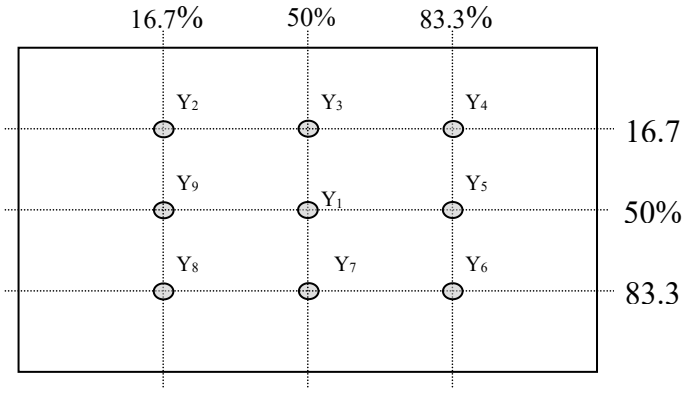



Fig. 2 Definition of points

Note 7:Definition of Luminance (Refer Fig. 2)

Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ......,Pn).

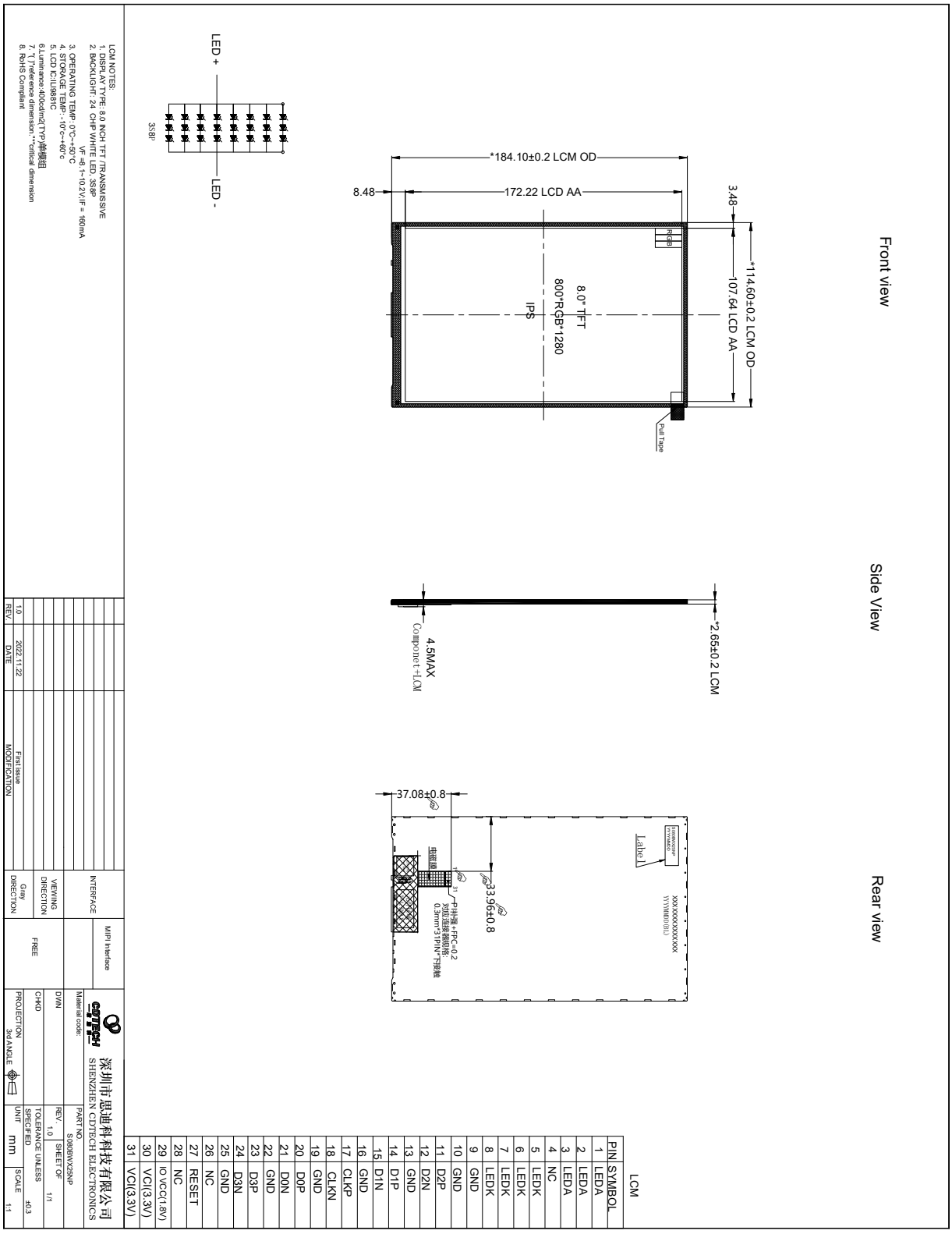
# 7. Reliability Test Items

| Test Item | Test Conditions | |
|---|---|---|
| High Temperature Storage | Ta= +60℃ | 96hrs |
| Low Temperature Storage | Ta= -10℃ | 96hrs |
| High Temperature Operation | Ta= +50℃ | 96hrs |
| Low Temperature Operation | Ta= 0℃ | 96hrs |
| High Temperature and Humidity Storage | Ta= +60℃, 90% RH | 96hrs |
| Thermal Shock (Non-operation) | -10℃/30 min ~ +60℃/30 min for 20 cycles<br>Start with cold temperature<br>end with high temperature | |
| Electro Static Discharge | Contact = ± 4 kV, class B<br>Air = ± 8 kV, class B<br>R=330Ω,C=150pF | |
| Vibration | Sweep: 10Hz~55Hz~10Hz<br>Stroke: 1.5mm<br>2 hrs for each direction of X .Y. Z. | |
| Mechanical Shock | 60G 6ms,±X,±Y,±Z<br>3 times for each direction | |
| Package Drop Test | Height: 60 cm<br>1 corner, 3 edges, 6 surfaces | |

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

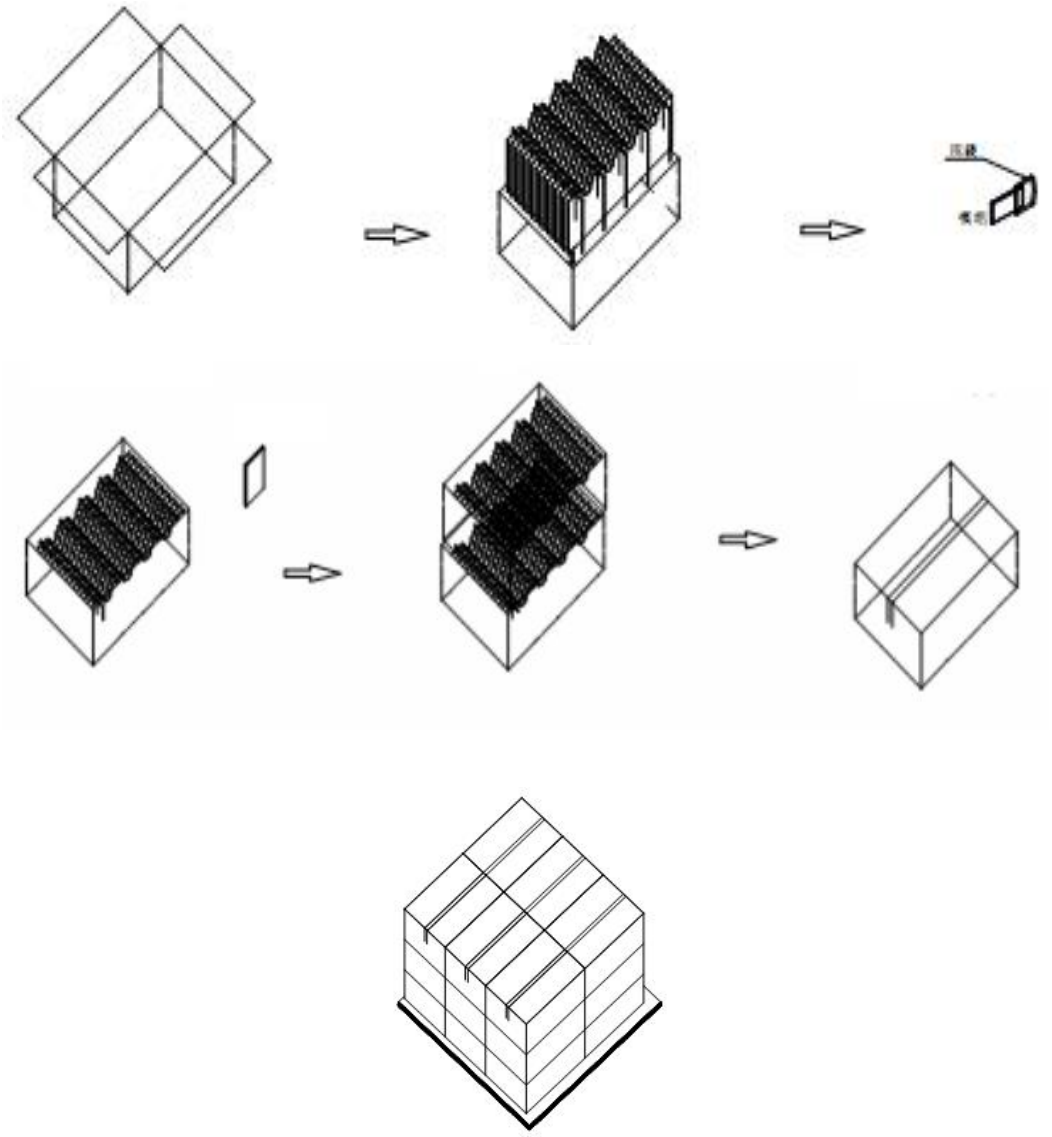
1). Air bubble in the LCD
2). Seal leak or Glass crack
3). Non display or abnormal display
4). Brightness reduction >50%

# 8. Mechanical Drawing



# 9. Packing

**Packing Method**



Steps:
1. Put module into tray cavity
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above
4. Fix the cardboard to the tray stack with adhesive tape
5. Put the tray stack into carton
6. Carton sealing with adhesive tape

# 10. Precautions for Use of LCD modules

## 10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

## 10.2 Storage Precautions

10.2.1.When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2.The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time,the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3.The LCD modules should be stored in the room without acid, alkali and harmful gas.

## 10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.