PRODUCT SPECIFICATION

CDTECH Model: **S024HQ42NN-DC21**

CUSTOMER Model: -

Description: **2.4 ” TFT-LCD Module with CTP**

Version: **2.0**

CDTECH	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2023.4.14	2023.4.14	2023.4.14

	SIGNATURE	DATE
CUSTOMER APPROVAL		

Record of Revisions

Version	Revise Date	Description	Page
2.0	2023-4-14	First Release	-

Contents

1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	2.4	inch
Number of Pixels	240 (H) RGB x 320 (V)	pixels
Display Mode	Normally Black	-
Viewing Direction	Free	o' clock
Interface	MCU	-
Display Colors	16.7M	colors
Outline Dimension	47.79 (H) x 69.96 (V) x 4.05 (D)	mm
Active Area	36.72 (H) x 48.96 (V)	mm
Pixel Pitch	0.153 (H) x 0.153 (V)	mm
Driver IC	ILI9340X	-
Operation Temperature	-20~70	℃
Storage Temperature	-30~80	℃

1.2 Touch Panel Information

Item	Specification
Touch Structure	G+G
Bonding Type with LCM	Perimeter Bonding
Driver IC	HX8571-E27
Interface	I²C
Touch Count Max	5 Points
Surface treatment	-
Surface hardness	6H
I2C slave address	0x48
Origin of coordinate	Top Left Corner

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Analog Supply voltage	VDD	-0.3	5.0	V	Note 1
Digital supply voltage	IOVCC	-0.3	3.6	V	Note 1

Note 1:Permanent damage may occur to the LCD module if beyond this specification.
Functional operation should be restricted to the conditions described under normal operating conditions.

3. Elecrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

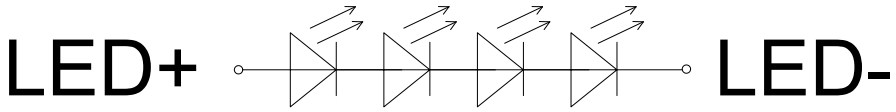
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Supply voltage	VCI	2.5	2.8	3.3	V	
Analog supply current	I_{VCI}	-	TBD	-	mA	VDD=2.8V
Logic supply voltage	IOVCC	1.65	1.8	3.3	V	
Logic supply current	I_{IOVCC}	-	TBD	-	mA	IOVCC=1.8V
Logic input voltage	VIH	0.7*IOVCC	-	IOVCC	V	
	VIL	GND	-	0.3*IOVCC	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I_F	-	20	-	mA	
Driving Voltage	V_F	10.8	-	13.6	V	
Power consumption	W_{BL}	0.216	-	0.272	W	
LED Life-Time	N/A	-	50,000	-	Hours	Ta=25℃ Note 1

Note 1:LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :



3.3 Touch Panel

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply voltage	VCC	-	3.3	-	V	
Analog supply current	I_{VCC}	-	TBD	-	mA	VCC=3.3V
Input high-level voltage	VIH	0.7*VCC	-	VCC	V	
Input low -level voltage	VIL	GND	-	0.3*VCC	V	

4. Interface Pin Assignment

4.1 LCM Pin Assignment

Recommended connector：FH26-45S-0.3SHW manufactured by HIROSE

No.	Symbol	Description
1	VCI	Power supply
2	IOVCC	Digital power supply
3	IM0	<table><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr></table>
4	IM3	
5	IM2	
6	IM1	
7	RESET	Global reset pin
8	VSYNC	Vertical sync input. Negative polarity
9	HSYNS	Horizontal sync input. Negative polarity
10	DOTCLK	Dot-clock signal and oscillator source
11	ENABLE	Data Enable
12-29	DB17-DB0	DATA BUS
30	SDO	Serial output data
31	SDI	Serial Input data
32	RD	Read signal
33	WR/(D/CX)	I system :Write signal Serial interface: Data or command select
34	RS/(SCL)	I system :Data or command select Serial interface:Serial clock signal
35	CS	Chip select
36	GND	System Ground
37	LEDA	Power for LED backlight (Anode)
38	LEDK	Power for LED backlight (Cathode)
39	LEDK	Power for LED backlight (Cathode)
40-45	NC	No connection

4.2 Touch FPC Pin Assignment

No.	Symbol	Description
1	GND	Ground
2	SCL	I2C clock input
3	SDA	I2C data input and output
4	INT	Interrupt signal from CTP
5	RESET	Reset pin
6	VCC	Power supply

5. Interface Characteristics

5.1 DC Electrical Characteristics

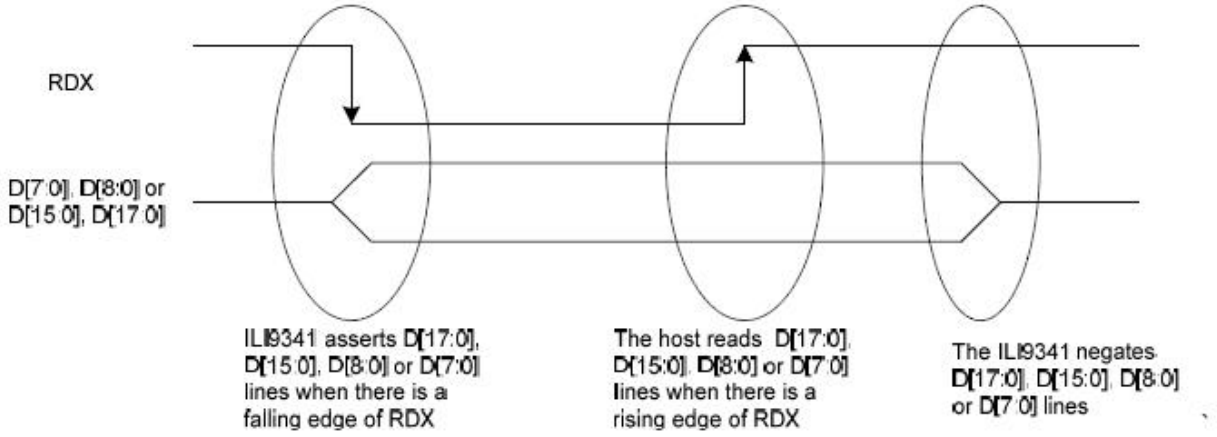
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDDIO	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.4	-	3.3	V
VCI	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO whichever is higher	-	3.3	V
VGH	Gate driver High Output Voltage Booster efficiency	No panel loading; 4x or 5x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	88	90	-	%
		No panel loading; 6x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	82	84	-	%
VCIX2	VCIX2 primary booster efficiency	No panel loading, ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	83	85	-	%
VGH	Gate driver High Output Voltage		9	-	18	V
VGL	Gate driver Low Output Voltage		-15	-	-6	V
VcomH	Vcom High Output Voltage		V_{CI} + 0.5	-	5	V
VcomL	Vcom Low Output Voltage		$-V_{CIM}$+0.5	-	-1	V
VLCD63	Max. Source Voltage		-	-	6	V
ΔVLCD63	Source voltage variation		-2		2	%
V_{OH1}	Logic High Output Voltage	Iout=-100μA	0.9* VDDIO	-	VDDIO	V
V_{OL1}	Logic Low Output Voltage	Iout=100μA	0	-	0.1*VDDIO	V
V_{IH1}	Logic High Input voltage		0.8*VDDIO	-	VDDIO	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*VDDIO	V
I_{OH}	Logic High Output Current Source	Vout = V_{DDIO}-0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	μA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	μA

C_{IN}	Logic Pins Input Capacitance			-	5	7.5	pF
R_{SON}	Source drivers output resistance			-	1	-	kΩ
R_{GON}	Gate drivers output resistance			-	5	-	kΩ
R_{COM}	Vcom output resistance			-	200	-	Ω
I_{dp}(262k)	Display current for 262k	Vddio= 1.8V, Vci = 2.8V. 5x/-5x booster ratio. Full color current consumption, without panel loading	Ivdd	-	150	300	uA
			Ivci	-	2.5	8	mA
I_{dp}(8 color)	Display current for 8 color mode	Current consumption for 8 color partial display, without panel loading	Ivdd	-	120	300	μA
			Ivci	-	1	5	mA
I_{slp}	Sleep mode current	Oscillator off, no source/gate output, Ram read write halt. Send command R10-0001 (sleep mode)	Ivdd	-	0.5	1	μA
			Ivci	-	10	75	μA

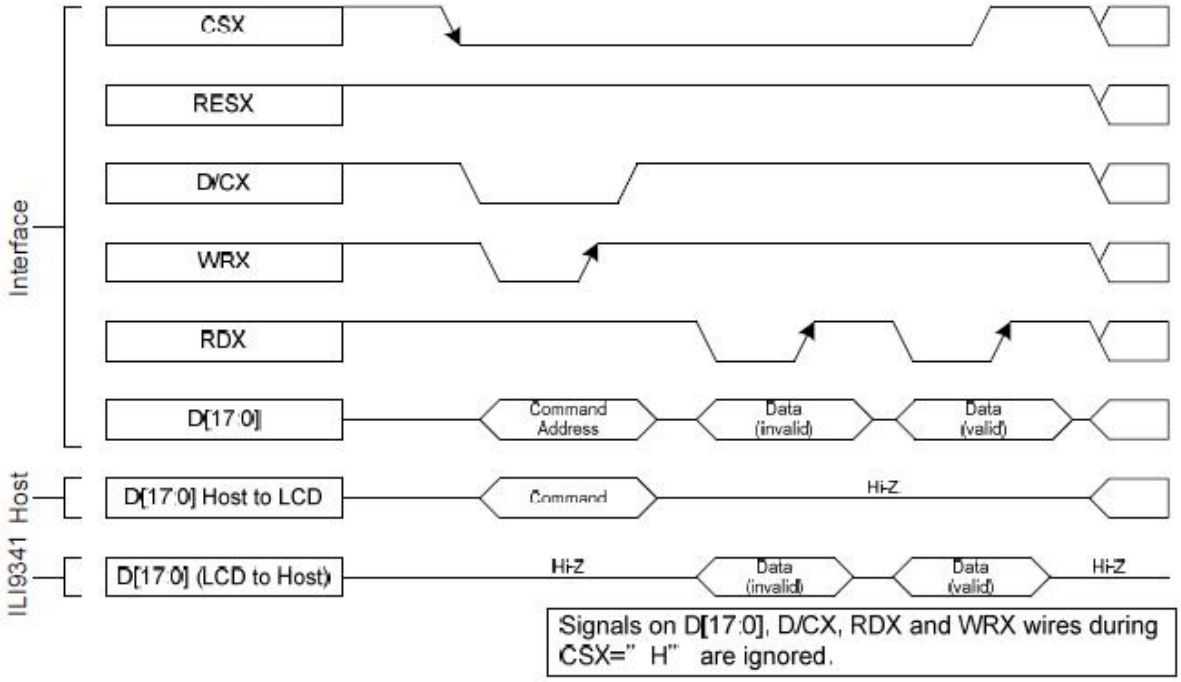
Remark: Ivdd = Ivddio

Note: The DC characteristic is base on only N-buffer or only P-buffer mode. (Refer to R3Fh command)

5.2 Timing

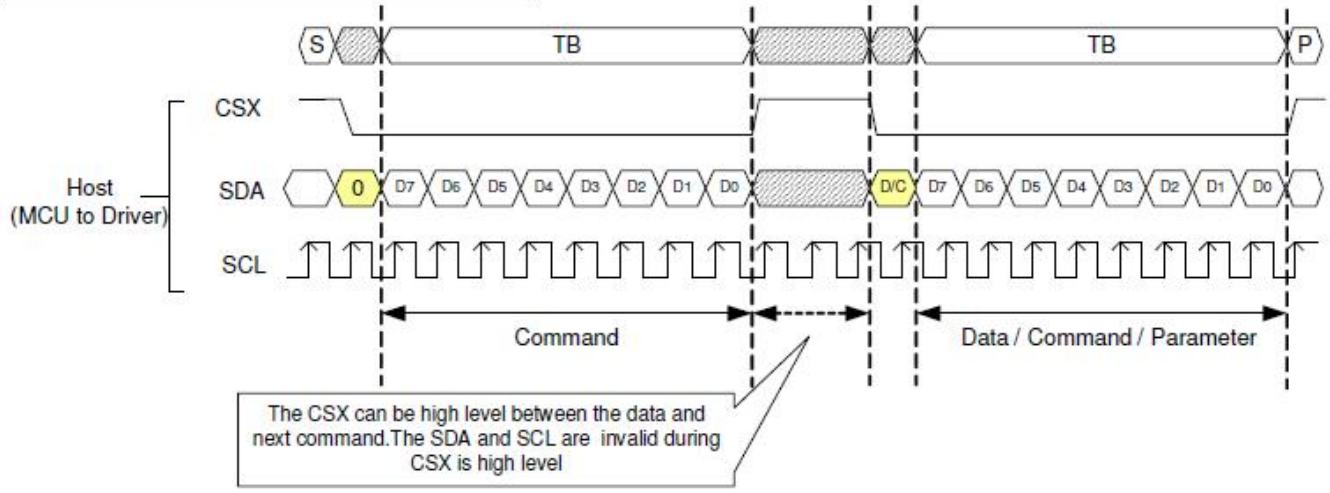


Note: RDX is an unsynchronized signal (It can be stopped).

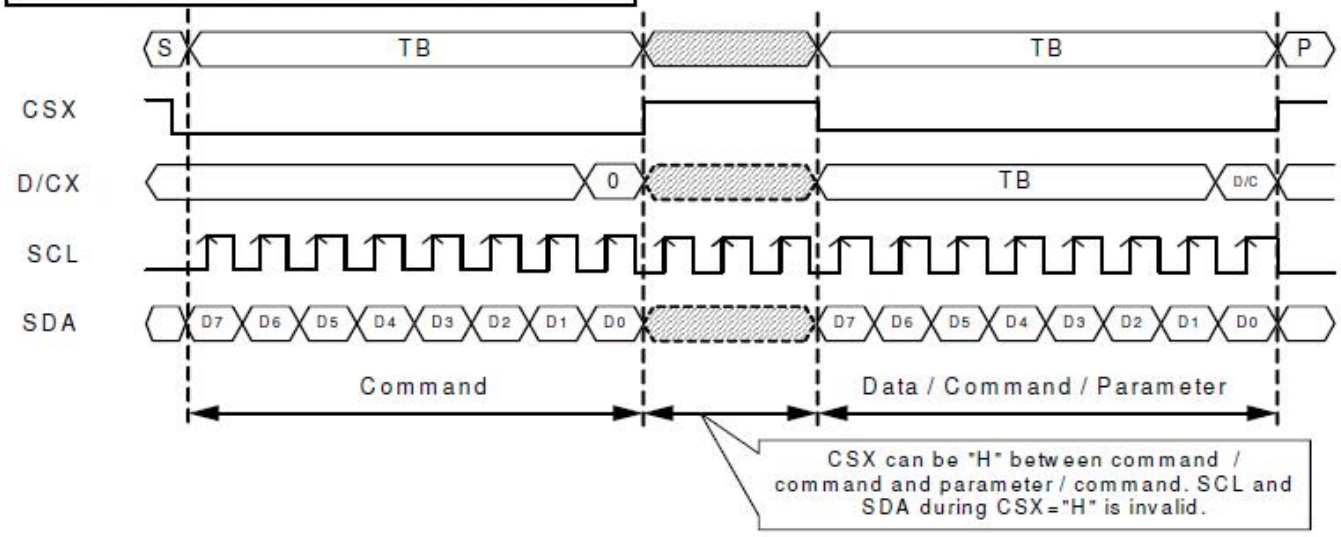


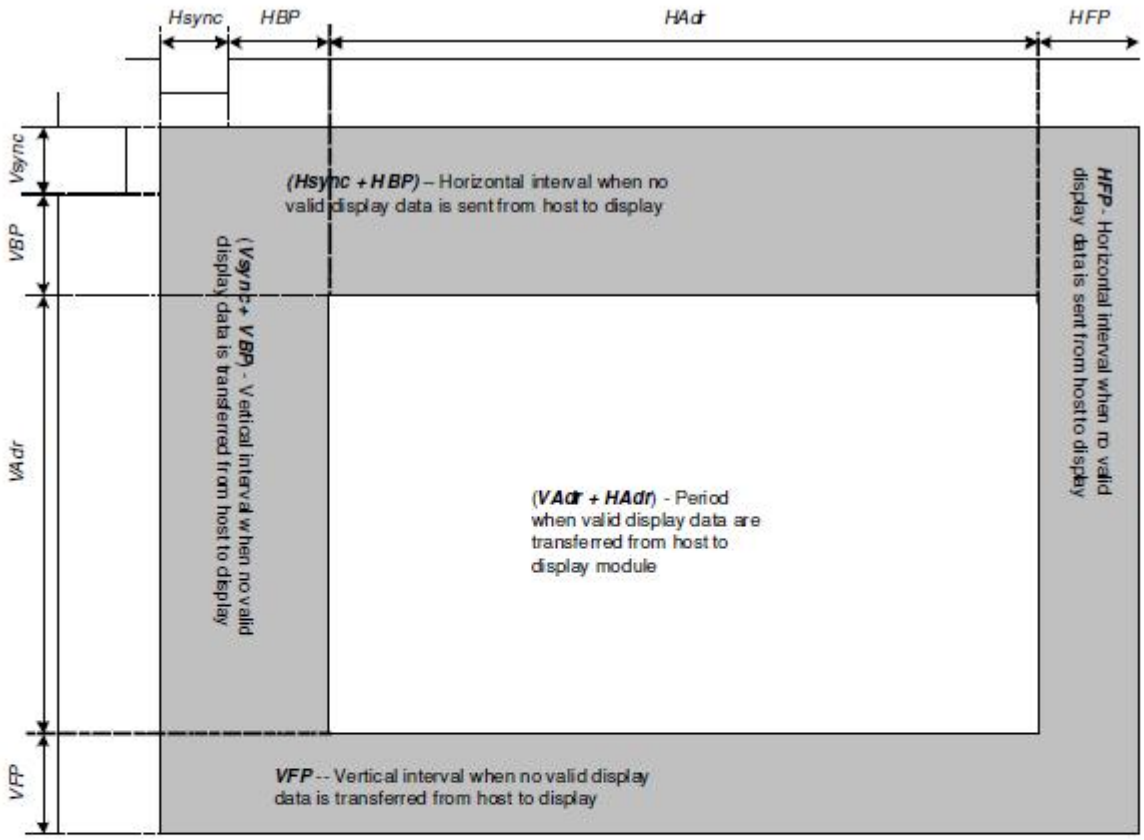
Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9341 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

3-line Serial Interface Protocol



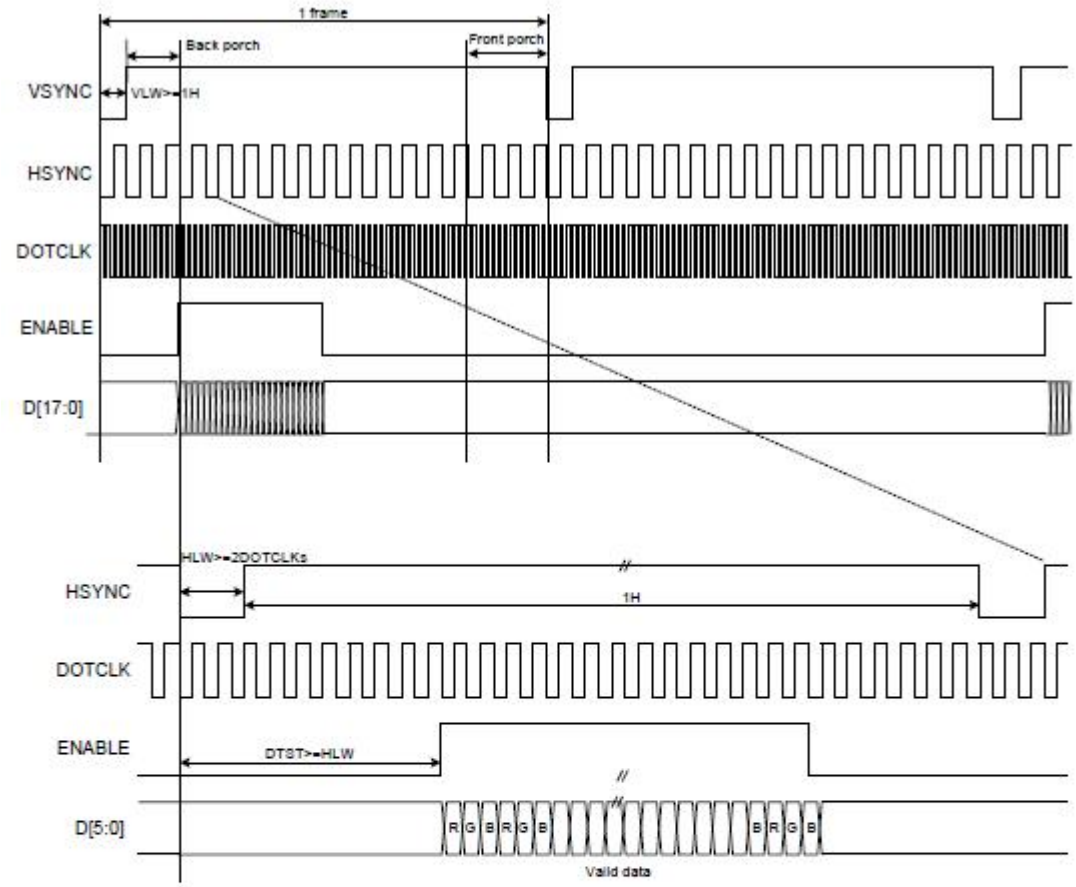
4-line Serial Interface Protocol



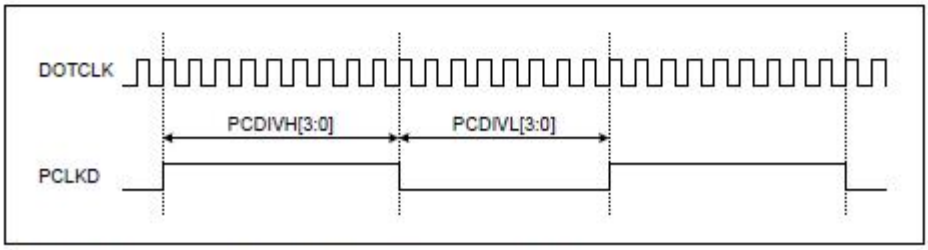


Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

The timing chart of 18-/16-bit RGB interface mode is shown as below.



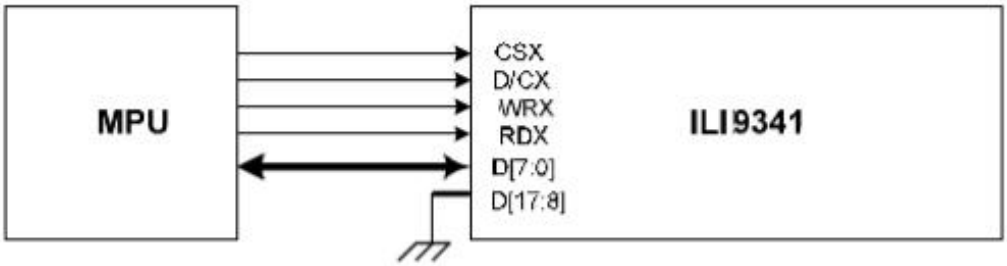
VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

The 8080-Ⅰ system 8-bit parallel bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0000".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

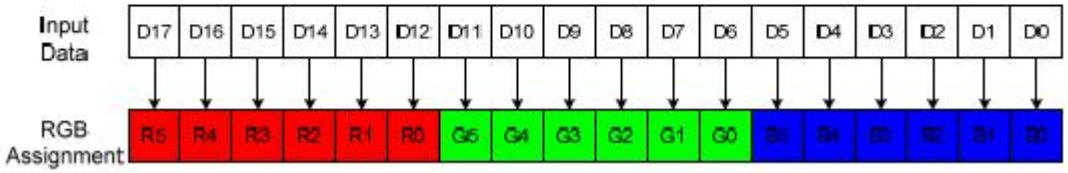
Count	0	1	2	3	4	...	477	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	...	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	...	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	...	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

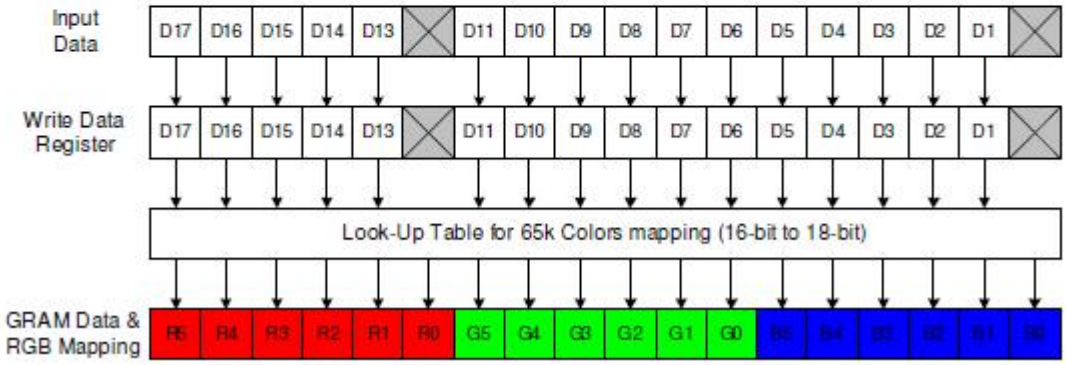
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D15		0R4	1R4	2R4	...	237R4	238R4	239R4
D14		0R3	1R3	2R3	...	237R3	238R3	239R3
D13		0R2	1R2	2R2	...	237R2	238R2	239R2
D12		0R1	1R1	2R1	...	237R1	238R1	239R1
D11		0R0	1R0	2R0	...	237R0	238R0	239R0
D10		0G5	1G5	2G5	...	237G5	238G5	239G5
D9		0G4	1G4	2G4	...	237G4	238G4	239G4
D8		0G3	1G3	2G3	...	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	...	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	...	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	...	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	...	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	...	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	...	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	...	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	...	237B0	238B0	239B0

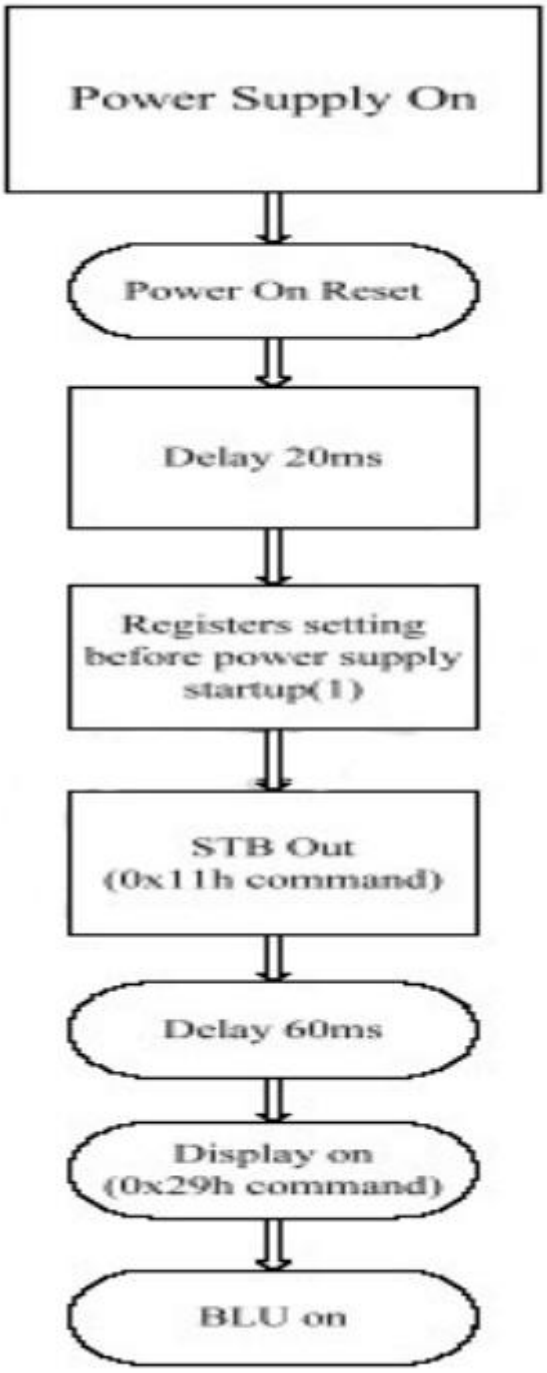
The 18-bit RGB interface is selected by setting the DPI [2:0] bits to "110". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to "10". The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.



The 16-bit RGB interface is selected by setting the DPI [2:0] bits to "101". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [17:13] & D [11:1]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [17:13] and D [11:1] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.



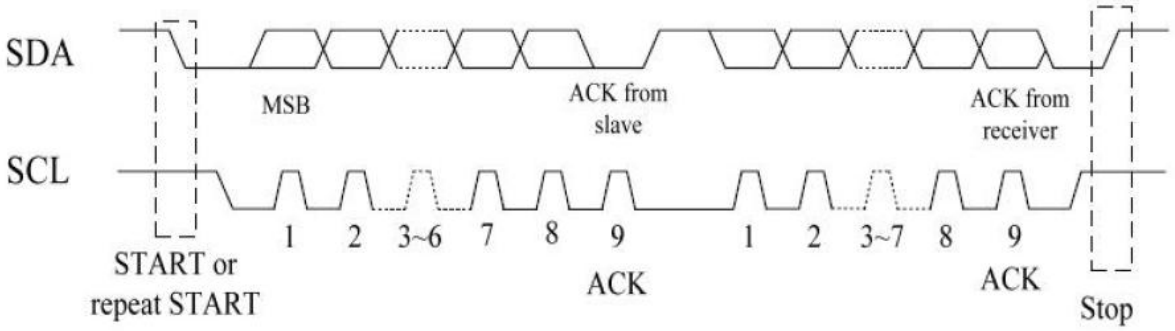
5.3 Power ON/OFF Sequence



5.4 Capacitive touch panel Specification

I2C

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 2-4.



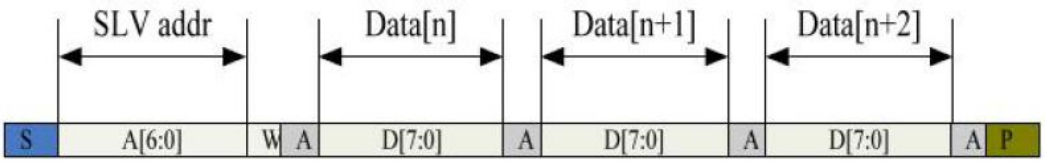


Figure 2-5 I2C master write, slave read

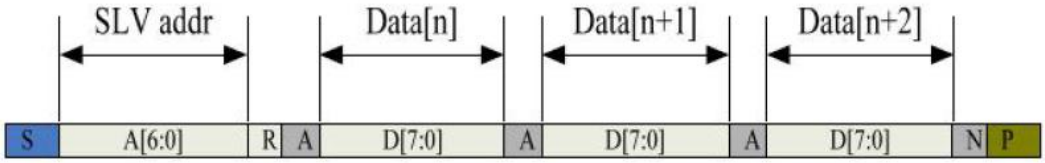


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address A[6:4]: 3'b011 A[3:0]: data bits are identical to those of I2CCON[7:4] register.
W	1'b0: Write
R	1'b1: Read
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

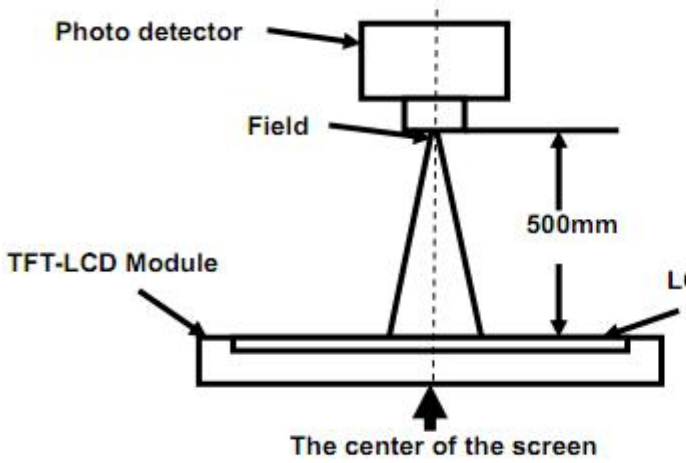
Parameter	Unit	Min	Max
SCL frequency	KHz	0	400
Bus free time between a STOP and START condition	us	4.7	\
Hold time (repeated) START condition	us	4.0	\
Data setup time	ns	250	\
Setup time for a repeated START condition	us	4.7	\
Setup Time for STOP condition	us	4.0	\

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	Φ=90°(12 o'clock)	-	80	-	deg	Note2
	θ_B	Φ=270°(6 o'clock)	-	80	-	deg	Note2
	θ_L	Φ=180°(9 o'clock)	-	80	-	deg	Note2
	θ_R	Φ=0°(3 o'clock)	-	80	-	deg	Note2
Response Time	T_{ON}	Normal θ=Φ=0°	-	16	21	msec	Note4
	T_{OFF}		-	19	24	msec	Note4
Contrast Ratio	CR		640	800	-	-	Note1 Note3
Color Chromaticity	W_X		0.260	0.310	0.360	-	Note1 Note5
	W_Y		0.286	0.336	0.386	-	Note1 Note5
Luminance	L		200	250	-	cd/m²	Note1 Note7
Luminance Uniformity	Y_U		75	80	-	%	Note1 Note6
NTSC	-		-	70	-	%	-

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2:Definition of viewing angle range and measurement system
Viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

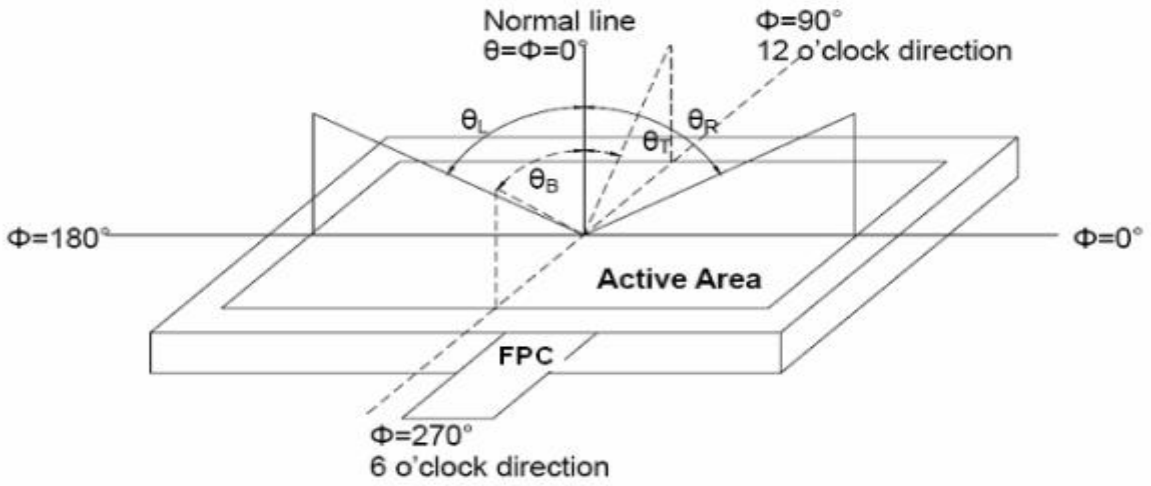


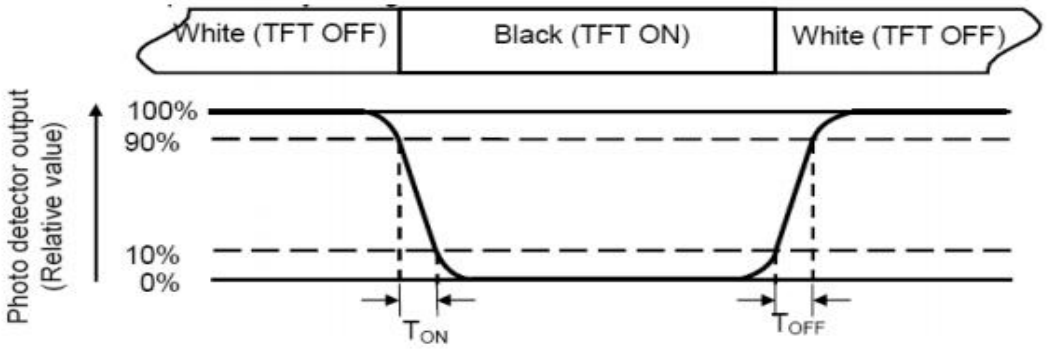
Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5:Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6:Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

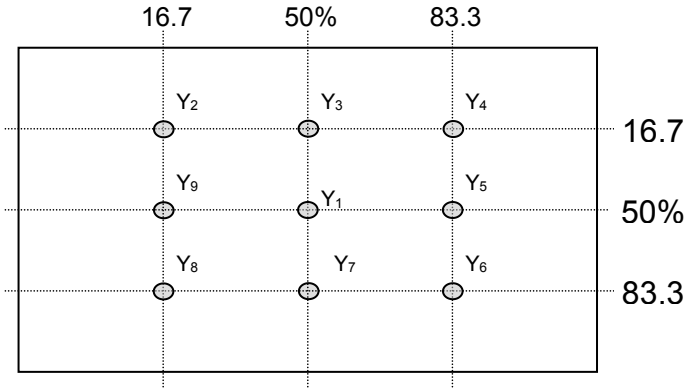


Fig. 2 Definition of points

Note 7:Definition of Luminance (Refer Fig. 2)

Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn).

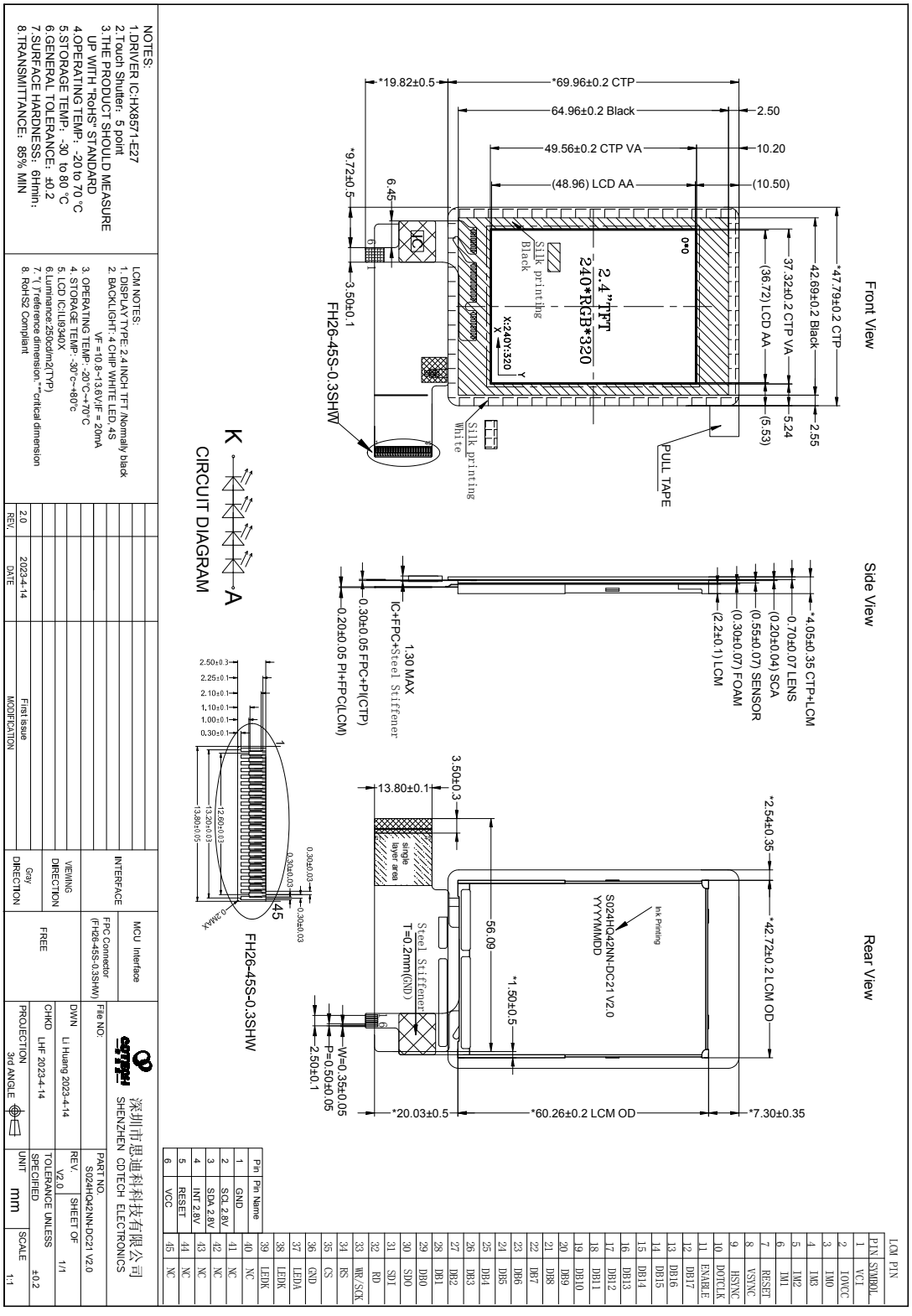
7. Reliability Test Items

Test Item	Test Conditions	
High Temperature Storage	Ta= +80℃	96hrs
Low Temperature Storage	Ta= -30℃	96hrs
High Temperature Operation	Ta= +70℃	96hrs
Low Temperature Operation	Ta= -20℃	96hrs
High Temperature and Humidity Storage	Ta= +60℃, 90% RH	96hrs
Thermal Shock (Non-operation)	-30℃/30 min ~ +80℃/30 min for 20 cycles Start with cold temperature end with high temperature	
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF	
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.	
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction	
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

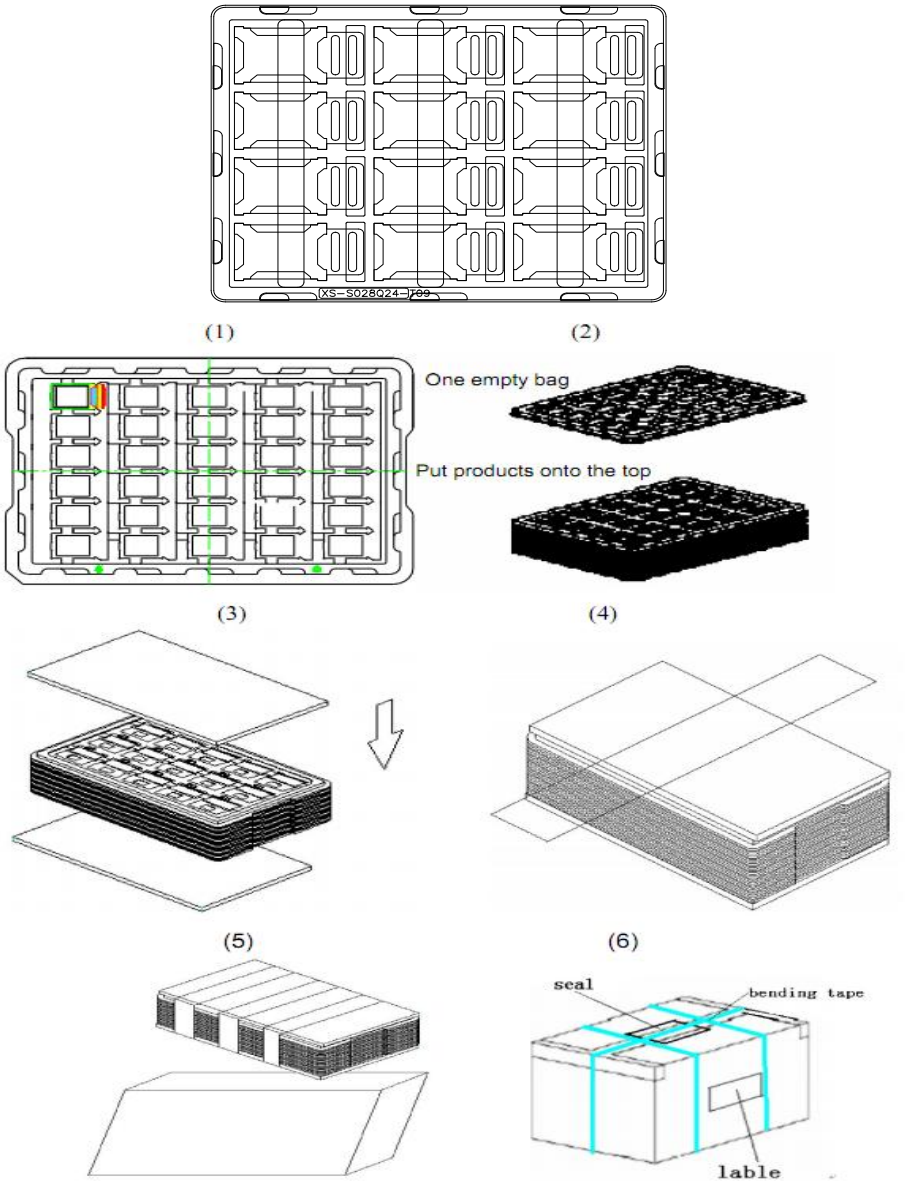
1). Air bubble in the LCD
2). Seal leak or Glass crack
3). Non display or abnormal display
4). Brightness reduction >50%

8. Mechanical Drawing



9. Packing

Packing Method



Steps:

1. Put module into tray cavity
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above
4. Fix the cardboard to the tray stack with adhesive tape
5. Put the tray stack into carton
6. Carton sealing with adhesive tape

10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1.When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2.The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time,the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3.The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.