PRODUCT SPECIFICATION

CDTECH Model: **S035CHV85EN**

CUSTOMER Model: -

Description: **3.5” TFT-LCD Module**

Version: **1.0**

CDTECH	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2022.8.4	2022.8.4	2022.8.4

	SIGNATURE	DATE
CUSTOMER APPROVAL		

Record of Revisions

Version	Revise Date	Description	Page
1.0	2022-08-02	First Release	-
	2022-08-04	Update the drawing page	22

Contents

1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	3.5	inch
Number of Pixels	320(H) RGB x 480(V)	pixels
Display Mode	Normally Black	-
Viewing Direction	Free	o' clock
Interface	RGB/MCU/MIPI	-
Display Colors	16.7M	colors
Outline Dimension	54.36(H) x 83.18(V) x 2.43(D)	mm
Active Area	48.96(H) x 73.44 (V)	mm
Pixel Pitch	0.153(H) x0.153(V)	mm
Driver IC	ILI9488	-
Operation Temperature	-20~70	℃
Storage Temperature	-30~80	℃

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Analog Supply voltage	VDD	-0.3	5.0	V	Note 1
Digital supply voltage	IOVCC	-0.3	3.6	V	Note 1

Note 1:Permanent damage may occur to the LCD module if beyond this specification.
Functional operation should be restricted to the conditions described under normal operating conditions.

3. Elecrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

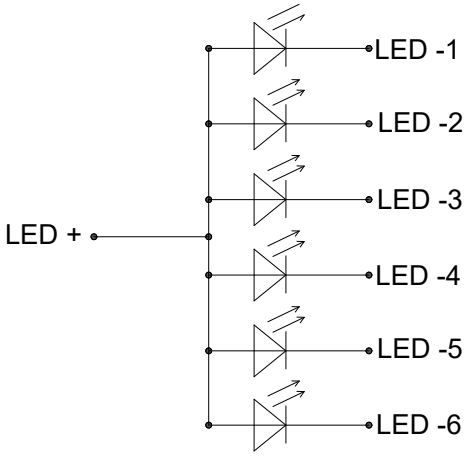
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Supply voltage	VCC	3.0	3.3	3.6	V	
Analog supply current	I_{VCC}	-	TBD	-	mA	VDD=3.3V
Logic supply voltage	IOVCC	1.65	1.8	3.3	V	
Logic supply current	I_{IOVCC}	-	TBD	-	mA	IOVCC=1.8V
Logic input voltage	VIH	0.7*IOVCC	-	IOVCC	V	
	VIL	GND	-	0.3*IOVCC	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I_F	-	120	-	mA	
Driving Voltage	V_F	5.6	-	6.4	V	
Power consumption	W_{BL}	0.627	-	0.768	W	
LED Life-Time	N/A	30,000	-	-	Hours	Ta=25℃ Note 1

Note 1:LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :



4. Interface Pin Assignment

4.1 LCM Pin Assignment

Recommended connector：FH26-61S-0.3SHW manufactured by HIROSE

No.	Symbol	Description
1	GND	Ground
2-5	NC	No connection
6-7	VCC	A supply voltage to the analog circuit
8	IOVCC	A supply voltage to the digital circuit
9	CABC-PWM	The PWM frequency output for LED driver control
10	NC	No connection
11	IM0	Select the interface mode (Note 1)
12	IM1	
13	IM2	
14	NC	No connection
15	RESX	Reset input signal
16-39	DB23-DB0	Data bus
40	RDX	serve as a read signal
41	WRX/SCL	8080 system (WRX): Serves as a write signal and writes data at the rising edge 3/4-line serial interface (SCL): The pin used as serial clock pin
42	D/CX	Data/Command Selection pin. Low: Command H: Parameter
43	CSX	Chip select input signal
44	SDI	Serial data input/output
45	SDO	Serial data output
46	VSYNC	Vertical sync input. Negative polarity
47	HSYNC	Horizontal sync input. Negative polarity
48	ENABLE	A data ENABLE input signal,Fix to DGND level when not in use.
49	DOTCLK	Dot-clock signal and oscillator source
50	MIPI_CLK_P	Positive polarity of low voltage differential clock signal
51	MIPI_CLK_N	Negative polarity of low voltage differential clock signal
52	MIPI_DATA_N	Negative polarity of low voltage differential data signal
53	MIPI_DATA_P	Positive polarity of low voltage differential data signal
54	GND	Ground
55	LED-A	Backlight LED Anode

56	LED-K1	Backlight LED Cathode
57	LED-K2	Backlight LED Cathode
58	LED-K3	Backlight LED Cathode
59	LED-K4	Backlight LED Cathode
60	LED-K5	Backlight LED Cathode
61	LED-K6	Backlight LED Cathode

Note 1:

IM2	IM1	IM0	Interface
0	0	0	MIPI-DBI Type B 24-bit bus (DB_EN = 1)
0	0	0	MIPI-DBI Type B 18-bit bus (DB_EN = 0)
0	0	1	MIPI-DBI Type B 9-bit bus
0	1	0	MIPI-DBI Type B 16-bit bus
0	1	1	MIPI-DBI Type B 8-bit bus
1	0	1	MIPI-DBI Type C Option 1 (3-line SPI)
1	1	0	MIPI DSI
1	1	1	MIPI-DBI Type C Option 3 (4-line SPI)

5. Interface Characteristics

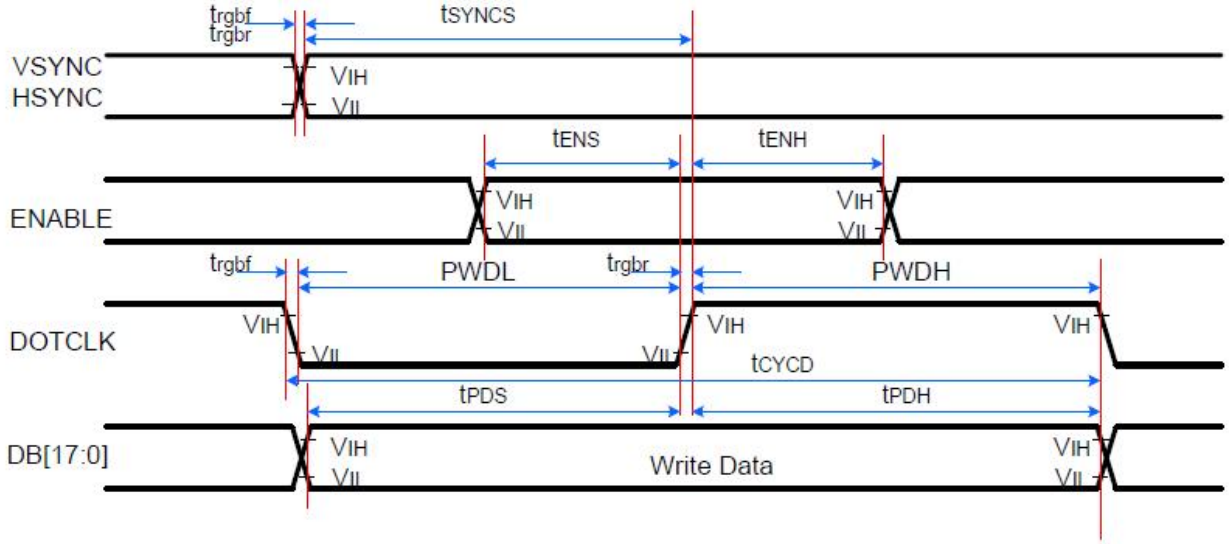
5.1 DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	3.3	V	
Logic operating voltage	IOVCC	-	1.65	1.8	3.3	V	Note 1, 2
OTP Supply voltage	DDVDH	-	-	7	-	V	Note 1
Logic High level input voltage	VIH	-	0.7*IOVCC		IOVCC	V	Note 1
Logic Low level input voltage	VIL	-	-0.3		0.3*IOVCC	V	Note 1
Logic High level output voltage TE, SDO (SDA) , CABC_PWM_OUT	VOH	IOH = -1.0mA	0.8*IOVCC		IOVCC	V	Note 1
Logic Low level output voltage TE, SDO (SDA) , CABC_PWM_OUT	VOL	IOL = +1.0mA	0		0.2*IOVCC	V	Note 1
Gate Driver High Voltage	VGH	-	10.0	-	20	V	
Gate Driver Low Voltage	VGL	-	-15.0	-	-6.0	V	
Driver Supply Voltage	-	|VGH-VGL|	16	-	32	V	
Input and Output							
Logic High Level Input Voltage	VIH	-	0.7*IOVCC	-	IOVCC	V	
Logic Low Level Input Voltage	VIL	-	DGND	-	0.3*IOVCC	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-2.0	-	-0.06	V	Note 3
Source Driver							
Source Output Range	VSOUT	-	0.1	-	VREG1OUT-0.1	V	Note 4
Positive Gamma Reference Voltage	VREG1OUT	-	3.625	-	5.5	V	
Negative Gamma Reference Voltage	VREG2OUT	-	-5.5	-	-3.625	V	
Source Output Setting Time	Tr	Below with 99% precision	-	10	-	uS	Note 3. 4
Output Deviation Voltage (Source Output channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	20	mV	Note 3
		4.2V>Sout>0.8V	-	-	15	mV	-
Output Offset Voltage	VOFFSET	-	-	-	35	mV	Note 3
Booster Operation							
Booster (VCIx2) Voltage	DDVDH	-			6	V	
Booster (VCIx2) Voltage	DDVDL	-	-6			V	
Booster (VCIx2 Drop Voltage)	VCI1x2 drop	loading=1mA	-	-	5	%	
Gate Driver High Voltage	VGH	-	10.0	-	20	V	
Gate Driver Low Voltage	VGL	-	-15.0	-	-6.0	V	
Standby mode current consumption (Ta = 25℃, Interface: DBI and DPI)							
Sleep in mode	VCI	VCI=2.8V IOVCC=1.8V	-	100	-	uA	
Deep Standby mode	VCI		-	1	-	uA	

Notes:

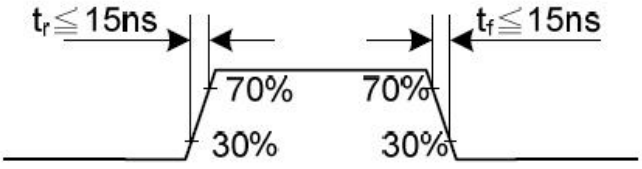
1. Ta = -30 to 70 ℃ (no damage up to 85℃ (at maximum)), IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, DGND=0V.
2. Supply the digital IOVCC voltage equal to or less than the analog VCI voltage.
3. Source channel loading = 10KΩ,30pF/channel
4. The maximum value is between 10KΩ,30pF/channel and Gamma setting value.

5.2 DPI Parallel Interface (RGB Interface) Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB [23:0]	t_{POS}	Data setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V



5.3 DPI Parallel Interface (RGB Interface) Timing

The DPI can display moving pictures by two ways: rewrite into the GRAM and transmit directly to the shift register. The selection is set by the register BPGRAM (bypass GRAM) and RM bit. The RM bit selects an interface for the access operation of the Frame Memory. For the DPI, RM should be set as 1.

BPGRAM	Display Data Path
1	Direct to shift register
0	Write into Memory
RM	**Interface for RAM access**
0	System interface
1	RGB interface

The DM bit selects the clock operation mode. It allows switching between display operations in synchronization with the internal oscillation clock. If DM = 1, the external DOTCLK cannot be stopped unless it enters the Sleep-In mode.

DM	RGB Interface Operating Clock Selection
0	Internal system clock
1	RGB interface (DOTCLK)

RGB Interface Selection

The DPI can be selected by the RCM bit. When the RCM is set to 0, the DE mode is selected by VSYNC, HSYNC, DOTCLK, ENABLE, and DB [23:0] pins. When RCM is set to 1, the SYNC mode is selected by VSYNC, HSYNC, DOTCLK, and DB [23:0] pins. It supports several pixel formats that can be selected by DPI [2:0] bits in Pixel Format Set (R3Ah) command. The selection of a given interface is done by DPI [2:0], as shown in Table 6 and Figure 17.

Table 6: DPI Interface Selection

RCM	DPI [2:0]			RGB Interface Mode	RGB Mode	Used Pins
0	1	1	1	24-bit RGB interface (16.7M colors)	**DE Mode** Valid data is determined by the ENABLE signal.	VSYNC, HSYNC, ENABLE, DOTCLK, DB [23:0]
0	1	1	0	18-bit RGB interface (262K colors)		VSYNC, HSYNC, ENABLE, DOTCLK, DB [17:0]
0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, ENABLE, DOTCLK, DB [15:0]
1	1	1	1	24-bit RGB interface (16.7M colors)	**SYNC Mode** In the SYNC mode, ENABLE signal is ignored; blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, DB [23:0]
1	1	1	0	18-bit RGB interface (262K colors)		VSYNC, HSYNC, DOTCLK, DB [17:0]
1	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, DB [15:0]

24-bit DPI interface connection (DB [23:0] is used): set pixel format DPI [2:0] = 3'h7

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

18-bit DPI interface connection (DB [17:0] is used): set pixel format DPI [2:0] = 3'h6

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
						R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit DPI interface connection (DB [15:0] is used): set pixel format DPI [2:0] = 3'h5

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
								R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 17: DPI Interface 24/18/16 Pixel Format Selection

The Pixel clock (DOTCLK) runs all the time without stop. It is used to enter VSYNC, HSYNC, ENABLE and DB [23:0] states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as the internal clock for other functions of the display module.

Vertical synchronization (VSYNC) is used to indicate when a new frame of the display is received. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to indicate when a new line of the frame is received. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Data Enable (ENABLE) is used to indicate when the RGB information that should be transferred in the display is received. This is a high enable, and its state is read to the display module by a rising edge of the DOTCLK signal.

DB [23:0] is used to indicate what is the information of the image that is transferred on the display (when ENABLE = 0 (low) and there is a rising edge of DOTCLK). DB [23:0] can be 0 (low) or 1 (high). These lines are read by a rising edge of the DOTCLK signal. In RGB interface modes, the input display data is written to GRAM first then outputs the corresponding source voltage according to the gray data from GRAM.

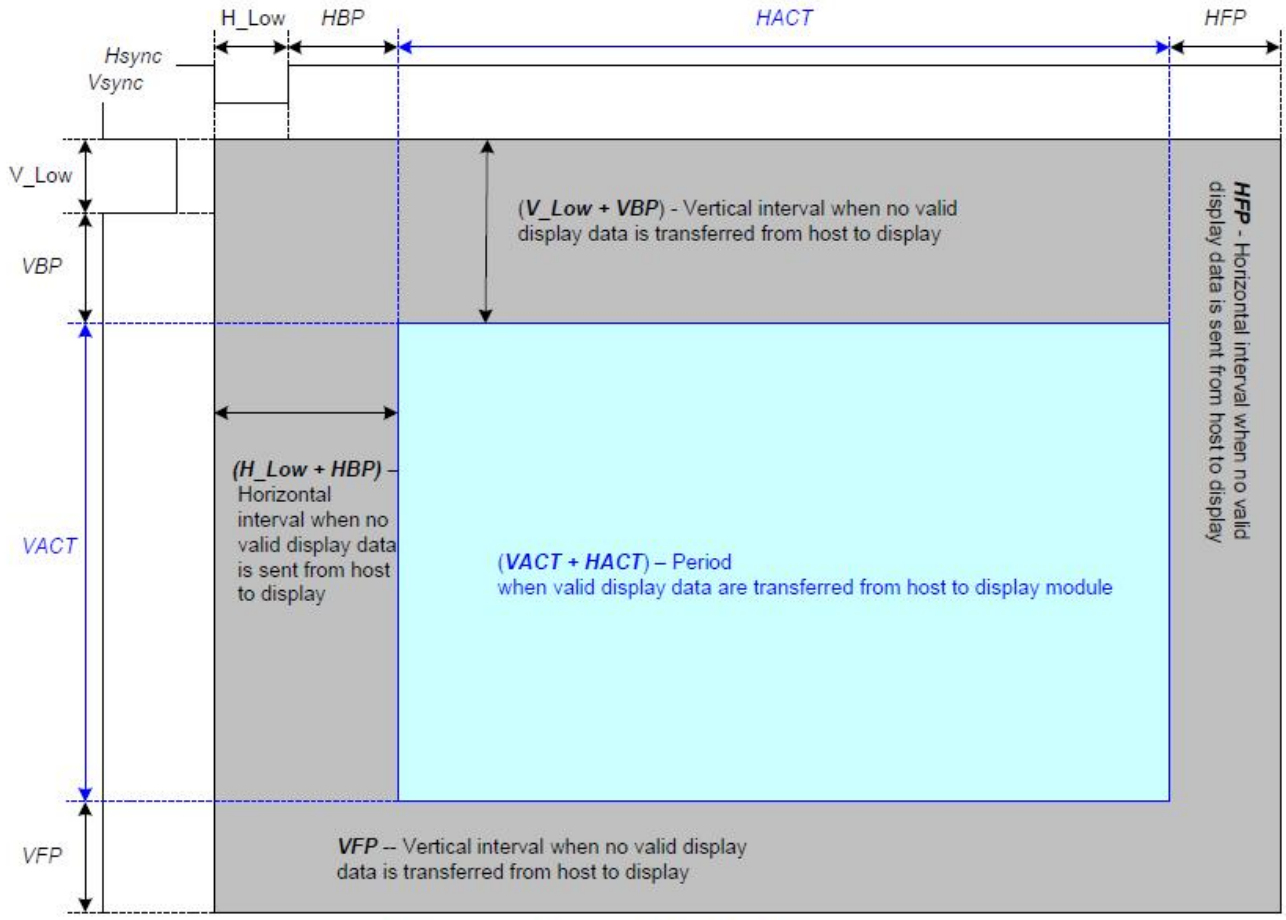


Figure 18: General DPI Timing Diagram

Parameters	Symbols	Min.	Typ.	Max.	Units
Horizontal Synchronization	H_Low	3	-	-	DOTCLK
Horizontal Back Porch	HBP	3	-	-	DOTCLK
Horizontal Address	HACT	-	320	-	DOTCLK
Horizontal Front Porch	HFP	3	-	-	DOTCLK
Horizontal Frequency		-	-	33	KHz
Vertical Synchronization	V_Low	1	-	-	Line
Vertical Back Porch	VBP	2	-	-	Line
Vertical Address	VACT	-	480	-	Line
Vertical Front Porch	VFP	2	-	-	Line
Vertical Frequency		60	-	70	Hz
DOTCLK cycle		100	-	50	ns
DOTCLK Frequency		10	-	20	MHz

Example：DOTCLK = 20Mhz, TE=70Hz, V_Low+VBP=2, VFP=2, H_Low+HBP=100, HFP=170.

The timing chart of 16-/18-/24-bit DPI interface mode is illustrated in Figure 19.

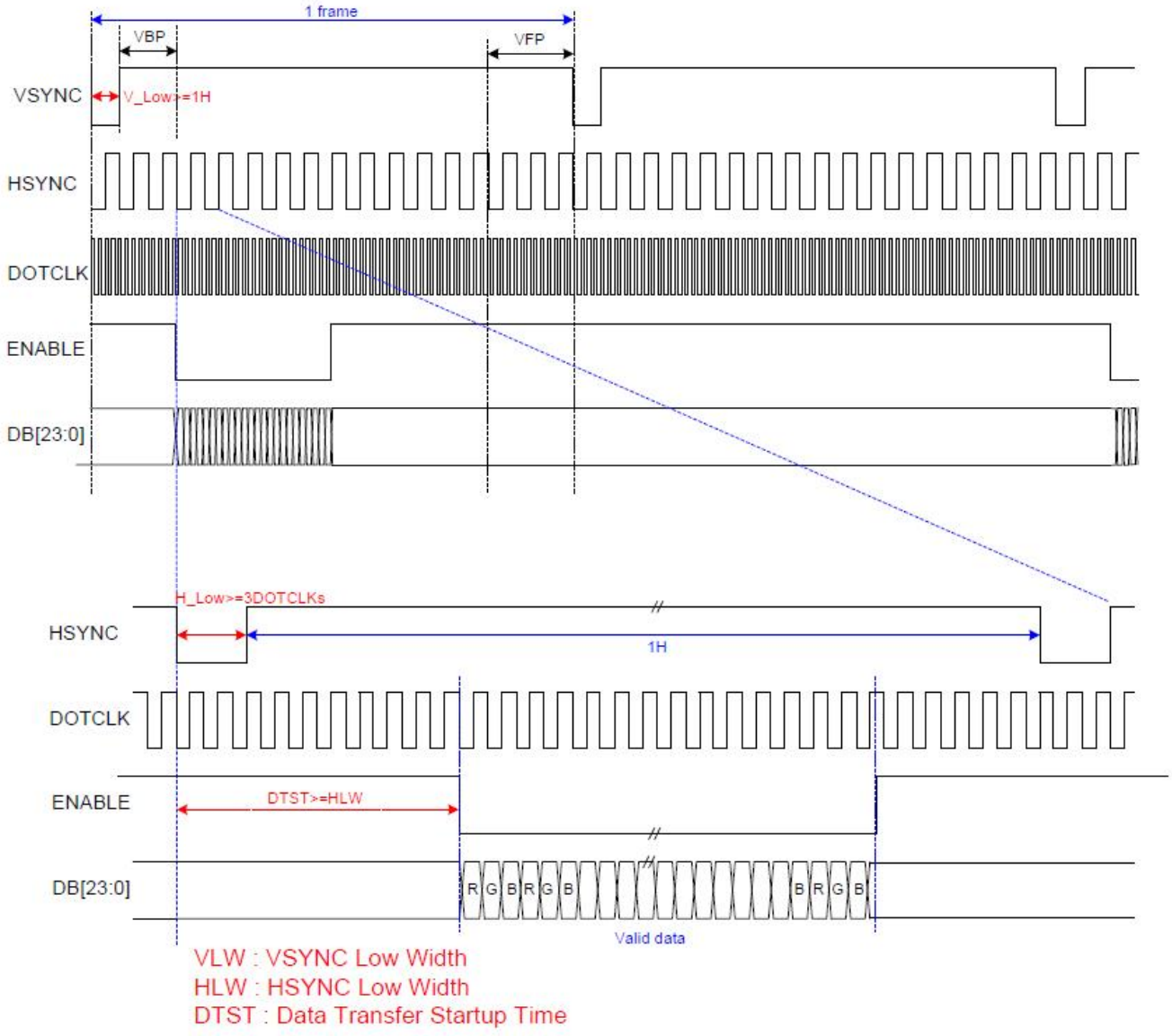


Figure 19: DPI Interface Timing Diagram

Note: VSPL = 0, HSPL = 0, DPL = 0 and EPL = 0 of Interface Mode Control B0h command.

5.4 DPI Parallel Interface (MPI) Timing

. MIPI_CLOCK Lanes

MIPI_CLOCK_P/N lanes can be driven into three different power modes:

- Low Power Mode (LPM)
- Ultra Low Power Mode (ULPM)
- High Speed Clock Mode (HSCM)

Clock lanes are in the single ended mode (LP = Low Power) when entering or leaving the Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single ended mode (LP = Low Power) when entering or leaving the High Speed Clock Mode (HSCM). These entering and leaving protocols use clock lanes in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different clock lanes power modes is illustrated below.

The mode change is also illustrated below.

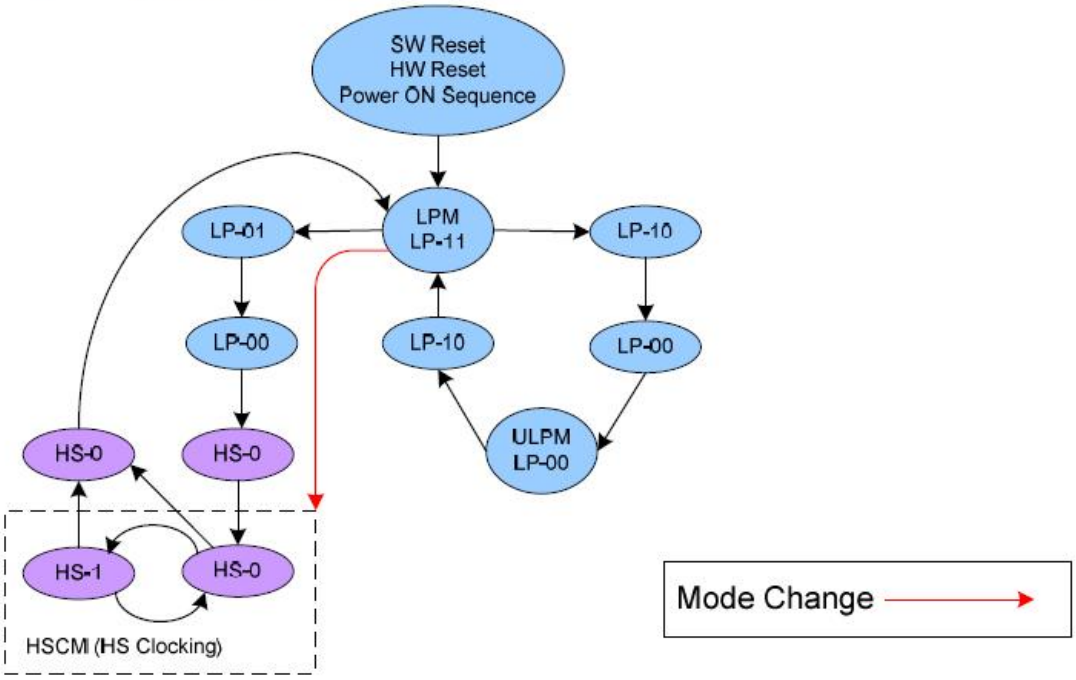


Figure 28: Mode Change from LPM to HSCM

MIPI_CLOCK_P/N lanes can be driven to the High Speed Clock Mode (HSCM), when MIPI_CLOCK lanes start to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). This sequence is illustrated below.

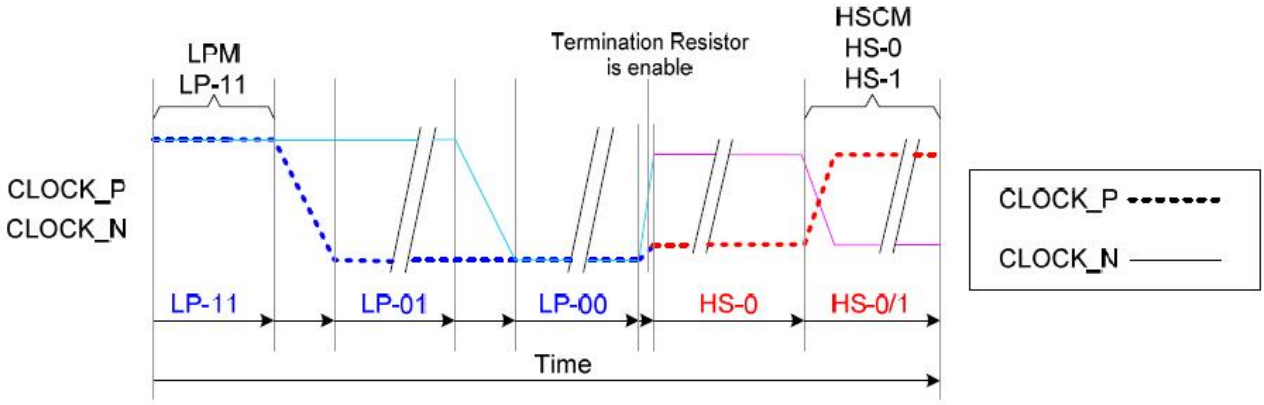


Figure 27: From LPM to HSCM

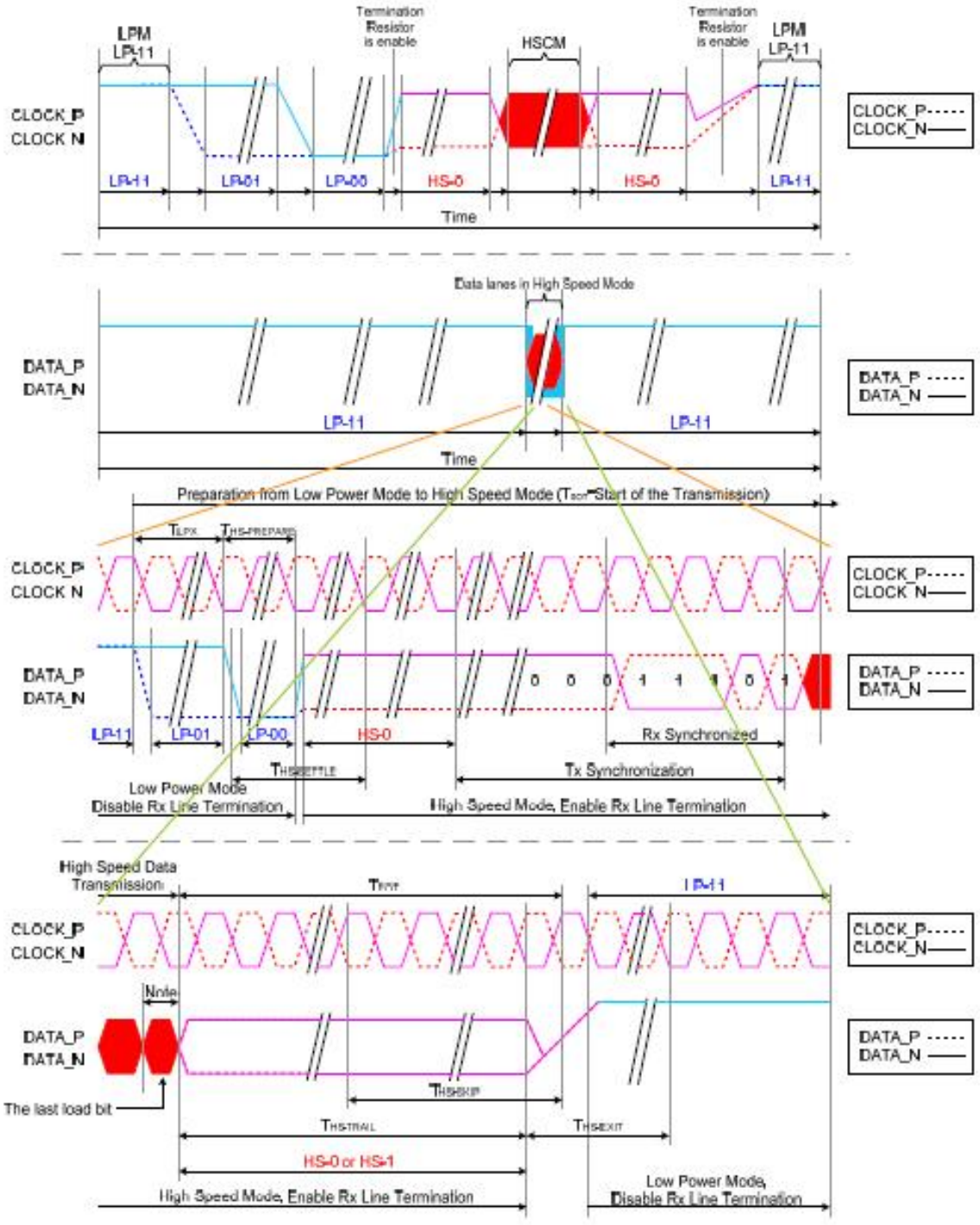


Figure 29: High Speed Clock Burst

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

5.5 MIPI_DATA Lanes

MIPI_DATA_P/N Data Lanes can be driven in different modes:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined in the following table.

Table 8: Entering and Leaving Sequence

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

The burst of the high-speed data transmission (HSDT) can consist of one or several data packet(s). These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the chapter "Short Packet (SPa) and Long Packet (LPa) Structures".

The single packet in High-Speed Data Transmission is illustrated below for reference purpose:

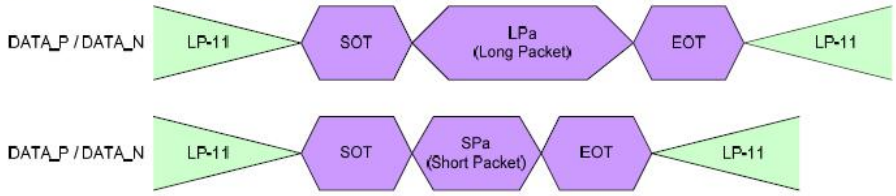


Figure 39: Single Packet in High-Speed Data Transmission

The multiple packets in High-Speed Data Transmission are illustrated below for reference purpose:

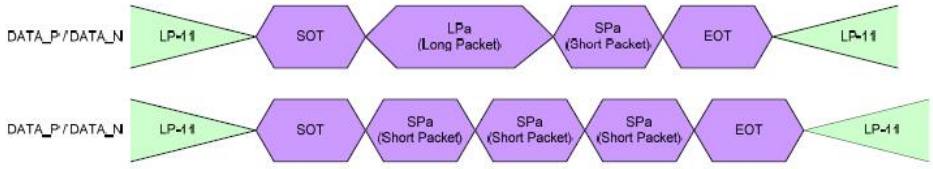


Figure 40: Multiple Packets in High-Speed Data Transmission (Examples)

Table 10: Abbreviations

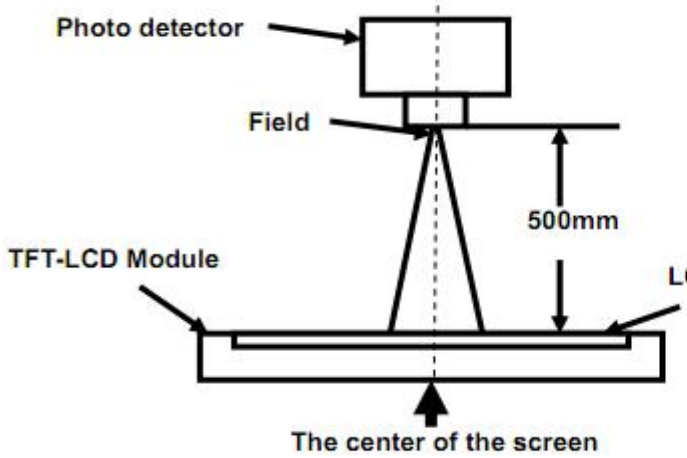
Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, both of Data lanes are 1 (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	Φ=90°(12 o'clock)	70	80	-	deg	Note2
	θ_B	Φ=270°(6 o'clock)	70	80	-	deg	Note2
	θ_L	Φ=180°(9 o'clock)	70	80	-	deg	Note2
	θ_R	Φ=0°(3 o'clock)	70	80	-	deg	Note2
Response Time	T_{ON}	Normal θ=Φ=0°	-	15	-	msec	Note4
	T_{OFF}		-	15	-	msec	Note4
Contrast Ratio	CR		-	700	-	-	Note1 Note3
Color Chromaticity	W_X		0.2746	0.3246	0.3746	-	Note1 Note5
	W_Y		0.2984	0.3484	0.3984	-	Note1 Note5
Luminance	L		600	700	-	cd/m²	Note1 Note7
Luminance Uniformity	Y_U		75	80	-	%	Note1 Note6
NTSC	-		-	50	-	%	-

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2:Definition of viewing angle range and measurement system
Viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

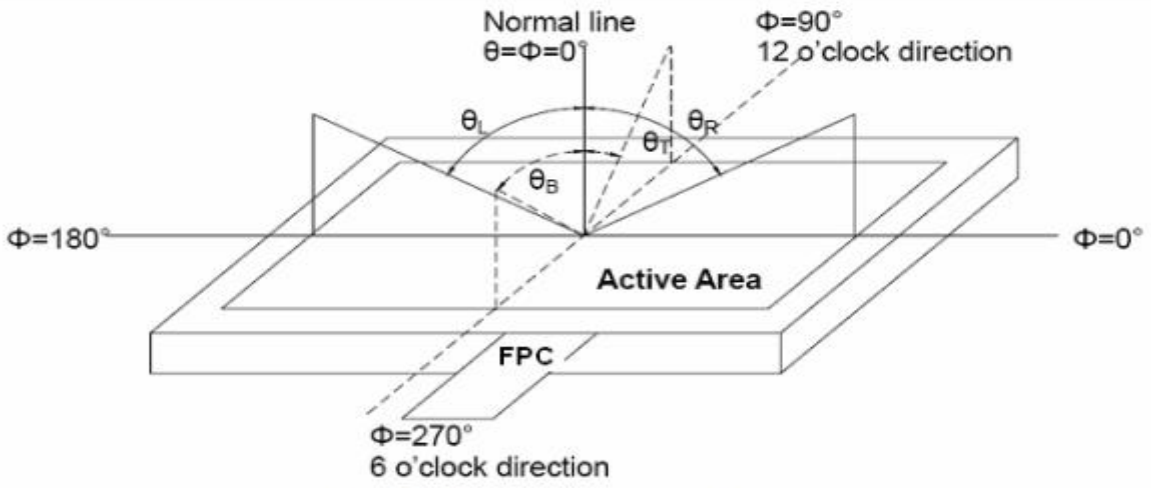


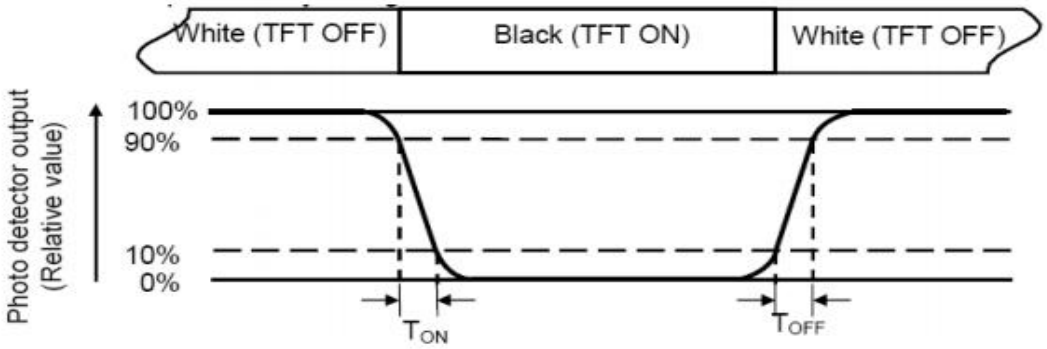
Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5:Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6:Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

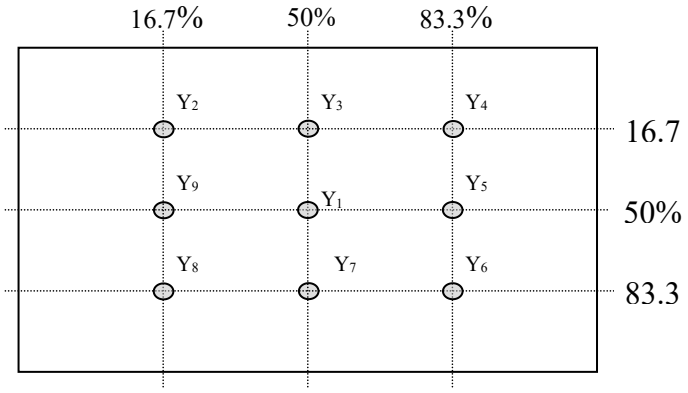


Fig. 2 Definition of points

Note 7:Definition of Luminance (Refer Fig. 2)

Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn).

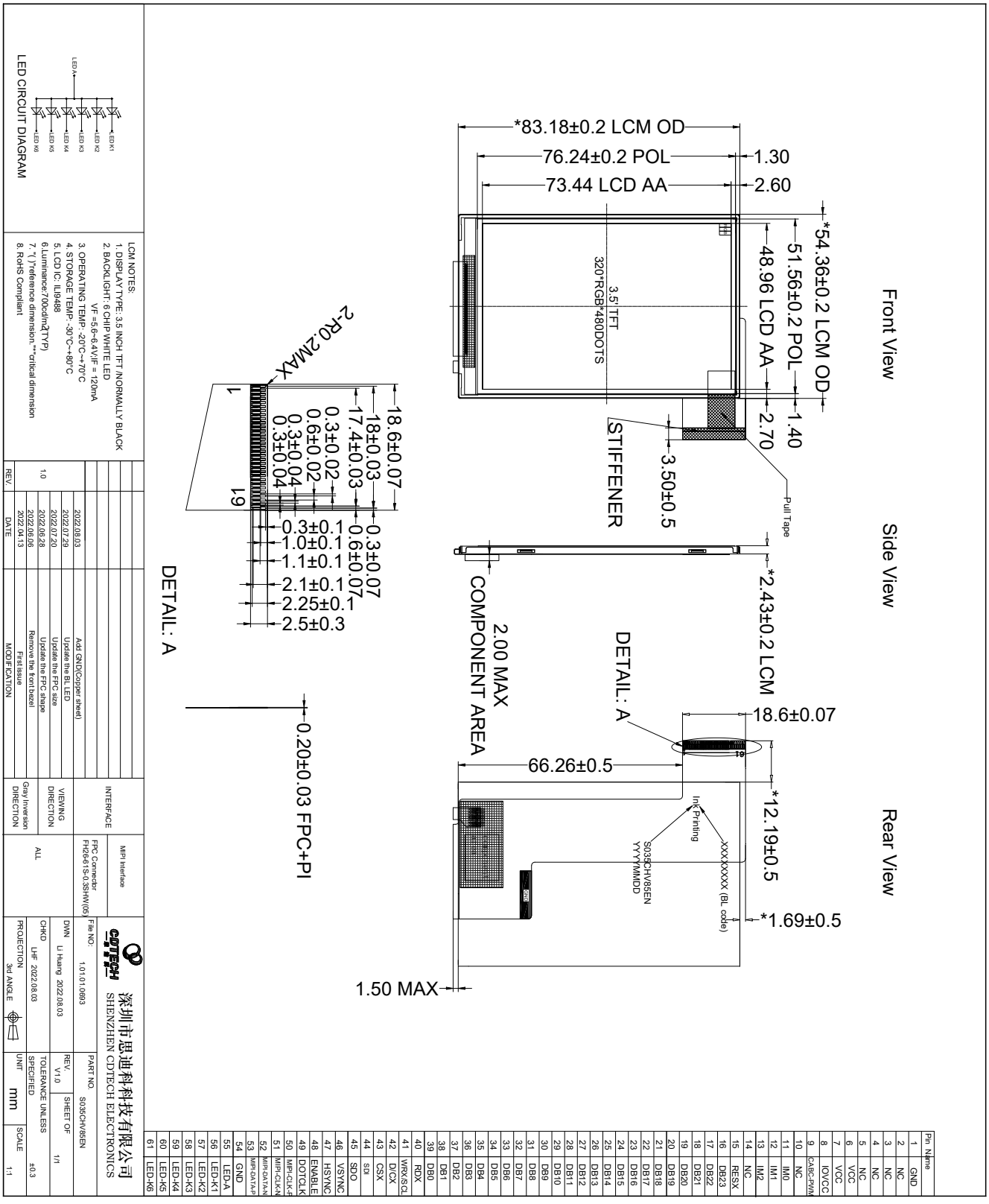
7. Reliability Test Items

Test Item	Test Conditions	
High Temperature Storage	Ta= +80℃	96hrs
Low Temperature Storage	Ta= -30℃	96hrs
High Temperature Operation	Ta= +70℃	96hrs
Low Temperature Operation	Ta= -20℃	96hrs
High Temperature and Humidity Storage	Ta= +60℃, 90% RH	96hrs
Thermal Shock (Non-operation)	-30℃/30 min ~ +80℃/30 min for 20 cycles Start with cold temperature end with high temperature	
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF	
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.	
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction	
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

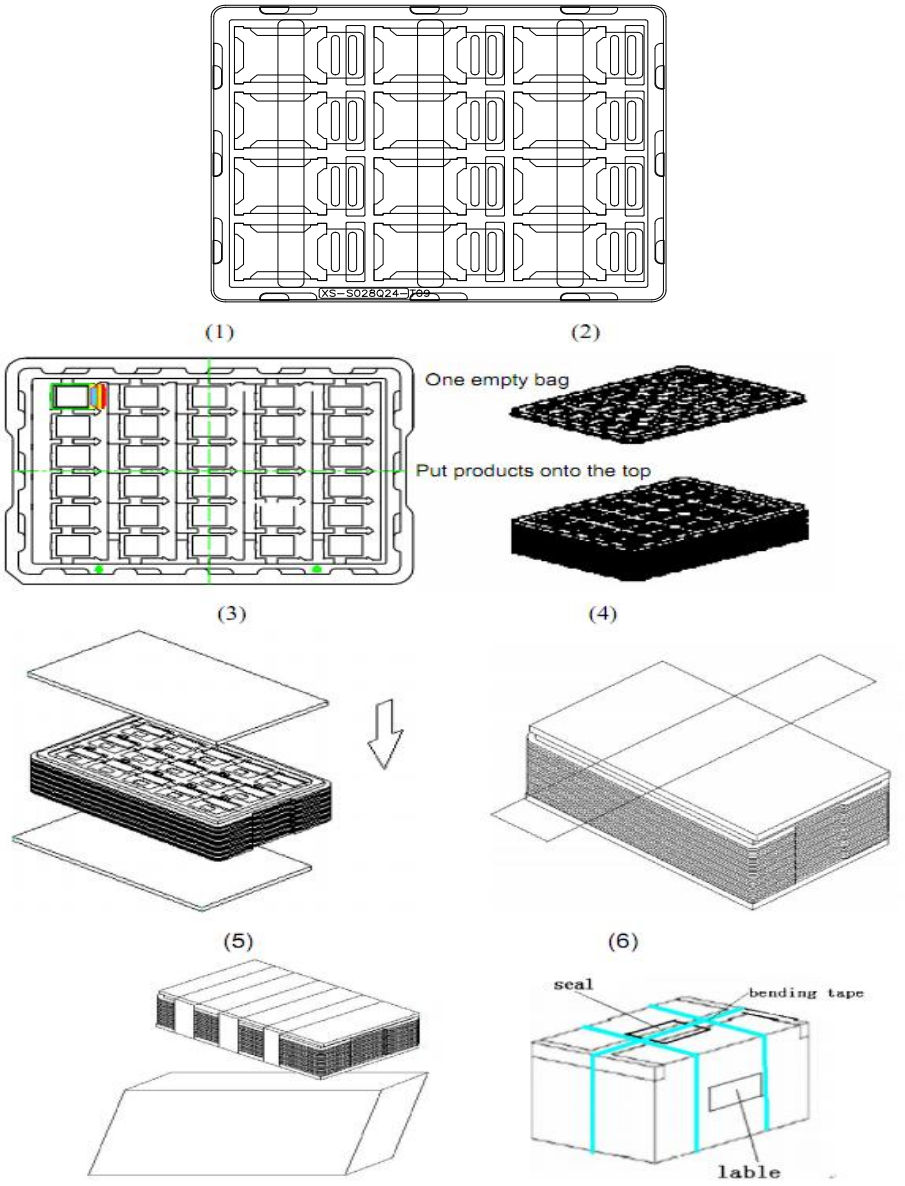
1). Air bubble in the LCD
2). Seal leak or Glass crack
3). Non display or abnormal display
4). Brightness reduction >50%

8. Mechanical Drawing



9. Packing

Packing Method



Steps:

1. Put module into tray cavity
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above
4. Fix the cardboard to the tray stack with adhesive tape
5. Put the tray stack into carton
6. Carton sealing with adhesive tape

10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1.When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2.The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time,the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3.The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.