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ILI2131A

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Single Chip Capacitive Touch Panel Controller

Data Sheet

(Preliminary)

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1. Introduction

ILI2131A is a high performance capacitive touch panel controller. It integrates I2C interfaces and KGD Flash memory into a QFN-68 package. ILI2131A has 55 touch sensor channels, it can support discrete and on-cell touch sensors.

With ILITEK's unique driving technology and algorithm, ILI2131A has excellent noise immunity ability and acheave high signal to noise ratio. For noise immunity, ILI2131A can support IEC-61000-4-6 CS 10Vrms requirement. ILI2131A is an optimal touch solution for several kind of applications.

2. Features

2.1 Driving and Sensing Channels for Capacitive Touch Panel

- 11 TX driving channels
- 28 RX sensing channels
- 16 TRX channels
- 1 guard ring pin.
- Integrated 10V pumping Tx voltage for driving heavy RC loading touch panel.
- Support mutual-cap and self-cap driving/sensing technology
- Support G/G (DITO), G/G (SITO), OGS, GFF, GF2, FFF and On-Cell touch panel stack up (approved by ILITEK or ILITEK qualified touch panel maker)
- Support both of direct bonding and air bonding with TFT and IPS LCD module (LCM)
- Support Ag nano wire (AgNW), metal mesh (copper or Ag), printing copper and ITO conductive material
- Support Diamond and proprietary sensor patterns (approved by ILITEK or ILITEK qualified touch panel maker)
- Support PET and glass cover lens
  - Plastic 0.2mm to 4mm, depends on panel size, touch size, panel stack up and performance requirements
  - Glass 0.4mm to 8mm, depends on panel size, touch size, panel stack up and performance requirements

2.2 Host Interface

- I2C
  - Support 100kHz standard mode and 400kHz fast mode clock rate
  - I2C slave clock stretching function
  - Support Windows HID over I2C protocol

2.3 Reset

- Support chip enable/disable input
- Support power on reset (POR) function
- Support low voltage detection (LVD) function

2.4 Power Supply

- Input voltage for Analog and Digital I/O (PVDD), nominal 3.3V
- On-chip 1.2V regulator output for Digital core (VDD12), nominal 1.2V
- On-chip X2 charge pump controller output (PVDD_MVCP), nominal 2*AVDD_HVCP
- On-chip programmingable MV regulator output for internal Analog circuit (AVDD)
- On-chip programmingable HV regulator output for internal Analog circuit (HVDD)

2.5 General Purpose I/O (GPIO)

- 4.9V general purpose I/O, up to 32 pin (Multi-function with Rx channel)

2.6 Package

- 68-pin, QFN-68, 8 × 8 × 0.75 mm, pitch 0.4 mm

2.7 Operating Temperature

- -40℃ to +85℃

2.8 storage **temperature**

- -55~125°C

3. Device Overview

3.1. Block Diagram

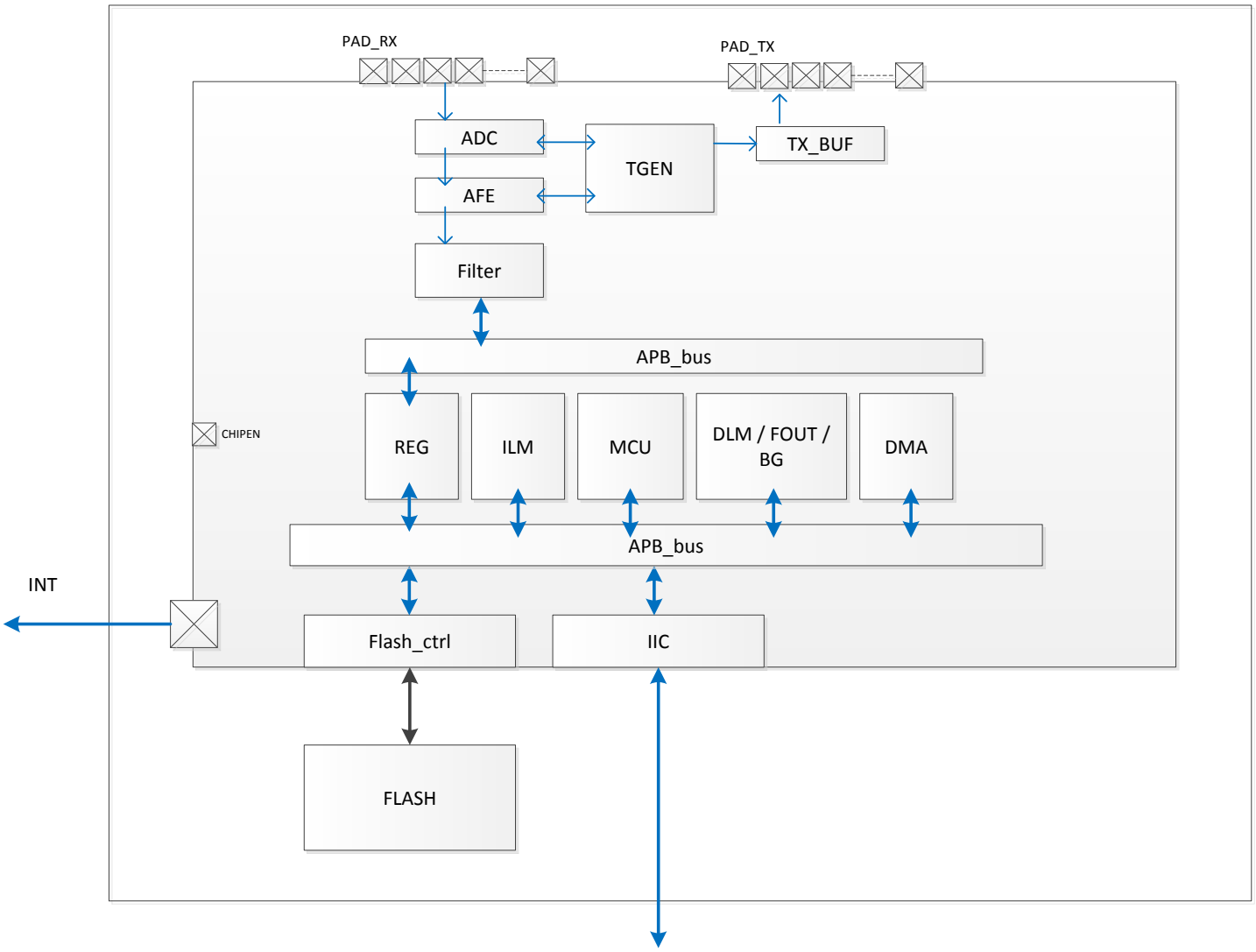


Figure 1. ILI2131A Block Diagram

3.2. Pin Configuration

3.2.1. QFN-68 (Top View)

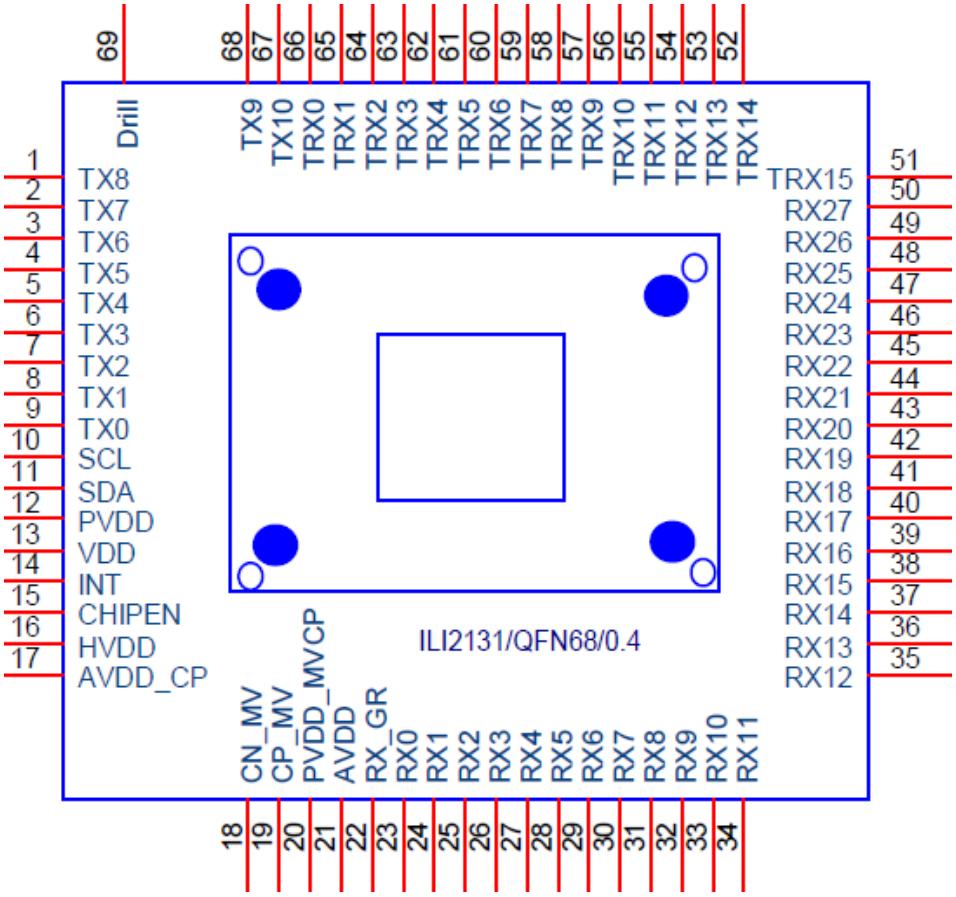


Figure 2. ILI2131A Schematic Symbol

3.2.2. Pin Definition

Pin	Name	Type	Power Supply	Description	If Unused...
1 ~ 9	TX8 ~ Tx0	I/O	HVDD	TX driving channel	Leave open
10	SCL	OD	PVDD	I2C Mode: Serial Clock.	Leave open
11	SDA	OD	PVDD	I2C Mode: Serial Data.	Leave open
12	PVDD	P	PVDD	Input 3.2V power supply. Connect to a bypass capacitor.	--
13	VDD12	P	--	On-chip 1.2V regulator output. Connect to a bypass capacitor.	--
14	INT	O	PVDD	Multi-function: INT: output interrupt signal to Host (I2C Mode).	--
15	CHIPEN	I	PVDD	Chip enable/disable signal.	--
16	HVDD	P	PVDD	Connect to a bypass capacitor. HVDD generator by self mode : On-chip programmingable HV regulator output. Output Level : 8V to 10 V External mode : Input Level : 10V to 30V	--
17	AVDD_CP	I	AVDD_CP	Input 3.3V power supply Connect to a bypass capacitor.	--
18	CN_MV	P	AVDD	On-chip X2 charge pump output clock (optional). Connect a flying capacitor to C1P_MV.	--
19	CP_MV	P	AVDD	On-chip X2 charge pump output clock (optional). Connect a flying capacitor to C1N_MV.	--
20	PVDD_MVCP	P	AVDD	On-chip X2 charge pump controller output. Connect to a bypass capacitor.	--
21	AVDD	P	AVDD	On-chip programmingable MV regulator output. Connect to a bypass capacitor.	--
22	GR	I/O	AVDD	RX driving channel TRX: output UART data to Host (UART Mode). Output Level : 4.9V, Input Level : 3.3V / 4.9V	--
23	RX0	I/O	AVDD	RX driving channel TRX: output UART data to Host (UART Mode). Output Level : 4.9V, Input Level : 3.3V / 4.9V	--
24 ~ 50	RX1 ~ RX27	I/O	AVDD	RX driving channel	Leave open
51 ~ 66	TRX0 ~ TRX15	I/O	PVDD	TRX driving channel. It can be programming to TX driving and RX sensing function.	Leave open
67 ~ 68	TX10 ~ TX9	I/O	PVDD	TX driving channel	Leave open
69	E-PAD	P	GND	Ground	--

Pin Type:

P: Power or Ground

I: Input only

O: Output only

I/O: Input or Output

OD: Open drain output

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Item	Symbol	Unit	Value
Input Power Supply 1	PVDD	V	-0.3 ~ +3.63
Input Power Supply 2	AVDD_CP	V	-0.3 ~ +3.63
Input Power Supply 3 (For External mode only)	HVDD	V	-0.3 ~ +25
Voltage forced onto any pin		V	-0.3 ~ +3.63
Parameters maximum writes		Cycle	10,000
ESD target for Human Body Model	HBM	V	4000
ESD target for Machine Model	MM	V	400
Maximum junction temperature	Tj	℃	125
Operating temperature	Topr	℃	-40 ~ +85
Storage temperature	Tstg	℃	-55 ~ +125

External mode : Customer supply HVDD Voltage for TP IC

CAUTION:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanently damage to the device. These are stresses ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability of the device.

4.2. Recommended Operating Conditions

Item	Symbol	Unit	Recommended Value
Input Power Supply 1	PVDD	V	3.3 ± 5%
Input Power Supply 2	AVDD_CP	V	3.3 ± 5%
Input Power Supply 3 (For External mode only)	HVDD	V	20 ± 100mV
Operating Temperature	Topr	℃	-40 ~ +85
Storage Temperature	Tstg	℃	-55 ~ +125
Temperature Slew Rate			10℃/min

4.3. Input Power Supply and GPIO Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Input Power Supply 1	PVDD	2.97	3.3	3.63	V	
Input Power Supply 2	AVDD_CP	2.97	3.3	3.63	V	
Input Power Supply 3 (External mode : 10V to 30V)	HVDD	-	10	30	V	
On-Chip 1.2V Regulator	VDD12	1.08	1.2	1.32	V	
Operating Current	PVDD		60		mA	1
Idle Current	PVDD		10		mA	1
GPIO Pull Down Resistor			200K		Ω	
Low Input Logic Level	VIL		0.3* PVDD		V	
High Input Logic Level	VIH		0.7* PVDD		V	

Note 1: The configuration values listed below table were used in the ILITEK's Bench Board to validate the interfaces and derive the operating current.

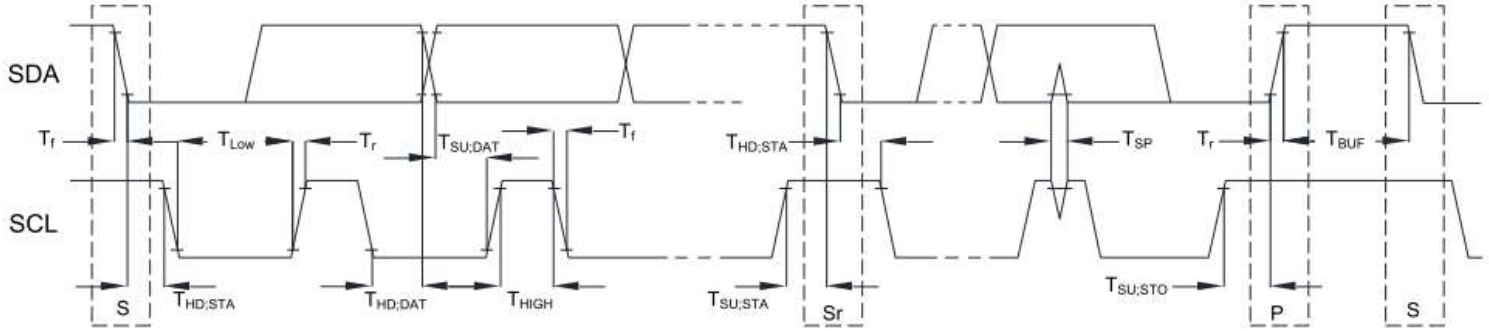
Note 2 : External mode : Customer supply HVDD Voltage for TP IC

Internal mode : TP IC generate HVDD voltage (8V to 10V) by self

Test Configuration Table

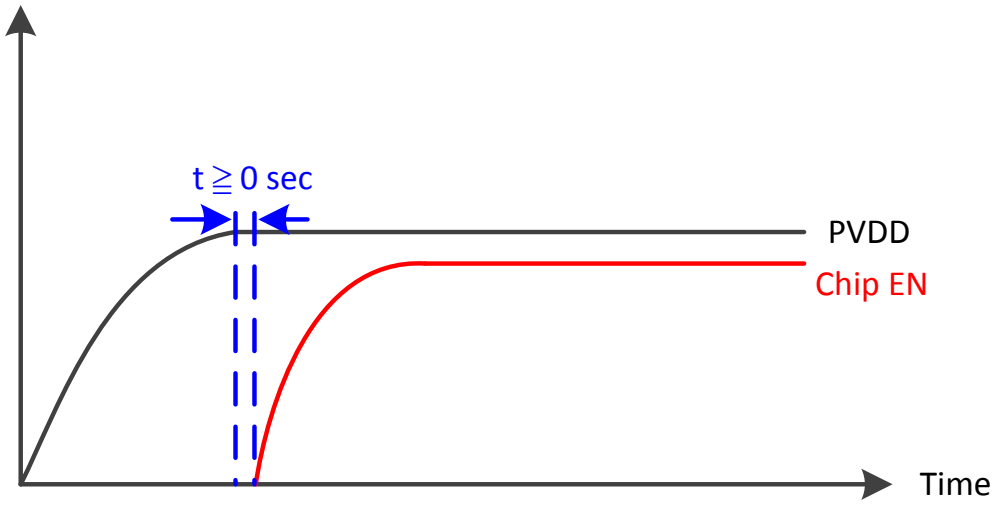
Item	Value	Note
Active Mode Report Rate	120Hz	ILI2520 report Touch ID to ILITEK's I2C to USB Bridge Board.
Report Touch ID Number	10 + (1)	Multiple Virtual Keys Support
I2C SCL Clock Rate	400kHz	Fast mode
I2C Idle Mode	Idle time: 300ms	Support Touch Wake Up function

4.4. I2C AC Characteristics

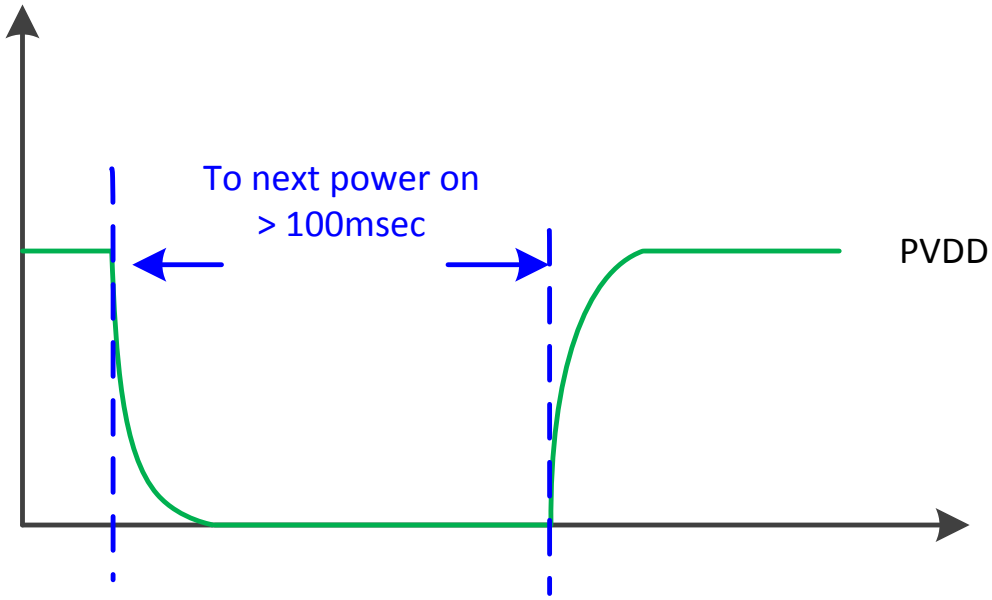


Item	Symbol	100kHz		400kHz		Unit
		Min.	Max.	Min.	Max.	
SCL standard mode clock frequency	FSCL	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock is generated.	THD;STA	4	--	0.6	--	us
LOW period of the SCL clock	TLOW	4.7	--	1.3	--	us
HIGH period of the SCL clock	THIGH	4	--	0.6	--	us
Setup time for a repeat START condition.	TSU;STA	4.7	--	0.6	--	us
Data hold time	THD;DAT	0	3.45	0	0.9	us
Data setup time	TSU;DAT	250	--	100	--	ns
Rising time of both SDA and SCL signals	Tr	--	1000	--	300	ns
Falling time of both SDA and SCL signals	Tf	--	300	--	300	ns
Setup time for STOP condition.	TSU;STO	4	--	0.6	--	us
Free time between STOP and START condition	TBUF	4.7	--	1.3	--	us
Pulse width of spikes which must be suppressed by input filter	TSP	--	--	0	50	ns

4.5. Power On Sequence

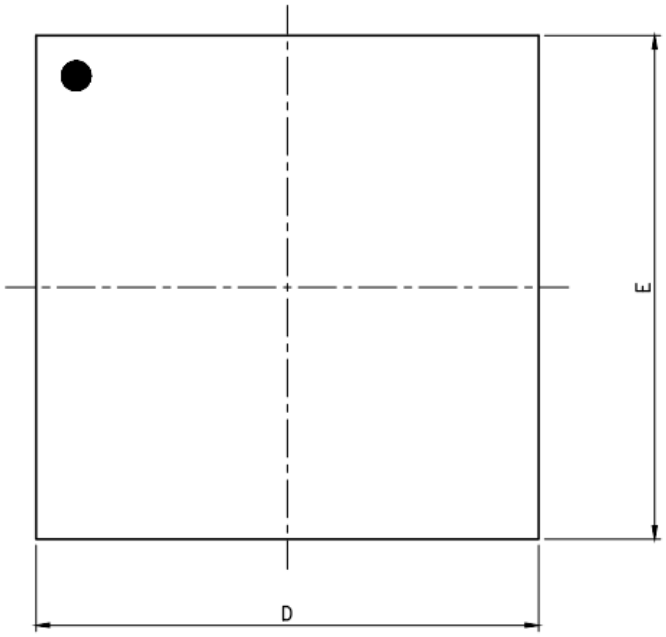


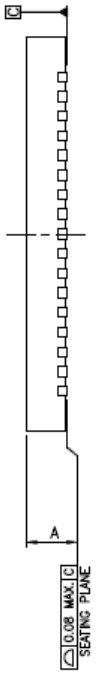
4.6. Power Off to Power On Sequence

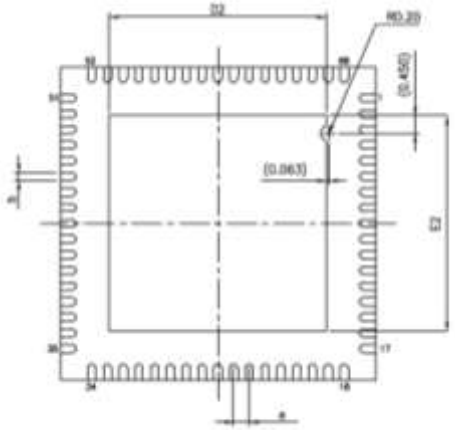


5. Package Information

5.1. QFN-68 Package Dimension



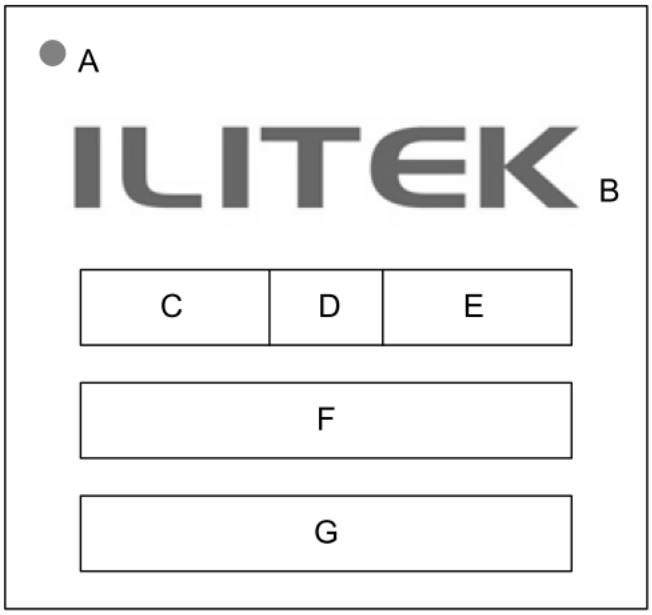




	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X868)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.15	0.20	0.25
D	8.00 BSC		
E	8.00 BSC		
e	0.40 BSC		

PAD SIZE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
236X23* MIL	5.45	5.50	5.55	5.45	5.50	5.55

5.2. Marking Information



Item	Description
A	Pin 1 Indication
B	ILITEK logo
C	IC Model Name: ILI2131A
D	Blank
E	Blank
F	Assembly Lot No.: The code will be updated by production control (1st code is A)
G	Wafer Lot No.: The code will be updated by production control (1st code is A)

6. Revision History

Version No.	Date	Page	Description
V001	2020/03/12	All	Initial release
V002	2020/05/14	8	Recommand Input Voltage