PRODUCT SPECIFICATION

CDTECH Model: **S029GQ07NS**

CUSTOMER Model: -

Description: **2.9” TFT-LCD Module**

Version: **1.0**

CDTECH	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2023.4.18	2023.4.18	2023.4.18

	SIGNATURE	DATE
CUSTOMER APPROVAL		

Record of Revisions

Version	Revise Date	Description	Page
1.0	2023-4-4	First Release	-
	2023-4-18	Update the NOTE 1 of the LCM pin	7

Contents

1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	2.9	inch
Number of Pixels	320 (H) RGB x 120 (V)	pixels
Display Mode	Normally White	-
Viewing Direction	12 o' clock	o' clock
Interface	RGB/MCU/SPI	-
Display Colors	262K	colors
Outline Dimension	76.90 (H) x 38.22 (V) x 3.26 (D)	mm
Active Area	70.08 (H) x 26.28 (V)	mm
Pixel Pitch	0.219 (H) x 0.219 (V)	mm
Driver IC	SSD2119	-
Operation Temperature	-20~70	℃
Storage Temperature	-30~80	℃

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Analog Supply voltage	VDD	-0.3	5.0	V	Note 1
Digital supply voltage	IOVCC	-0.3	3.6	V	Note 1

Note 1:Permanent damage may occur to the LCD module if beyond this specification.
Functional operation should be restricted to the conditions described under normal operating conditions.

3. Elecrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Supply voltage	VDD	2.5	2.8	3.3	V	
Analog supply current	I_{VDD}	-	TBD	-	mA	VDD=2.8V
Logic supply voltage	IOVCC	1.65	1.8	3.3	V	
Logic supply current	I_{IOVCC}	-	TBD	-	mA	IOVCC=1.8V
Logic input voltage	VIH	0.7*IOVCC	-	IOVCC	V	
	VIL	GND	-	0.3*IOVCC	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I_F	-	20	-	mA	
Driving Voltage	V_F	16.2	-	20.4	V	
Power consumption	W_{BL}	0.324	-	0.408	W	
LED Life-Time	N/A	-	50,000	-	Hours	Ta=25℃ Note 1

Note 1:LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :

4. Interface Pin Assignment

4.1 LCM Pin Assignment

Recommended connector：FH12-54S-0.5SH manufactured by HIROSE

No.	Symbol	Description
1	VBL-	Backlight LED Cathode
2	VBL-	Backlight LED Cathode
3	VBL+	Backlight LED Anode
4	VBL+	Backlight LED Anode
5	Y1(YU)	Touch panel up side
6	X1(XR)	Touch panel right side
7	NC	NC
8	RESET	Reset Signal pin (“Low” is enable)
9	CS	Chip select
10	SCL	Serial Clock.
11	SDA	Serial Data Input
12	SDO	Serial Data output
13	WSYNC	Ram write synchronization output. Leave it OPEN when not used
14-19	B0~B5	Data bus
20-21	NC	NC
22-27	G0~G5	Data bus
28-29	NC	NC
30-35	R0~R5	Data bus
36	HSYNC	Line Synchronous Signal
37	VSYNC	Frame Synchronous Signal
38	DOTCLK	Dot-clock signal and oscillator source
39	GND	Ground
40	IOVCC	Voltage input pin for logic
41	VDD	Booster input voltage pin
42	VDD	Booster input voltage pin
43	Y2(YD)	Touch panel down side
44	X2(XL)	Touch panel Left side
45	RS	Data or Command selest PIN
46	RD	6800 system: E(enable signal) 8080 system : RD(read strobe signal) Serial mode: Not use and should be connected to VDDIO or VSS

47	WR	6800 system : RW (indicates read cycle when high ,write cycle when low) 8080 system : WR (wirte strobe signal)
48	PS3	Interface selest PIN （Note 1）
49	PS2	
50	PS1	
51	PS0	
52	DEN	Display enable pin for controller
53	GND	Ground
54	GND	Ground

Note 1:

PS3	PS2	PS1	PS0	Interface Mode
0	0	0	0	16-bit 6800 parallel interface
0	0	0	1	8-bit 6800 parallel interface
0	0	1	0	16-bit 8080 parallel interface
0	0	1	1	8-bit 8080 parallel interface
0	1	0	0	9-bit generic D[17:9] (262k colour) + 3-wire SPI If 65K color, D12 shorts to D17 internally
0	1	0	1	16-bit generic (262k colour) + 3-wire SPI
0	1	1	0	18-bit generic (262k colour) + 3-wire SPI
0	1	1	1	6-bit generic D[17:12] (262k colour) + 3-wire SPI
1	0	0	0	18-bits 6800 parallel interface
1	0	0	1	9-bits 6800 parallel interface
1	0	1	0	18-bit 8080 parallel interface
1	0	1	1	9-bit 8080 parallel interface
1	1	1	0	3-wire SPI
1	1	1	1	4-wire SPI

5. Interface Characteristics

5.1 DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDDIO	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.4	-	3.6	V
VCI	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO whichever is higher	-	3.6	V
VGH	Gate driver High Output Voltage Booster efficiency	No panel loading; 4x or 5x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	88	90	-	%
		No panel loading; 6x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	82	84	-	%
VCIX2	VCIX2 primary booster efficiency	No panel loading, ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	83	85	-	%
VGH	Gate driver High Output Voltage		9	-	18	V
VGL	Gate driver Low Output Voltage		-15	-	-6	V
VcomH	Vcom High Output Voltage		V_{CI} + 0.5	-	5	V
VcomL	Vcom Low Output Voltage		$-V_{CIM}$+0.5	-	-1	V
VLCD63	Max. Source Voltage		-	-	6	V
ΔVLCD63	Source voltage variation		-2		2	%
V_{OH1}	Logic High Output Voltage	Iout=-100μA	0.9* VDDIO	-	VDDIO	V
V_{OL1}	Logic Low Output Voltage	Iout=100μA	0	-	0.1*VDDIO	V
V_{IH1}	Logic High Input voltage		0.8*VDDIO	-	VDDIO	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*VDDIO	V
I_{OH}	Logic High Output Current Source	Vout = V_{DDIO}-0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	μA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	μA

5.2 AC Electrical Characteristics

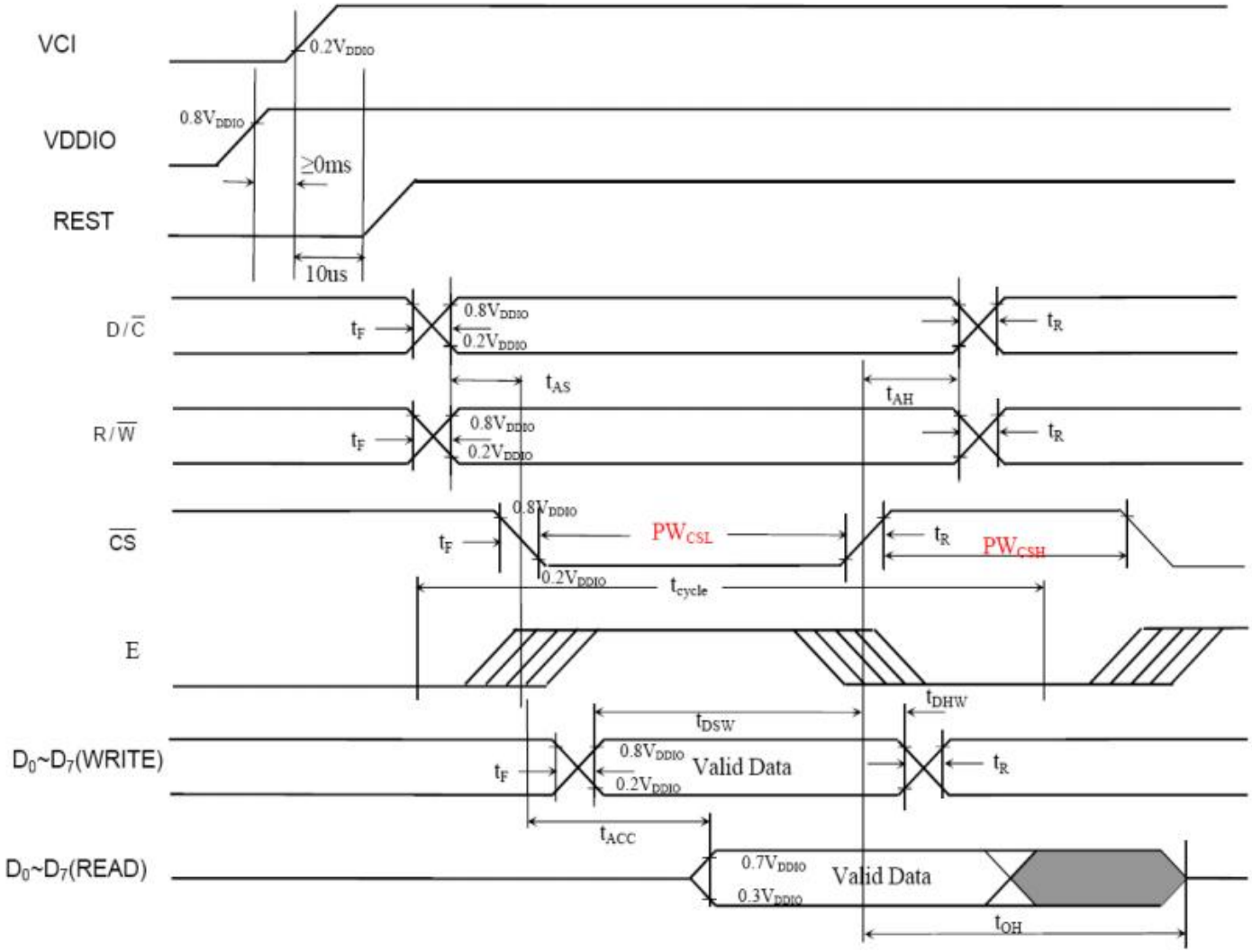
5.2.1 Parallel 6800-series Interface Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	1000	-	-	ns
t_{AS}	Address Setup Time ($R/\overline{W}$)	0	-	-	ns
t_{AH}	Address Hold Time ($R/\overline{W}$)	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time (/CS)	-	-	4	ns
t_F	Fall time (/CS)	-	-	4	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Parallel 6800-series Interface Timing Characteristics


VCI
0.2VDDIO
0.8VDDIO
VDDIO
≥0ms
REST
10us
D/C
tF
0.8VDDIO
0.2VDDIO
tR
tAS
tAH
R/W
CS
PWCSL
PWCSH
tcycle
E
tDHW
tDSW
D0~D7(WRITE)
Valid Data
tACC
D0~D7(READ)
0.7VDDIO
0.3VDDIO
tOH

5.2.2 Parallel 6800-series Interface Timing Characteristics

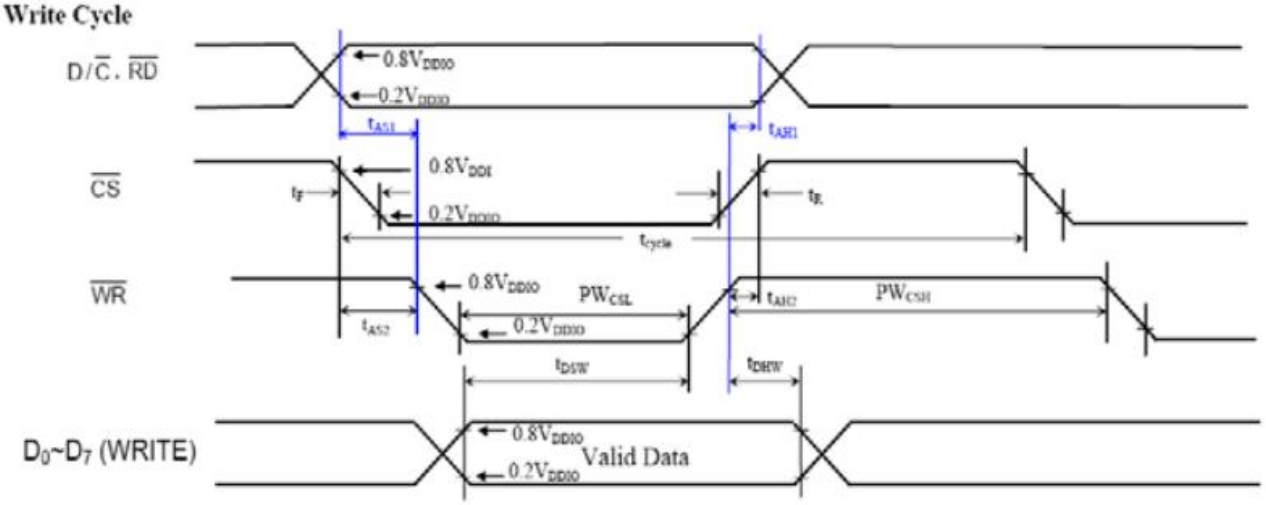
Parallel 8080 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CH}	Chip Select Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	100	-	-	ns
t_{ACC}	Access Time (RAM) Access Time (command)	250 250	- -	- -	ns ns
t_{PWLR} t_{PWLR} t_{PWLW}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	500 500 50	- - -	- - -	ns ns ns
t_{PWHR} t_{PWHW}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	500 50	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

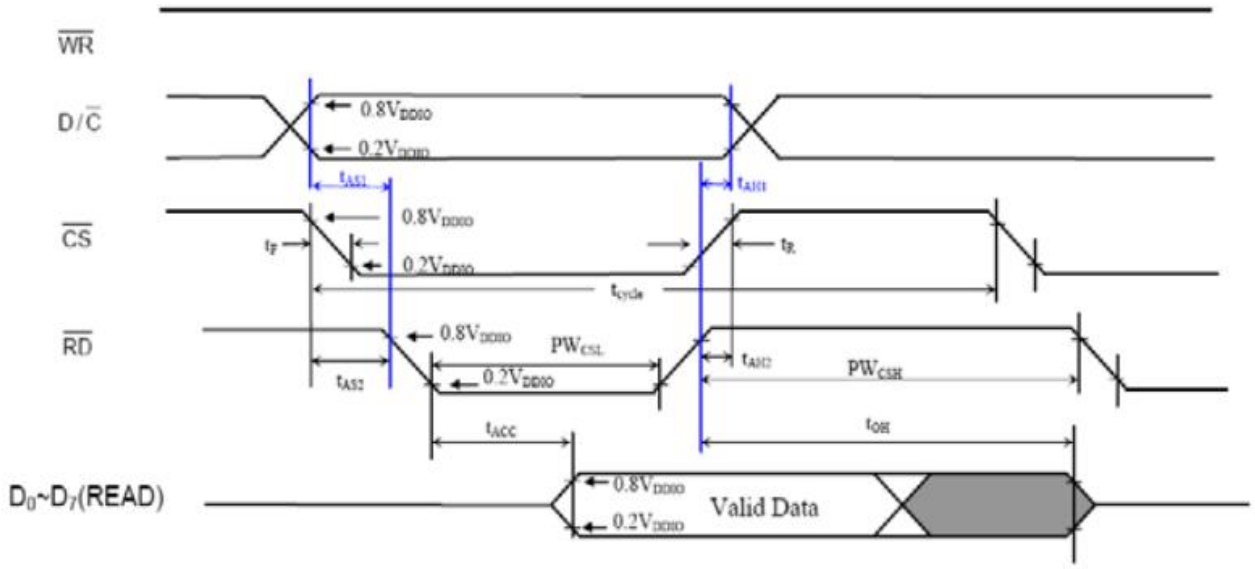
8080-series parallel interface characteristics (Form 1: /CS low pulse width > W/ R low pulse width)

Write Cycle



Remark: It's highly recommended that $\overline{RD}$ remains high for the whole write cycle

Read Cycle

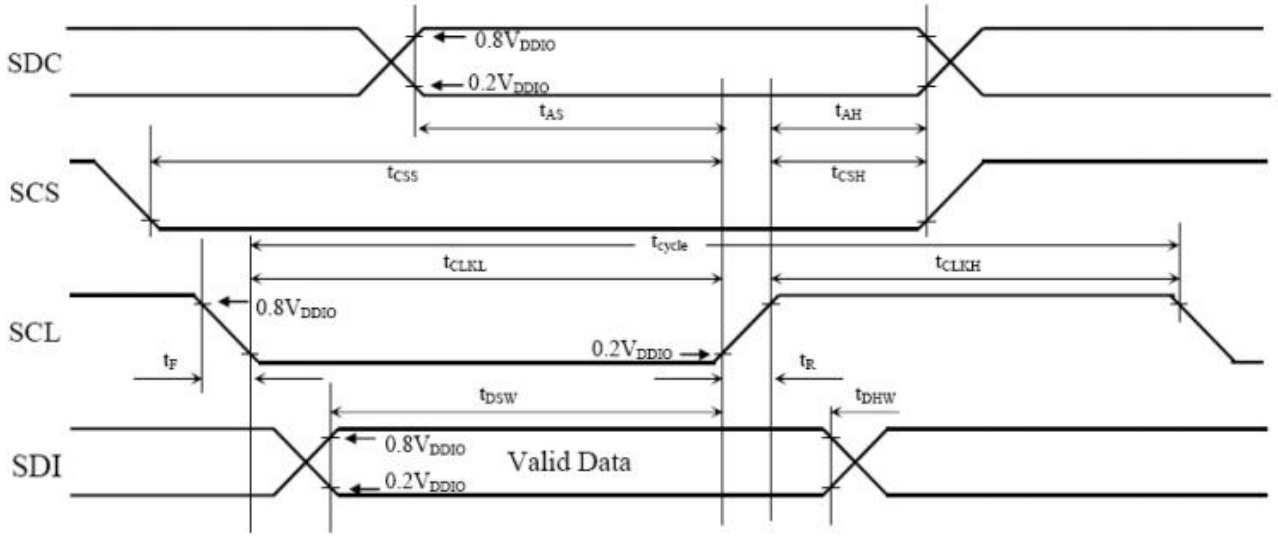


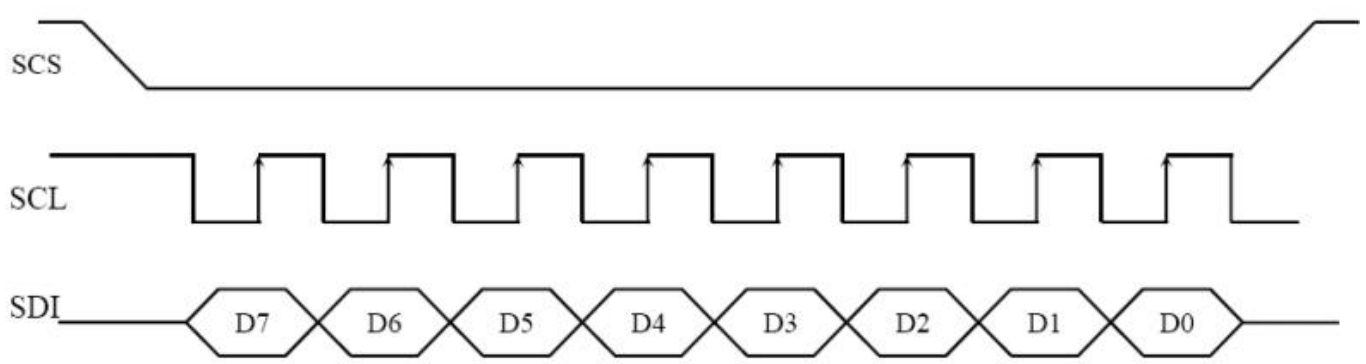
5.2.3 Serial Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

4 wire Serial Timing Characteristics





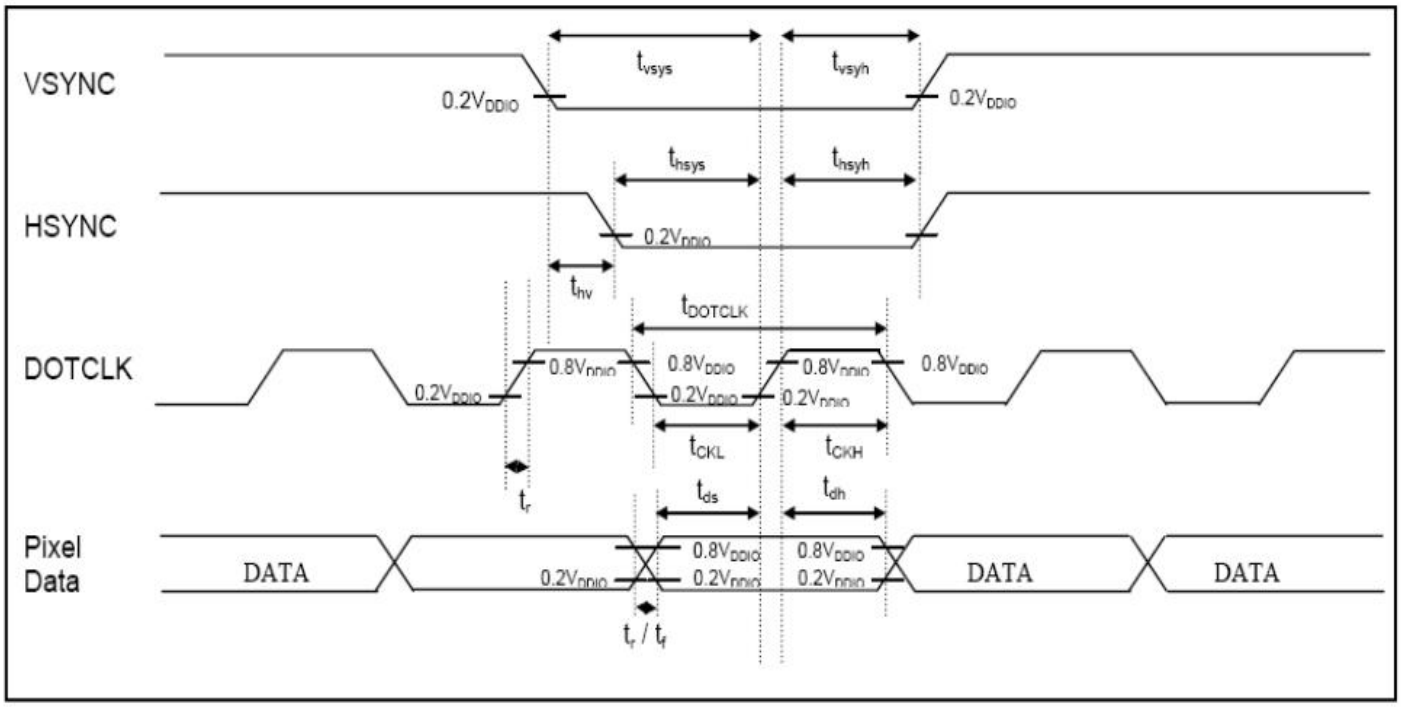
5.2.4 RGB Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

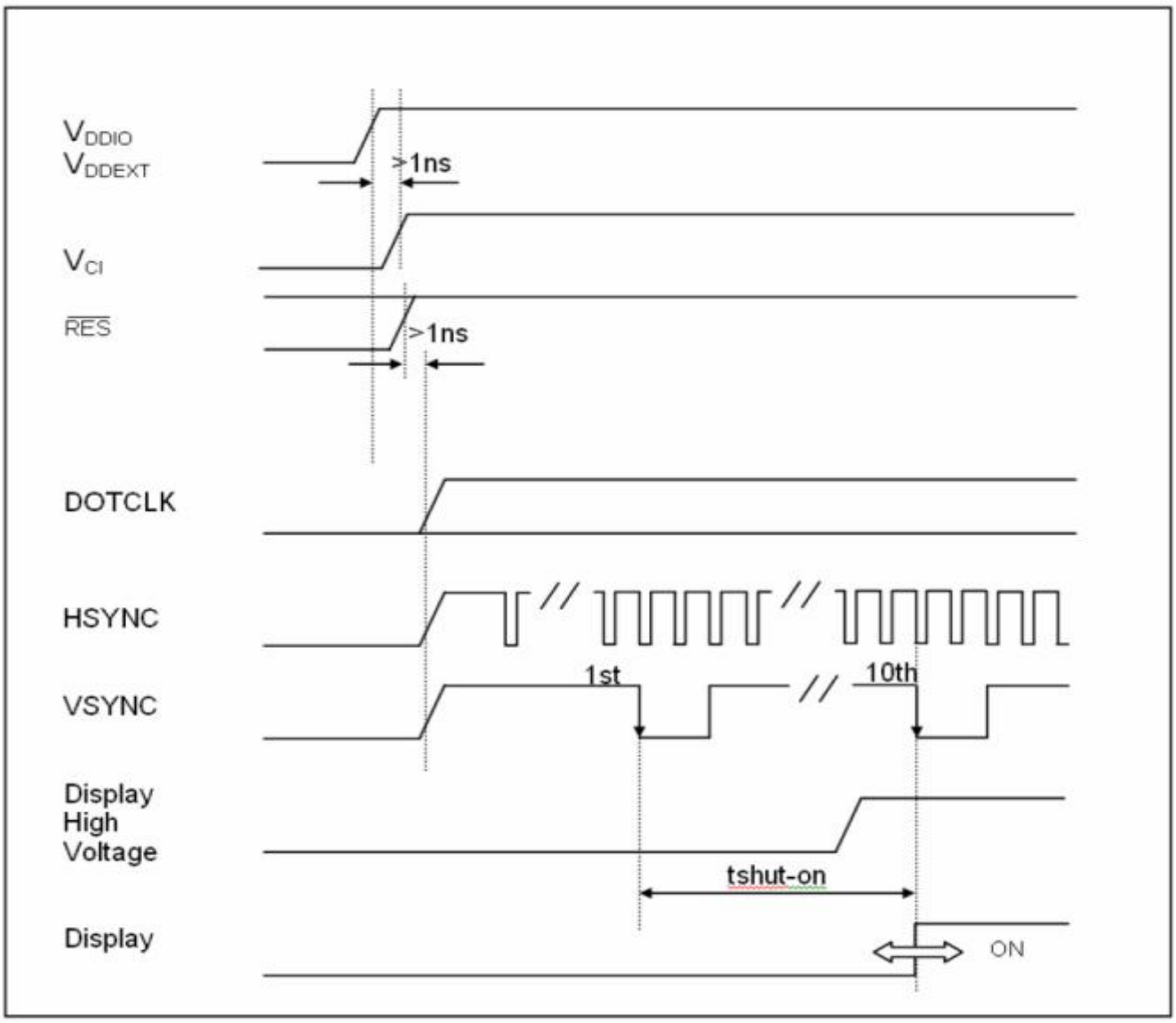
Symbol	Parameter	Min	Typ	Max	Unit
f_{DOTCLK}	DOTCLK Frequency (70Hz frame rate)	1	5.5	8.2	MHz
t_{DOTCLK}	DOTCLK Period	122	182	1000	us
t_{VSYS}	Vertical Sync Setup Time	20	-	-	ns
t_{VSYH}	Vertical Sync Hold Time	20	-	-	ns
t_{HSYS}	Horizontal Sync Setup Time	20	-	-	ns
t_{HSYH}	Horizontal Sync Hold Time	20	-	-	ns
t_{HV}	Phase difference of Sync Signal Falling Edge	0	-	320	t_{DOTCLK}
t_{CLK}	DOTCLK Low Period	61	-	-	ns
t_{CKH}	DOTCLK High Period	61	-	-	ns
t_{DS}	Data Setup Time	25	-	-	ns
t_{DH}	Data hold Time	25	-	-	ns
t_{RES}	Reset pulse width	8			ns

Note: External clock source must be provided to DOTCLK pin of SSD2119. The driver will not operate in absence of the clocking signal.

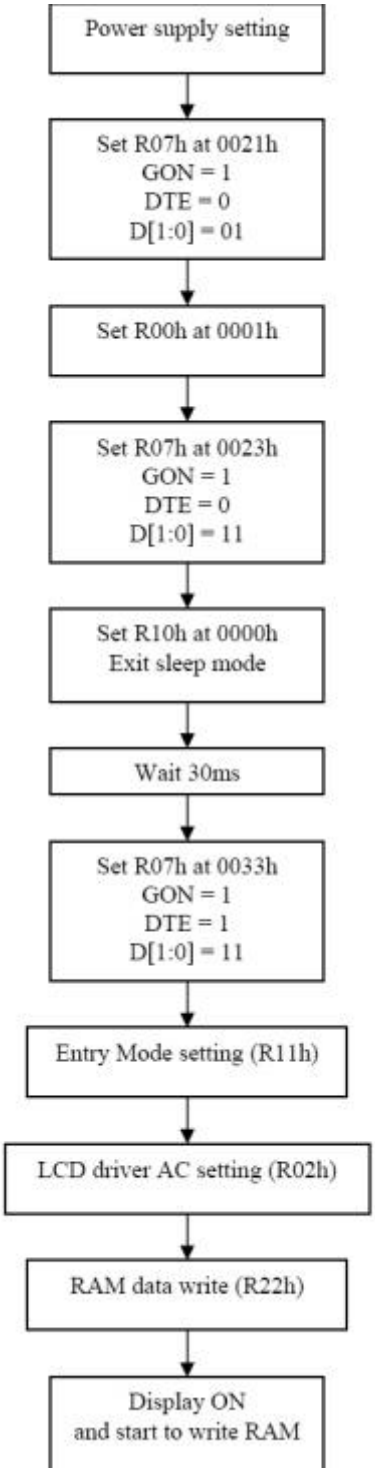
RGB Timing Characteristics



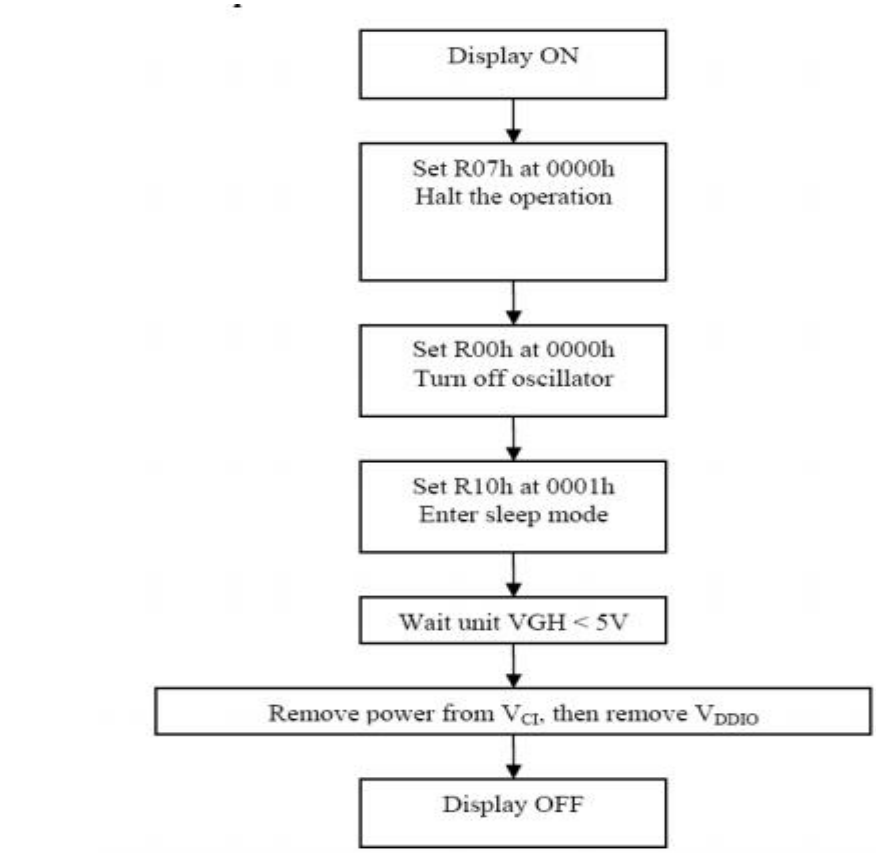
5.3 Power on sequence

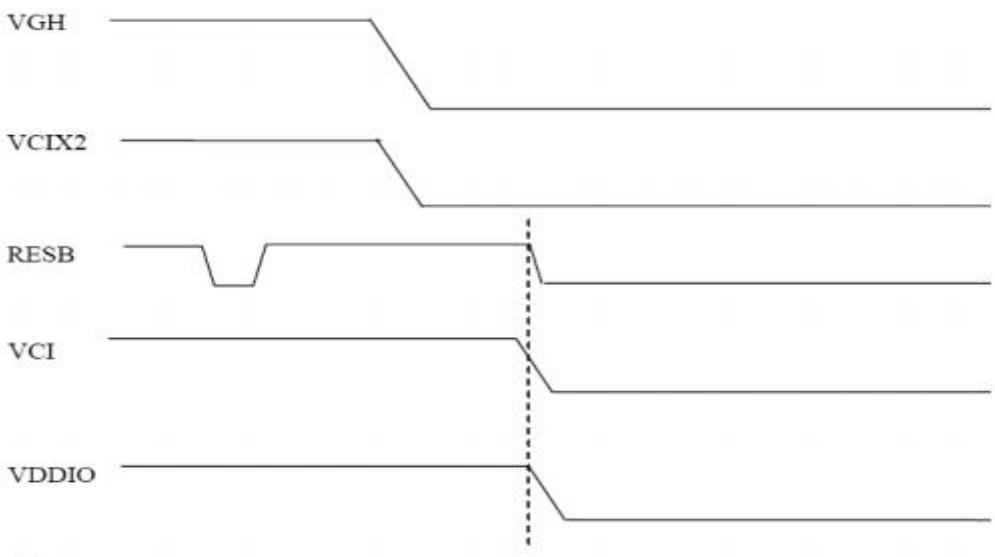


5.4 Display on sequence



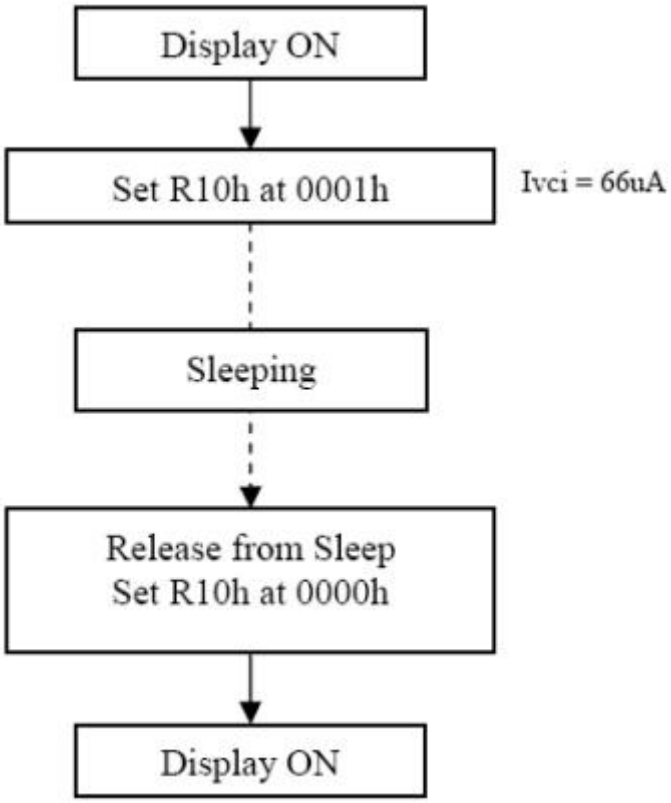
5.5 Display off sequence





Note:
1. VDDIO should be the last to fall, or VCI/VDDIO could be power off at the same time
2. If OTP is active in the application, the OTP programming voltage should be turned off and cap

5.6 Sleep mode display sequence



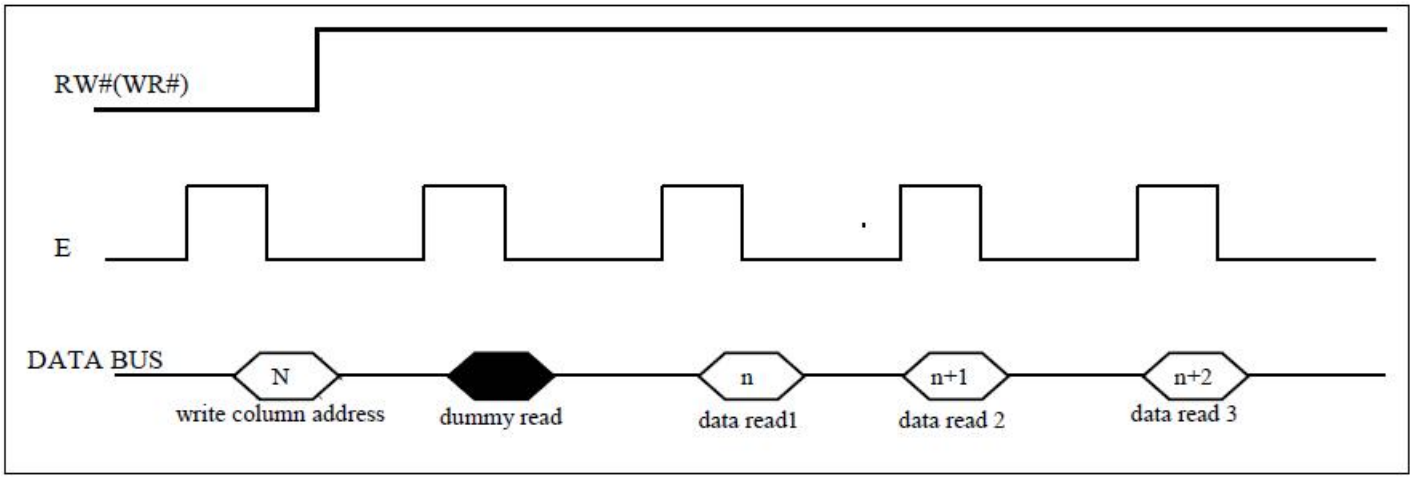
5.7 Interface

5.7.1 MPU Parallel 6800-series Interface

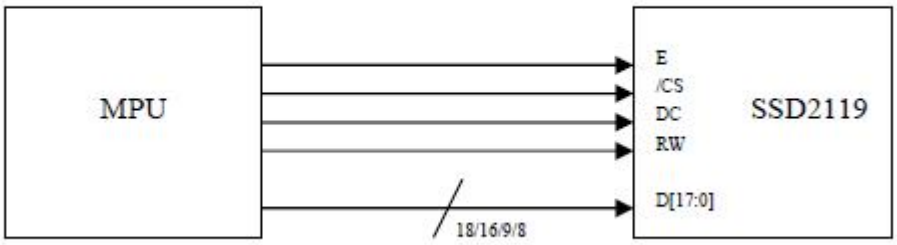
MPU Parallel 6800-series Interface

The parallel Interface consists of 18 bi-directional data pins D[17:0], RW, DC, E and CS.
RW input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or status register. RW input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of DC input.
The E input served as data latch signal (clock) when high provided that CS is low. Please refer to Parallel Interface Timing Diagram of 6800-series microprocessors.
In order to match the operating frequency of the GDDRAM with that of the MCU, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

Figure 7-1: Read Display Data



6800-series System Bus Interface



PS3	PS2	PS1	PS0	Interface Mode	Data bus	RW	E	DC	/CS	Operation
0	0	0	0	16-bit 6800 parallel interface	D[17:10], D[8:1]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 16-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 16-bit display data
0	0	0	1	8-bit 6800 parallel interface	D[17:10]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 8-bit display data
1	0	0	0	18-bits 6800 parallel interface	D[17:0]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 18-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 18-bit display data
1	0	0	1	9-bits 6800 parallel interface	D[17:9]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 9-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 9-bit display data

* A dummy read is required before the first actual display data read

5.7.2 MPU Parallel 8080-series Interface

MPU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins D[17:0], WR, DC, and CS.
RD input served as data read latch signal (clock) when low provided that CS is low. Weather reading the display data from GDDRAM or reading the status from the status register is controlled by DC. WR input served as data write latch signal (clock) when low provided that CS is low. Weather writing the display data to the GDDRAM or writing the command to the command register is controlled by DC. A dummy read is also required before the first actual display data read for 8080-series interface. Please refer to .

8080-series System Bus Interface

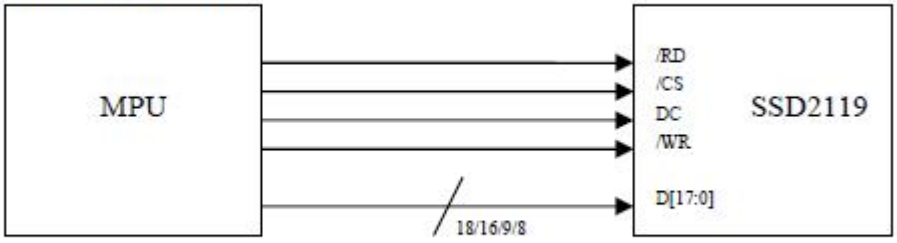


Table 15-3: The Function of 8080-series parallel interface

PS3	PS2	PS1	PS0	Interface Mode	Data bus	/WR	/RD	DC	/CS	Operation
0	0	1	0	16-bit 8080 parallel interface	D[17:10], D[8:1]	1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 16-bit display data
0	0	1	1	8-bit 8080 parallel interface	D[17:10]	1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 8-bit display data
1	0	1	0	18-bit 8080 parallel interface	D[17:0]	0	1	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 18-bit display data
1	0	1	1	9-bit 8080 parallel interface	D[17:9]	1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 9-bit display data

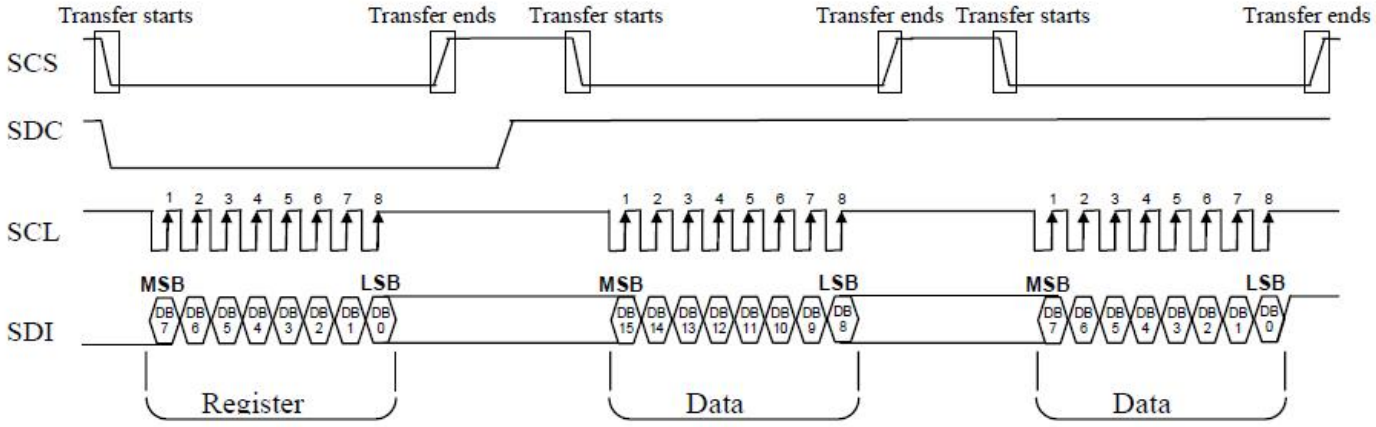
* A dummy read is required before the first actual display data read

5.7.3 4-wire Serial Peripheral Interface (8 bits)

4-wire Serial Peripheral Interface (8 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (SCS), serial transfer clock line (SCL), serial input data (SDI). The serial data transfer starts at the falling edge of SCS input and ends at the rising edge of SCS.
SDC determinates the data of SDI which is register or data.

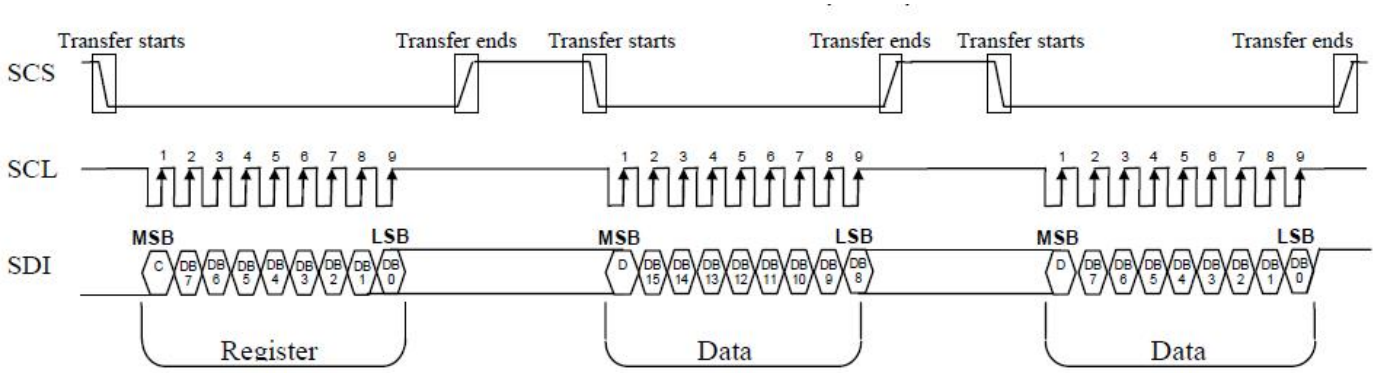
Figure 7-2: 4-wire SPI interface (8 bits)



5.7.4 3-lines Serial Peripheral interface

3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while SDC is not use. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: DC bit, D7 to D0 bit. The DC bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (DC bit = 1) or the command register (DC bit = 0).



5.7.5 RGB Interface

RGB Interface

SSD2119 supports RGB interface. RGB interface unit consists of D[17:0], HSYNC, VSYNC, DOTCLK and DEN signals for display moving pictures. When the RGB interface is selected, the display operation is synchronized with external control signals (HSYNC, VSYNC and DOTCLK). Data is written in synchronization with the control signals when DEN is enabled for write operation in order to avoid flicker or tearing effect while updating display data.

5.8 Command list

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R00h	Oscillation Start	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	GD	BGR	SM	TB	0	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
	(3AEFh)			0	0	1	1	1	0	1	0	1	1	1	0	1	1	1	1
R02h	LCD drive AC control	0	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	All GAMAS[2:0] setting 8 color (6A64h)			0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
	(5308h)			0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0004h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
R0Fh	Gate scan start position	0	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R10h	Sleep mode	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R11h	Entry mode	0	1	VS mode	DFM1	DFM0	0	Denmode	WMode	Nosync	DMode	TY1	TY0	ID1	ID0	AM	0	0	0
	(6230h)			0	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0

R12h	Sleep mode	0	1	0	0	DSLP	0	1	1	0	1	1	0	0	1	1	0	0	1
	(0D99h)			0	0	0	0	1	1	0	1	1	0	0	1	1	0	0	1
R15h	Entry mode	0	1	1	0	1	1	0	0	0	0	0	0	0	1	INVDOT	INVDEN	INVHS	INVVS
	(B010h)			1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0
R16h	Horizontal Porch	0	1	0	0	0	0	0	0	0	0	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(001Dh)			0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
R17h	Vertical Porch	0	1	VFP7	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0003h)			0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R20h	Uniformity	0	1	1	0	1	1	0	0	0	0	1	1	ENSVIN	0	1	0	1	1
	(B0EBh)			1	0	1	1	0	0	0	0	1	1	1	0	1	0	1	1
R22h	RAM data write	0	1	Data[17:0] mapping depends on the interface setting															
	RAM data read	1	1																
R25h	Frame Frequency	0	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
	(8000h)			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R26h	Analogue Setting	0	1	0	RW_T	VCB	RLTM	ENN	0	0	0	0	0	0	0	0	0	0	0
	(3800h)			0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
R28h	VCOM OTP (000Ah)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R29h	VCOM OTP (80C0h)	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00

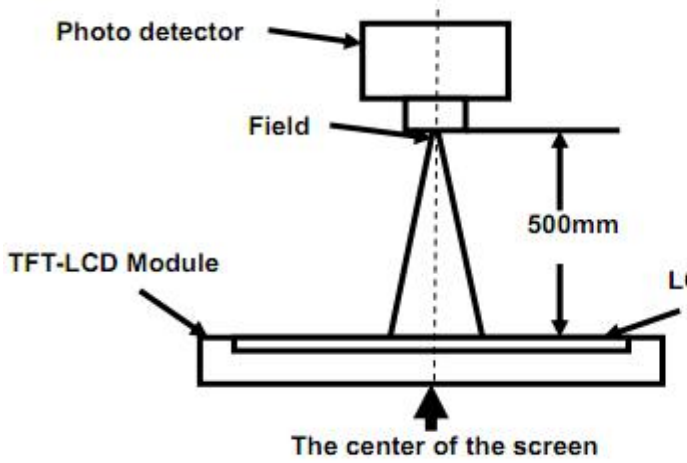
R41h	Vertical scroll control (1)	0	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R42h	Vertical scroll control (2)	0	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R44h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	(EF00h)			1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
R45h	Horizontal RAM address start position	0	1	0	0	0	0	0	0	0	HSA8	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	Horizontal RAM address end position	0	1	0	0	0	0	0	0	0	HEA8	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R48h	First window start	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	First window end	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Ah	Second window start	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	Second window end	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Eh	Set GDDRAM X address counter	0	1	0	0	0	0	0	0	0	XAD8	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	Set GDDRAM Y address counter	0	1	0	0	0	0	0	0	0	0	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	Φ=90°(12 o'clock)	45	55	-	deg	Note2
	θ_B	Φ=270°(6 o'clock)	55	65	-	deg	Note2
	θ_L	Φ=180°(9 o'clock)	55	65	-	deg	Note2
	θ_R	Φ=0°(3 o'clock)	55	65	-	deg	Note2
Response Time	T_{ON}	Normal θ=Φ=0°	-	25	-	msec	Note4
	T_{OFF}		-	25	-	msec	Note4
Contrast Ratio	CR		-	TBD	-	-	Note1 Note3
Color Chromaticity	W_X		0.256	0.306	0.356	-	Note1 Note5
	W_Y		0.291	0.341	0.391	-	Note1 Note5
Luminance	L		250	300	-	cd/m²	Note1 Note7
Luminance Uniformity	Y_U		75	80	-	%	Note1 Note6
NTSC	-		-	50	-	%	-

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2:Definition of viewing angle range and measurement system
Viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

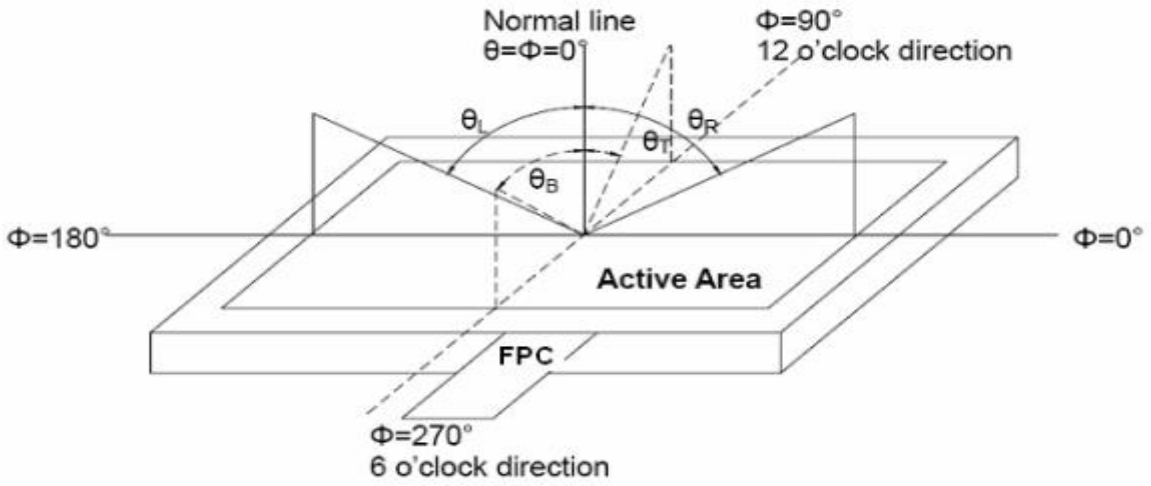


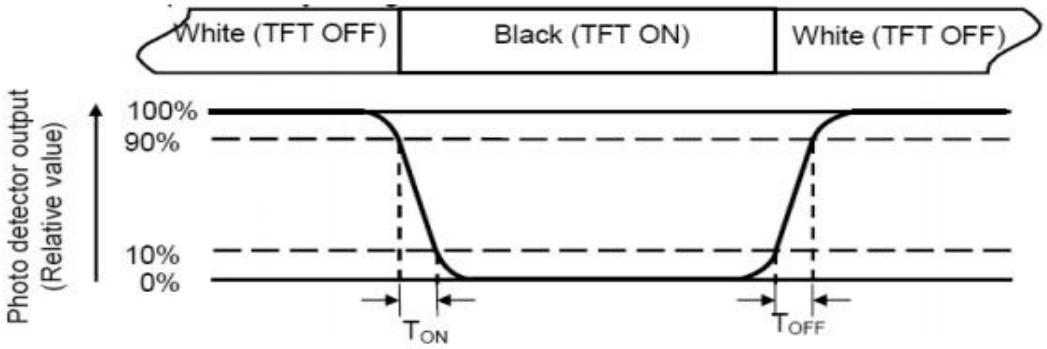
Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5:Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6:Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

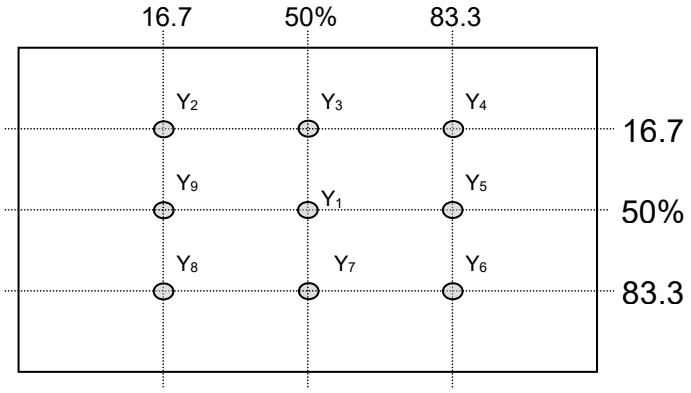


Fig. 2 Definition of points

Note 7:Definition of Luminance (Refer Fig. 2)

Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn).

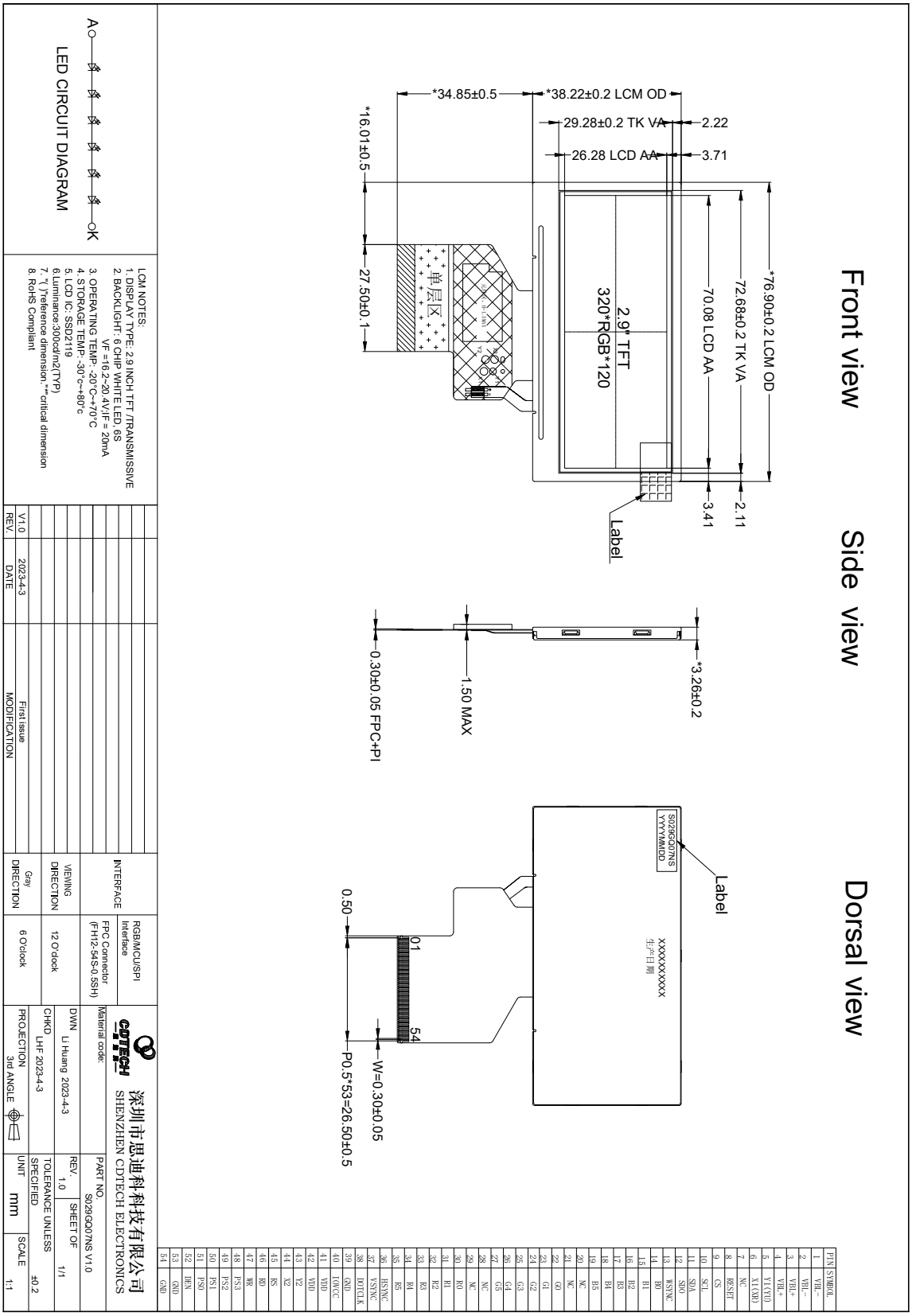
7. Reliability Test Items

Test Item	Test Conditions	
High Temperature Storage	Ta= +80℃	96hrs
Low Temperature Storage	Ta= -30℃	96hrs
High Temperature Operation	Ta= +70℃	96hrs
Low Temperature Operation	Ta= -20℃	96hrs
High Temperature and Humidity Storage	Ta= +60℃, 90% RH	96hrs
Thermal Shock (Non-operation)	-30℃/30 min ~ +80℃/30 min for 20 cycles Start with cold temperature end with high temperature	
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF	
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.	
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction	
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

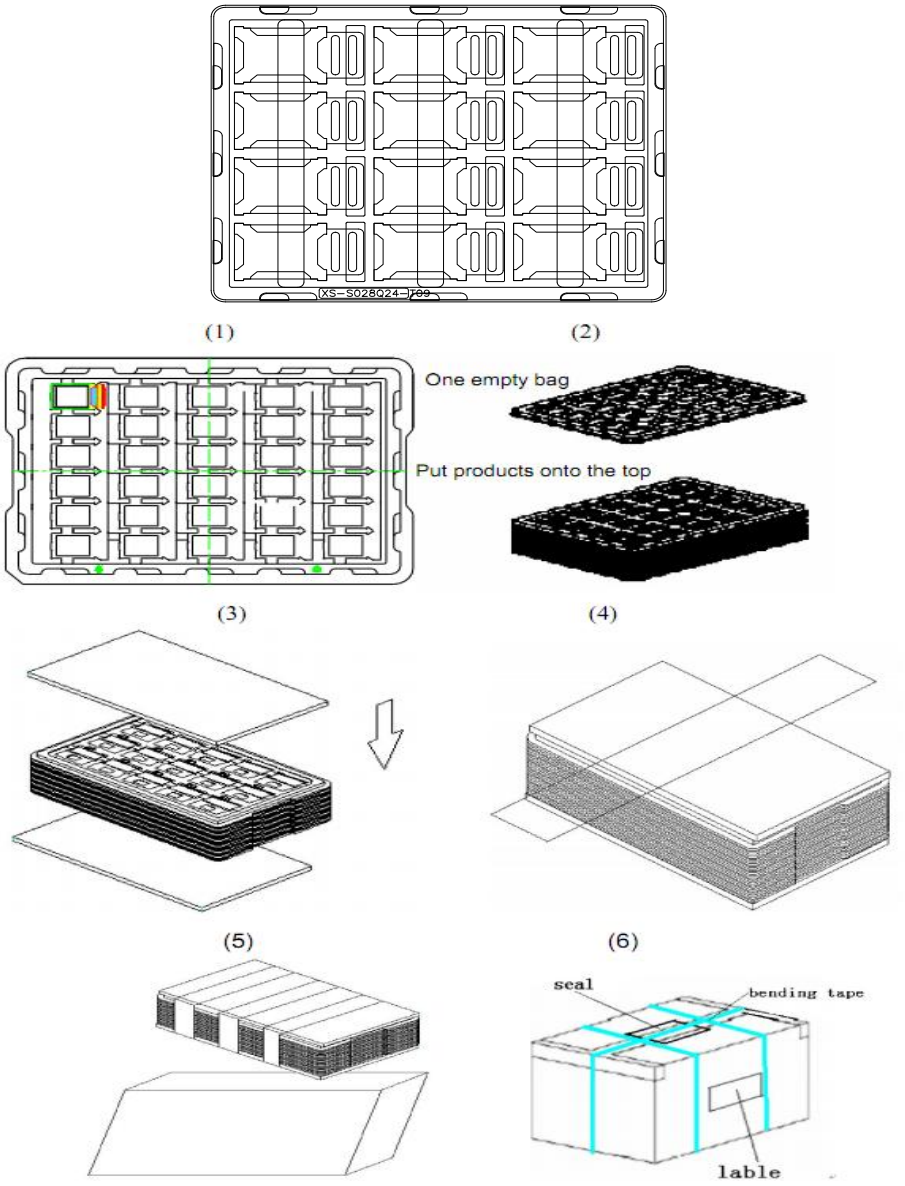
1). Air bubble in the LCD
2). Seal leak or Glass crack
3). Non display or abnormal display
4). Brightness reduction >50%

8. Mechanical Drawing



9. Packing

Packing Method



Steps:

1. Put module into tray cavity
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above
4. Fix the cardboard to the tray stack with adhesive tape
5. Put the tray stack into carton
6. Carton sealing with adhesive tape

10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1.When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2.The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time,the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3.The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.