NewVision

NV3035 Data Sheet

960X240 TFT LCD Single Chip Digital Driver

Preliminary Version 0.3
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Contents

1. General Description

NV3035 is a single chip digital driver for 320RGB×240 dot color TFT-LCD panels. It contains 960 channels source driver and 240 channels gate driver with timing controller and build-in power circuits.

The NV3035 incorporates 8-bit serial and 24-bit parallel RGB interface to receive digital display data. It generates 64-level gamma-corrected gray scale voltages and supports maximum 16M colors display with dithering function. The system function control commands can be set by using 3-wire serial peripheral interface.

NV3035 is designed for wide voltage supply range and small output deviation for better display quality. With advanced design, the NV3035 incorporates special designed architecture to achieve lower power dissipation, making this driver best suitable for small or mid sized portable devices such as cell phones, PDAs, mobile TV devices, etc.

2. Features

- One-Chip solution for 960×240 dot TFT LCD Driver
- 8-bit resolution 256 gray scale with Dithering
- **8-bit/24-bit digital(RGB) data interface**
- 3-Wire SPI for parameters programming
- **1.8~3.6V power supply for I/O circuits**
- 3.0~3.6V power supply for charge pump circuits
- Build-in 1.8V LDO for internal circuits
- Build-In DC-DC for power circuits (VGH/VGL/VCOMAC/VCOMDC voltage supply)
- Configurable color filter type for both Delta and Stripe type
- Operating frequency: 30MHz(max)
- Right/Left shift, Up and Down scan function selectable
- One Line / Two Line / Frame Inversion driving method selectable
- Support Cs on Common structure
- Build-In PWM circuit for LED Back-light
- Stand-by mode for super low power consumption
- Built-in Auto Test Pattern
- **OTP trimming for VCOMAC/VCOMDC with internal burning supply**
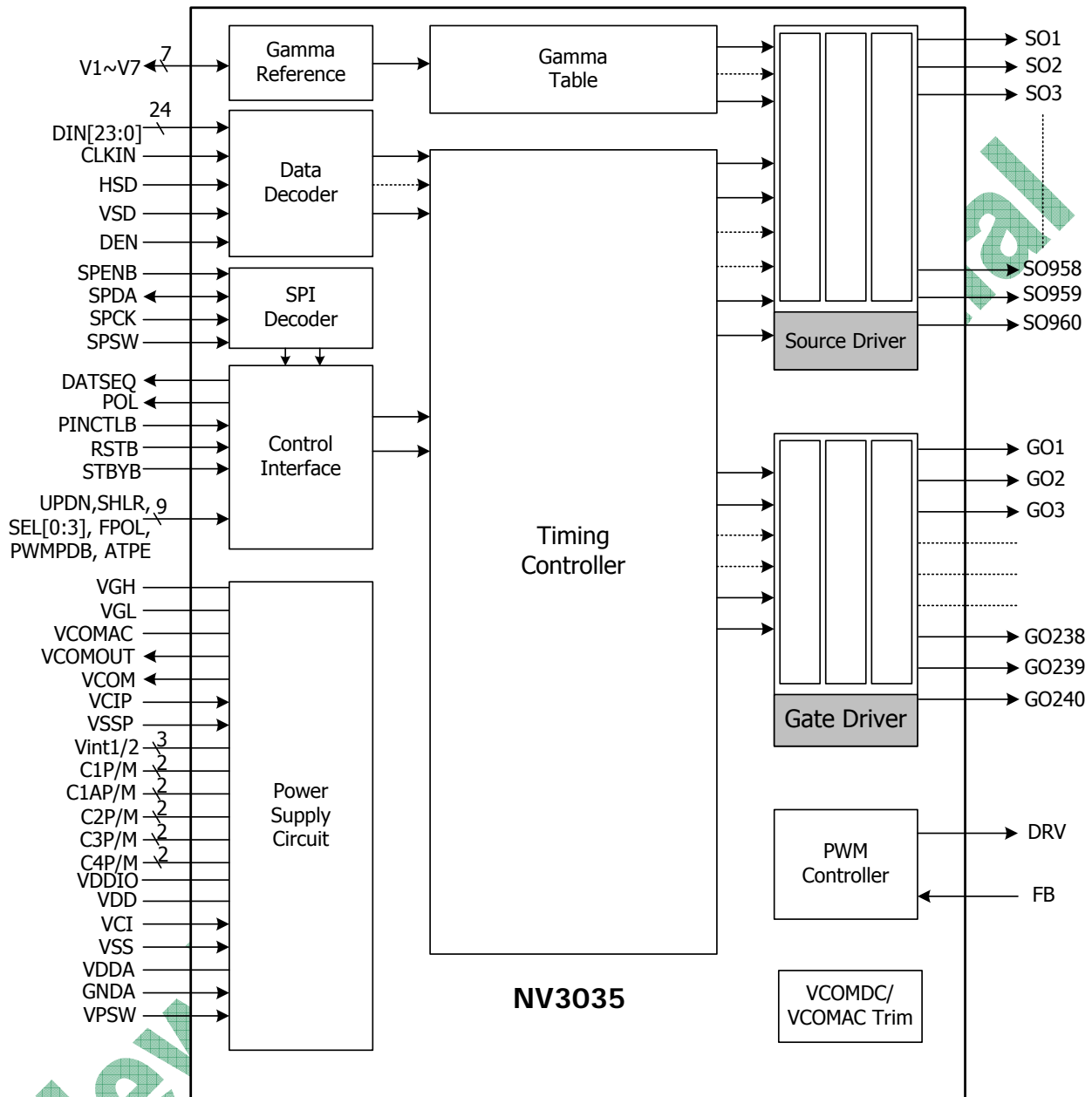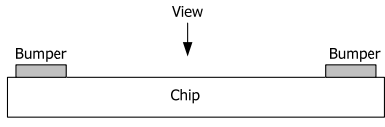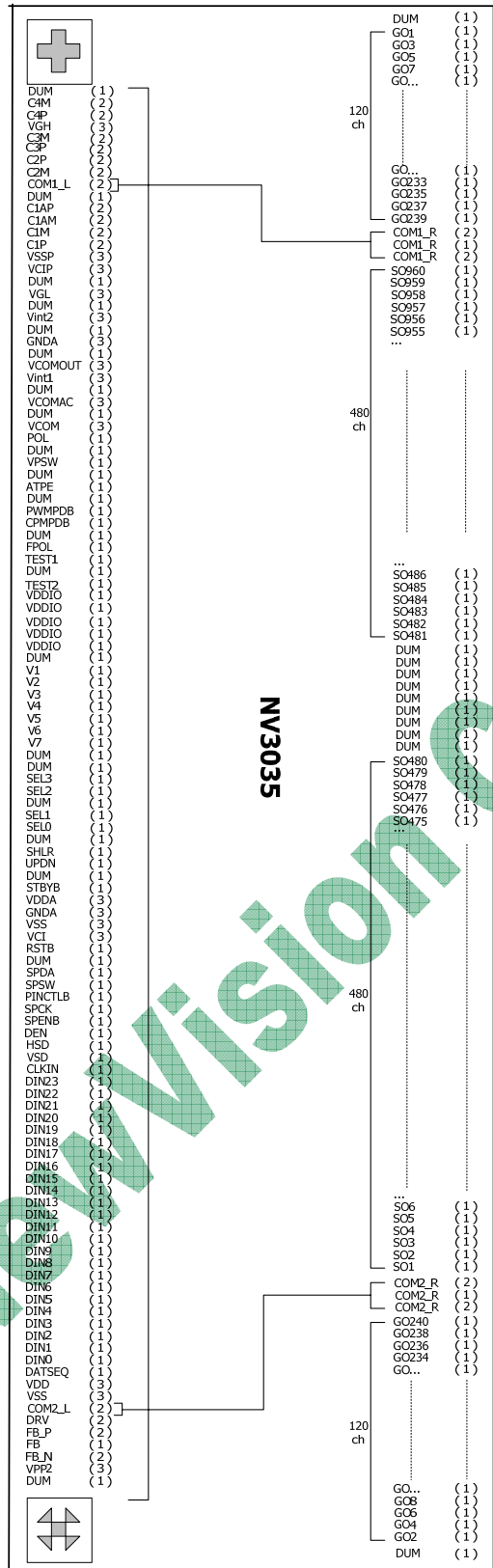- COG package

3. Block Diagram

Fig1.Block diagram

4. Pad Description

4.1 Pad Sequence (Bump Side)

Left side pad list (top to bottom):

Pad	
DUM	(1)
C4M	(2)
C4P	(2)
VGH	(3)
C3M	(2)
C3P	(2)
C2P	(2)
C2M	(2)
COM1_L	(2)
DUM	(1)
C1AP	(2)
C1AM	(2)
C1M	(2)
C1P	(2)
VSSP	(3)
VCIP	(3)
DUM	(1)
VGL	(3)
DUM	(1)
Vint2	(3)
DUM	(1)
GNDA	(3)
DUM	(1)
VCOMOUT	(3)
Vint1	(3)
DUM	(1)
VCOMAC	(3)
DUM	(1)
VCOM	(3)
POL	(1)
DUM	(1)
VPSW	(1)
DUM	(1)
ATPE	(1)
DUM	(1)
PWMPDB	(1)
CPMPDB	(1)
DUM	(1)
FPOL	(1)
TEST1	(1)
DUM	(1)
TEST2	(1)
VDDIO	(1)
VDDIO	(1)
VDDIO	(1)
VDDIO	(1)
VDDIO	(1)
DUM	(1)
V1	(1)
V2	(1)
V3	(1)
V4	(1)
V5	(1)
V6	(1)
V7	(1)
DUM	(1)
DUM	(1)
SEL3	(1)
SEL2	(1)
DUM	(1)
SEL1	(1)
SEL0	(1)
DUM	(1)
SHLR	(1)
UPDN	(1)
DUM	(1)
STBYB	(1)
VDDA	(3)
GNDA	(3)
VSS	(3)
VCI	(3)
RSTB	(1)
DUM	(1)
SPDA	(1)
SPSW	(1)
PINCTLB	(1)
SPCK	(1)
SPENB	(1)
DEN	(1)
HSD	(1)
VSD	(1)
CLKIN	(1)
DIN23	(1)
DIN22	(1)
DIN21	(1)
DIN20	(1)
DIN19	(1)
DIN18	(1)
DIN17	(1)
DIN16	(1)
DIN15	(1)
DIN14	(1)
DIN13	(1)
DIN12	(1)
DIN11	(1)
DIN10	(1)
DIN9	(1)
DIN8	(1)
DIN7	(1)
DIN6	(1)
DIN5	(1)
DIN4	(1)
DIN3	(1)
DIN2	(1)
DIN1	(1)
DIN0	(1)
DATSEQ	(1)
VDD	(3)
VSS	(3)
COM2_L	(2)
DRV	(2)
FB_P	(2)
FB	(2)
FB_N	(2)
VPP2	(3)
DUM	(1)

Center label: **NV3035**

Right side pad list (top to bottom):

Pad	
DUM	(1)
GO1	(1)
GO3	(1)
GO5	(1)
GO7	(1)
GO...	(1)

120 ch

Pad	
GO...	(1)
GO233	(1)
GO235	(1)
GO237	(1)
GO239	(1)
COM1_R	(2)
COM1_R	(2)
COM1_R	(2)
SO960	(1)
SO959	(1)
SO958	(1)
SO957	(1)
SO956	(1)
SO955	(1)
...	

480 ch

Pad	
...	
SO486	(1)
SO485	(1)
SO484	(1)
SO483	(1)
SO482	(1)
SO481	(1)
DUM	(1)
DUM	(1)
DUM	(1)
DUM	(1)
DUM	(1)
DUM	(1)
DUM	(1)
DUM	(1)
SO480	(1)
SO479	(1)
SO478	(1)
SO477	(1)
SO476	(1)
SO475	(1)
...	

480 ch

Pad	
...	
SO6	(1)
SO5	(1)
SO4	(1)
SO3	(1)
SO2	(1)
SO1	(1)
COM2_R	(2)
COM2_R	(2)
COM2_R	(2)
GO240	(1)
GO238	(1)
GO236	(1)
GO234	(1)
GO...	(1)

120 ch

Pad	
GO...	(1)
GO8	(1)
GO6	(1)
GO4	(1)
GO2	(1)
DUM	(1)

View ↓

Bumper   Bumper

Chip

4.2 Pad Description:

Designation	I/O	Description
DIN[23..0]	I	Data Input. 8-bit mode: DIN7:MSB; DIN0:LSB; the remainder should be connect to GND. 24-bit mode: DIN[7:0]=R[7:0] data; DIN[15:8]=G[7:0] data; DIN[23:16]=B[7:0] data. For 18bit RGB interface, connect two LSB bits of all the R/G/B data bus to GND.
CLKIN	I	Clock for Input Data. Data latched at rising/falling edge of this signal. Default positive edge latch data.
HSD	I	Horizontal Sync input. Default Negative polarity, can be change by HSDPOL register.
VSD	I	Vertical Sync input. Default Negative polarity, can be change by VSDPOL register.
DEN	I (Pull Low)	Data Input Enable. Active High to enable the data input Bus under "DE Mode". Normally pull low.
DATSEQ	O	Data sequence control pin for external T-CON. Output "1": for Odd line, "0": for Even line
POL	O	Frame polarity output. Amplitude of signal is from 0V to 3.3V
V1~V7	I/O	Gamma correction reference voltage. When VSET="1" is used. The voltage of pins V1~V7 must be swing and must be AVDD-0.1V>V1>V2>V3 V5>V6>V7>AGND+0.1V when POL="1" and AGND+0.1V<V1'<V2'<V3' V5'<V6'<V7'<AVDD-0.1V when POL="0", Where V1-V2=V2'-V1', V2-V3=V3'-V2',...V5-V6=V6'-V5',V6-V7=V7'-V6'. Note: V1~V7 must be supplied voltage external when VSET="1". Vx is external power of positive polarity and Vx' is external power of negative polarity
SPENB	I (Pull High)	3-Wire Communication Enable. Active Low. Normally pull high. **Please pull high or floating under PINCTLB=0 mode.**
SPDA	I/O	3-Wire Communication Data input/output.
SPCK	I	3-Wire Communication Clock input. Rising edge latch.
SPSW	I (Pull Low)	3-Wire register map select. "0" for default 3-Wire register map, "1" for optional 3-Wire register map.
RSTB	I (Pull High)	Global reset pin. Active Low to enter Reset State. Suggest connecting with a RC reset circuit for stability. Normally pull high.
PINCTLB	I (Pull High)	Enable pin control function. Normally pull high PINCTLB="0", Enable pin control function. TP0~14 and TP16~18 active as input pin for function control propose. Refer to the TP0~18 description for more information. PINCTLB="1", Default mode. TP0~14 and TP16~18 active as unknown state; Don't connect TP0~14 and TP16~18 to any state under this mode. **Note: The 3-wire control register will be disabled under PINCTLB=0 mode.**
SO1~SO960	O	Source Driver Output Signals.
GO1~GO240	O	Gate Driver Output Signals.
ALIGN_T/B	M	For assembly alignment.
CPMPDB	I	Charge pump on/off control pin. CPMPDB="0", internal charge pump will be shut down CPMPDB="1", internal charge pump normal operating If floating this pin, the charge pump will turn off
STBYB	I (Pull High)	Function control for standby mode. STBYB=0 to enter standby mode and STBYB=1 to exit standby mode. This pin is only valid when PINCTLB= "0".
UPDN, SHLR, SEL0~3, FPOL, ATPE	I	These are functional control pins. When PINCTLB= "1", the functional control is determined by respective registers, the connection state of these pins would be ignored; When PINCTLB= "0", these pins are valid for functional control.

Designation	I/O	Description
VPSW	I (Pull Low)	Voltage control switch. Normally pull low. VPSW="0". Default mode. VGH、VGL、VCOMAC and VCOMDC active as normal use and control by 3-wire. VPSW="1". Voltage fix mode. VGH=15V,VGL=-7V, VCOMAC=5.0V and VCOMDC=1.86V. Under the mode voltage can't control by 3-wire
VPP2	P	IC vendor test pin, float this pin.
VGH	PS	Capacitor pin. Positive power supply for Gate Driver output
VGL	PS	Capacitor pin. Negative power supply for Gate Driver ouput
VCOMAC	PS	Capacitor pin. Power supply for VCOMOUT output
VCOM	PS	VCOM DC voltage output pin for DC re-construction
VCOMOUT	O	Frame polarity output for panel VCOM. Amplitude of signal is from GNDA1 to VDDA1 The polarity of VCOMOUT is inversed with internal signal "POL" when "FPOL"=0
VDDA	PO	Power supply for source driver and gamma circuit
GNDA	PI	Ground pins for source driver and gamma circuit
VCI	PI	Power supply for digital and analog circuits
VSS	PI	Ground pins for digital circuits
VCIP	PI	Power supply for charge pump circuits
VSSP	PI	Ground pins for charge pump circuits
VDD	C	Capacitor connect pin for internal regulator Refer to the section of "Power Circuit" for the application.
C1P/M C1AP/M C2P/M C3P/M C4P/M Vint1/2	C	Capacitor connect pin for internal charge pump Refer to the section of "Power Circuit" for the application.
FB_P	I	Internal power switch current input pad. Note: Voltage on this pad should be <5.5V. Pull low in more than one LED case.
FB_N	O	Internal power switch current output pad. Note: Voltage on this pad should be <5.5V. Pull low in more than one LED case.
FB	VI	PWM controller feedback input. FB threshold is 0.6V nominal
DRV	O	PWM output driver signal for the boost converter
COM1_L/R	S	The internal link together between input side and Output side.
COM2_L/R	S	The internal link together between input side and Output side.
DUM	D	Don't connect to any signal or pull high/low.

Note:

I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, T: Testing

I/O: Input/Output. PS: Power Setting, C: Capacitor pin.

NV3035 Align Mark:

ALIGN_T	M	For assembly alignment.
ALIGN_B	M	For assembly alignment.

NV3035 Pass Line Description:

Pass Line No:	Pad Name	
1	COM1_L	COM1_R
2	COM2_L	COM2_R

5. Function Descriptions

5.1 Power Supply Circuits

NV3035 built in charge pump circuit for gate driver VGH/VGL voltage and panel VCOMAC/VCOMDC voltage. Following block diagram illustrate how the charge pump circuit works.
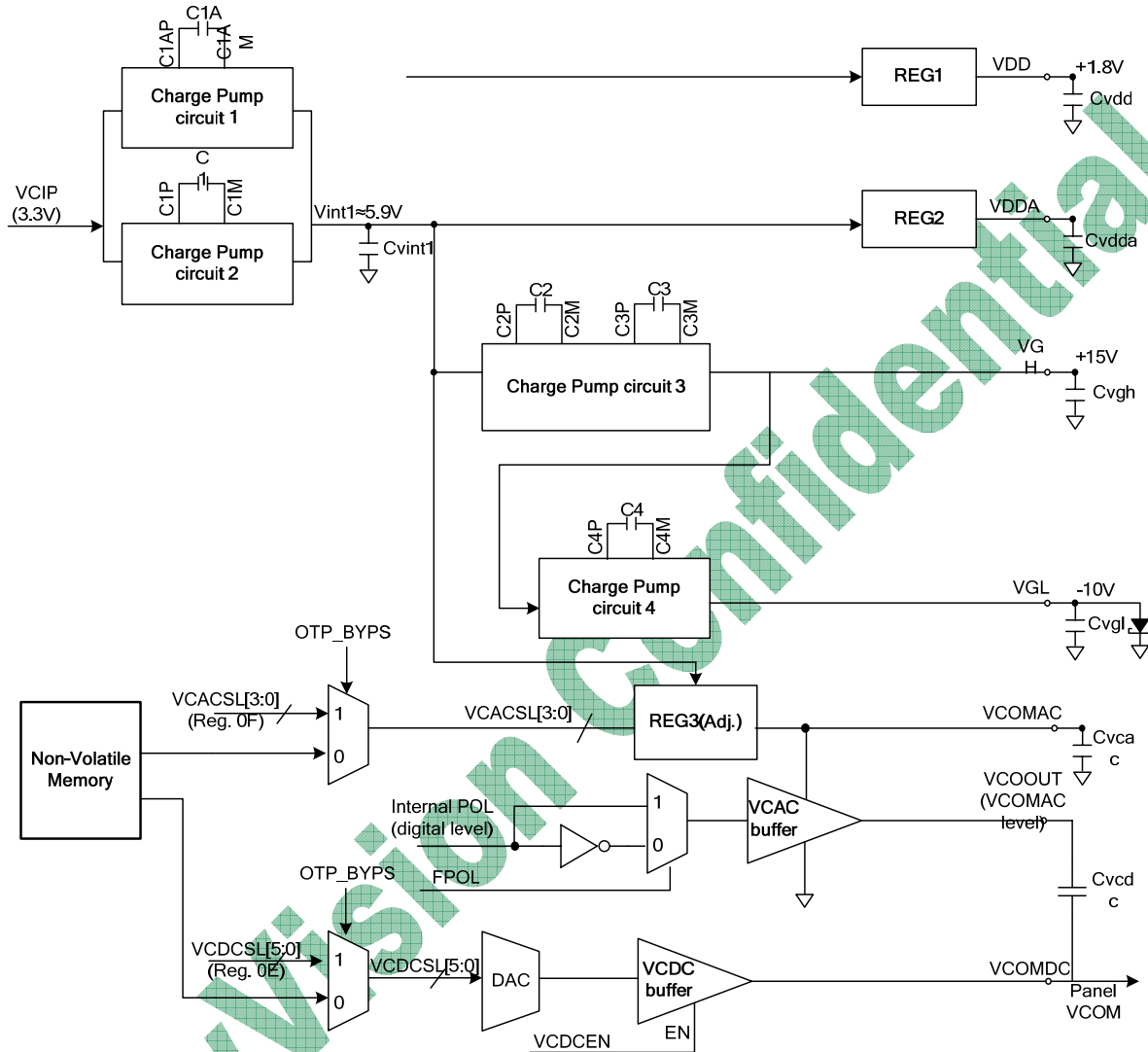
< Value of wiring resistance and Cap. >

Pin name	Resistor of wiring (ohm)	Cap no.	CAP (uF)
C1P	<10	C1	≥1uF
C1M	<10		
C2P	<10	C2	
C2M	<10		
C3P	<10	C3	
C3M	<10		
C4P	<10	C4	
C4M	<10		
C1AP	<10	C1A	
C1AM	<10		

*Note: Others Cap. Suggest value≥4.7uF
       Schottky diode turn-on voltage=0.2V

5.2 Input Data VS Output

Source Driver data output sequence can be control by "SHLR".

Output	SO1	SO2	SO3	...	SO958	SO959	SO960
SHLR="1"	First data			→			Last data
SHLR="0"	Last data			←			First data

Gate Driver scan output sequence can be control by "UPDN".

Scan	GO1	GO2	GO3	...	GO958	GO959	GO960
UPDN="1"	First data			→			Last data
UPDN="0"	Last data			←			First data

5.3 Gamma Adjustment Function

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages to get the relative resistor value and voltage calculation method, please.
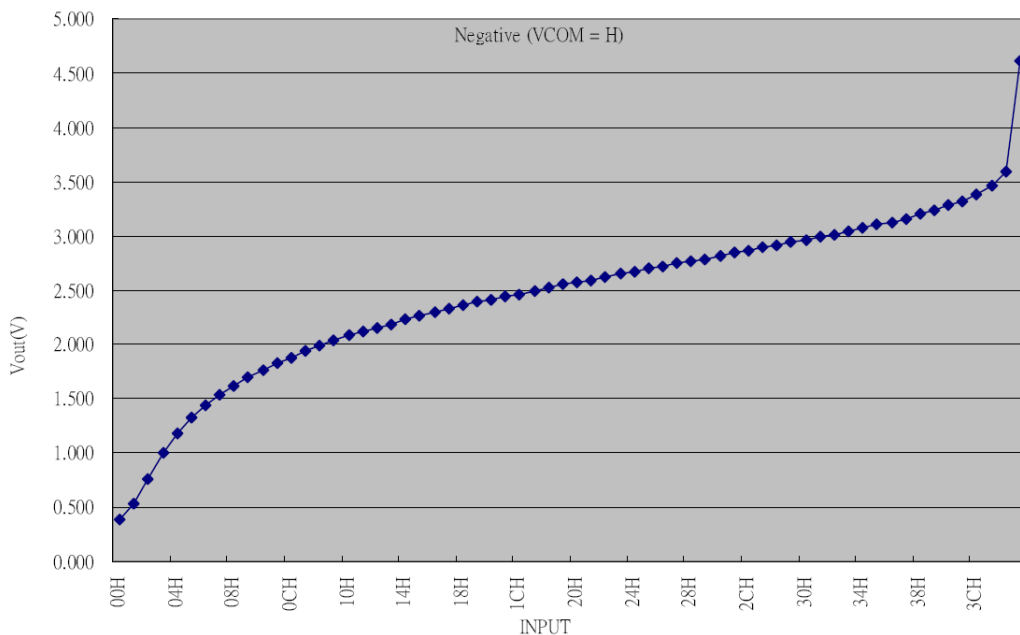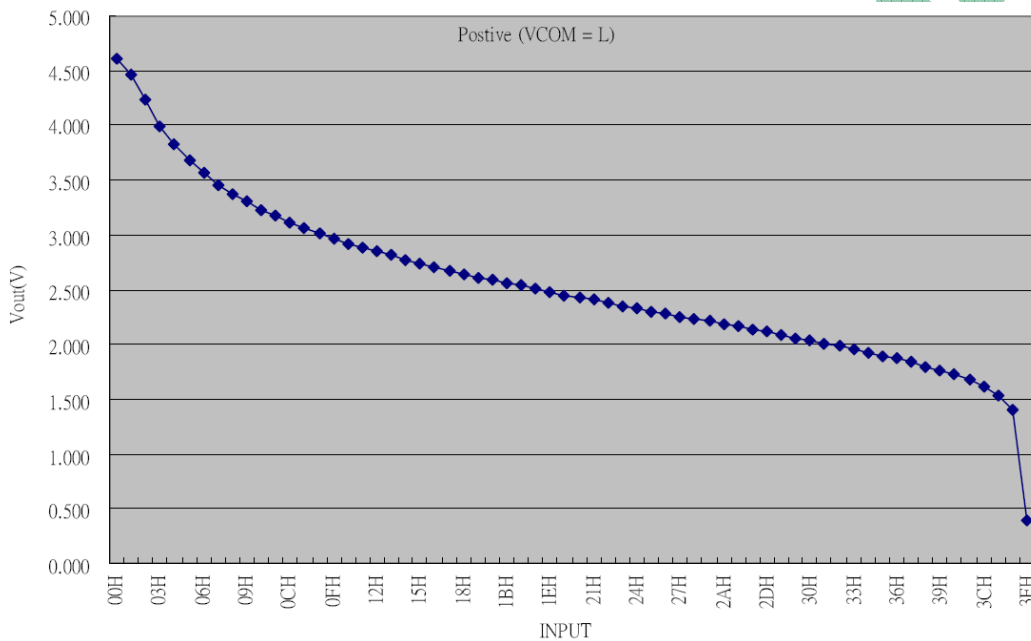
Input Data and Output Voltage Reference Table(VSET="0")

@VDDA=5V,VCOMOUT=L,POL=H	
Vno.	Unit=V
V1	4.610
V2	3.680
V3	3.115
V4	2.585
V5	2.185
V6	1.790
V7	0.390

@VDDA=5V,VCOMOUT=H,POL=L	
Vno.	Unit=V
V1	0.390
V2	1.320
V3	1.885
V4	2.415
V5	2.815
V6	3.210
V7	4.610

| Data	VCOMOUT=H,POL=L	Data	VCOMOUT=L,POL=H
(V1)00H	VDDA×0.078	(V1)00H	VDDA×0.922
01H	VDDA×0.107	01H	VDDA×0.893
02H	VDDA×0.153	02H	VDDA×0.847
03H	VDDA×0.201	03H	VDDA×0.799
04H	VDDA×0.236	04H	VDDA×0.764
(V2)05H	VDDA×0.264	(V2)05H	VDDA×0.736
06H	VDDA×0.288	06H	VDDA×0.712
07H	VDDA×0.308	07H	VDDA×0.692
08H	VDDA×0.325	08H	VDDA×0.675
09H	VDDA×0.340	09H	VDDA×0.660
0AH	VDDA×0.354	0AH	VDDA×0.646
0BH	VDDA×0.366	0BH	VDDA×0.634
(V3)0CH	VDDA×0.377	(V3)0CH	VDDA×0.623
0DH	VDDA×0.388	0DH	VDDA×0.612
0EH	VDDA×0.398	0EH	VDDA×0.602
0FH	VDDA×0.408	0FH	VDDA×0.592
10H	VDDA×0.416	10H	VDDA×0.584
11H	VDDA×0.424	11H	VDDA×0.576
12H	VDDA×0.431	12H	VDDA×0.569
13H	VDDA×0.438	13H	VDDA×0.562
14H	VDDA×0.446	14H	VDDA×0.554
15H	VDDA×0.453	15H	VDDA×0.547
16H	VDDA×0.459	16H	VDDA×0.541
17H	VDDA×0.465	17H	VDDA×0.535
18H	VDDA×0.472	18H	VDDA×0.528
19H	VDDA×0.478	19H	VDDA×0.522
(V4)1AH	VDDA×0.483	(V4)1AH	VDDA×0.517
1BH	VDDA×0.488	1BH	VDDA×0.512
1CH	VDDA×0.493	1CH	VDDA×0.507
1DH	VDDA×0.499	1DH	VDDA×0.501
1EH	VDDA×0.505	1EH	VDDA×0.495
1FH	VDDA×0.510	1FH	VDDA×0.490
20H	VDDA×0.514	20H	VDDA×0.486
21H	VDDA×0.519	21H	VDDA×0.481
22H	VDDA×0.525	22H	VDDA×0.475
23H	VDDA×0.530	23H	VDDA×0.470
24H	VDDA×0.535	24H	VDDA×0.465
25H	VDDA×0.540	25H	VDDA×0.460
26H	VDDA×0.545	26H	VDDA×0.455
27H	VDDA×0.550	27H	VDDA×0.450
28H	VDDA×0.554	28H	VDDA×0.446
29H	VDDA×0.558	29H	VDDA×0.442
(V5)2AH	VDDA×0.563	(V5)2AH	VDDA×0.437
2BH	VDDA×0.568	2BH	VDDA×0.432
2CH	VDDA×0.573	2CH	VDDA×0.427
2DH	VDDA×0.578	2DH	VDDA×0.422
2EH	VDDA×0.583	2EH	VDDA×0.417
2FH	VDDA×0.588	2FH	VDDA×0.412
30H	VDDA×0.593	30H	VDDA×0.407
31H	VDDA×0.598	31H	VDDA×0.402
32H	VDDA×0.603	32H	VDDA×0.397
33H	VDDA×0.609	33H	VDDA×0.391
34H	VDDA×0.615	34H	VDDA×0.385
35H	VDDA×0.621	35H	VDDA×0.379
36H	VDDA×0.626	36H	VDDA×0.374
37H	VDDA×0.632	37H	VDDA×0.368
(V6)38H	VDDA×0.642	(V6)38H	VDDA×0.358
39H	VDDA×0.648	39H	VDDA×0.352
3AH	VDDA×0.656	3AH	VDDA×0.344
3BH	VDDA×0.665	3BH	VDDA×0.335
3CH	VDDA×0.677	3CH	VDDA×0323
3DH	VDDA×0.693	3DH	VDDA×0.307
3EH	VDDA×0.719	3EH	VDDA×0.281
(V7)3FH	VDDA×0.922	(V7)3FH	VDDA×0.078

5.4 3-Wire SPI
3-Wire Command Format

NV3035 uses the 3-wire serial port as communication interface for all the function and parameter setting.

3-Wire communication can be bi-directional controlled by the "R/W" bit in address field. NV3035 3-Wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SPCK by external controller. Data in the "Hi-Z phase" will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SPDA pin under "Hi-Z phase" and "Data phase".

Refer to the section of "3-Wire Timing Diagram" for the detail timing, please.
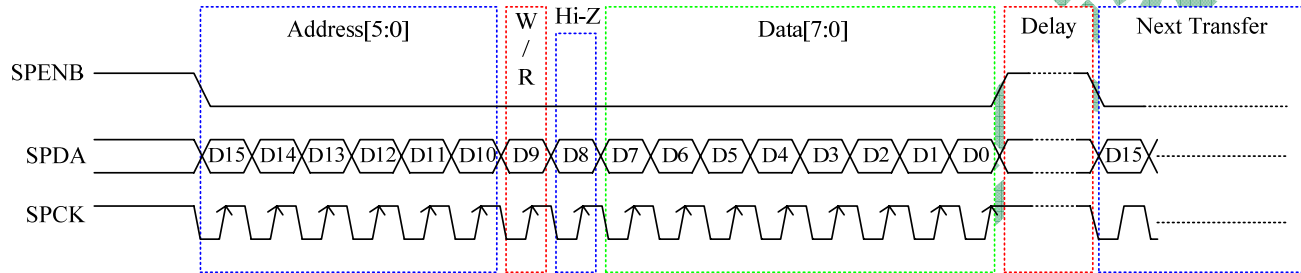
3-Wire Command Format:

Bit	Description
D15-D10	Register Address [5:0]
D9	W/R control bit. "1" for Write; "0" for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						1	X	DATA (Issue by external controller)							

3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						0	Hi-Z	DATA (Issue by NV3035)							

6. Command Description

6.1 Registers Table

Following table list the default 3-Wire control registers and bit name definition for NV3035. Refer to the next section for detail register function description, please.

NV3035 3-Wire Control Register List (Default)

3-Wire Registers		Register Description		
D[15:10]	Name	Init.	R/W	Function Description
000000b	R00	03h	R/W	System control register
000001b	R01	00h	R/W	Timing Controller function register
000010b	R02	03h	R/W	Operation control register
000011b	R03	8Ch	R/W	Input data Format control register
000100b	R04	46h	R/W	Source Timing delay control register
000101b	R05	0Dh	R/W	Gate Timing delay control register
000111b	R07	00h	R/W	Internal function control register
001000b	R08	08h	R/W	RGB Contrast control register
001001b	R09	40h	R/W	RGB Brightness control register
001011b	R0B	88h	R/W	R/B Sub-Contrast control register
001100b	R0C	20h	R/W	R Sub-Brightness control register
001101b	R0D	20h	R/W	B Sub-Brightness control register
001110b	R0E	2bh	R/W	VCOMDC Level Control Register
001111b	R0F	A5h	R/W	VCOMAC Level Control Register
010000b	R10	04h	R/W	VGAM2 level Control Register
010001b	R11	24h	R/W	VGAM3/4 level control register
010010b	R12	24h	R/W	VGAM5/6 level control register
011101b	R1D	00h	R/W	OTP operation control register
011110b	R1E	00h	R/W	OTP operation control register
011111b	R1F	00h	R/W	OTP operation control register

NV3035 3-Wire Register Bit Definition (Default)

Reg.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
				3-Wire Control Register Bit Map				
R00	PAT3	PAT2	PAT1	PAT0	PWMPDB	X	STBYB	RESETB
R01	X	X	X	SWD2	SWD1	SWD0	DITHB	CFTYP
R02	0	0	0	X	FPOL	VSET	UPDN	SHLR
R03	DENPOL	CLKPOL	HSDPOL	VSDPOL	SEL3	SEL2	SEL1	SEL0
R04	DDLY7	DDLY6	DDLY5	DDLY4	DDLY3	DDLY2	DDLY1	DDLY0
R05	X	HDLY6	HDLY5	HDLY4	HDLY3	HDLY2	HDLY1	HDLY0
R07	0	0	INVSL1	INVSL0	0	0	-	0
R08	X	X	X	CON4	CON3	CON2	CON1	CON0
R09	X	BRI6	BRI5	BRI4	BRI3	BRI2	BRI1	BRI0
R0B	SCONB1	SCONB0			SCONR1	SCONR0		
R0C	X	X	SBRIR5	SBRIR4	SBRIR3	SBRIR2	SBRIR1	SBRIR0
R0D	X	X	SBRIB5	SBRIB4	SBRIB3	SBRIB2	SBRIB1	SBRIB0
R0E	X	OTP_BYPS	VCDCSL5	VCDCSL4	VCDCSL3	VCDCSL2	VCDCSL1	VCDCSL0
R0F	VGLSL1	VGLSL0	VGHSL1	VGHSL0	VCACSL3	VCACSL2	VCACSL1	VCACSL0
R10	X	X	X	GAMEN	X	V2GAM2	V2GAM1	V2GAM0
R11	X	X	V4GAM2	V4GAM1	V4GAM0	V3GAM2	V3GAM1	V3GAM0
R12	X	X	V6GAM2	V6GAM1	V6GAM0	V5GAM2	V5GAM1	V5GAM0
R1D	PDIN[7]	PDIN[6]	PDIN[5]	PDIN[4]	PDIN[3]	PDIN[2]	PDIN[1]	PDIN[0]
R1E	PPROG	PSWSL	PWE	POR	PTM[1]	PTM[0]	PA[1]	PA[0]
R1F								OTPSEL

Note: Register function active at the falling edge of VSD except STBYB, RESETB register bits.

Registers list below require Vsync trigger

DITHB, CFTYP, FPOL, VSET, UPDN, SHLR, DDLY, HDLY, INVSL, CON, BRI, HUE, SAT, SCONB, SCONR, SBRIR, SBRIB

6.2 Command Descriptions

R00: System Control Register

Bit	Name	Initial	R/W	Description
Bit [7:4]	PAT[3:0]	0000b	R/W	Internal Test Pattern Selection PAT[3:0]: Select chip embedded test pattern.
Bit [3]	PWMPDB	0b	(R) R/W	Internal PWM controller Power Down bit PWMPDB="0", internal PWM controller will be shut down PWMPDB="1", internal PWM controller normal operating
Bit [2]	-	-	-	Reserve
Bit [1]	STBYB	1b	(R) R/W	Standby Mode function control. STBYB="0", TCON, Source output will turn off and outputs are High-Z. STBYB="1", Normal operation
Bit [0]	RESETB	1b	R/W	Global Reset Register. Write "0" to reset whole chip. This bit will set to "1" automatically after chip was reset.

PAT[3:0]: Embedded Auto Test Pattern Selection Register

PAT[3:0]	Test Pattern	Note
00H	Disable Internal Test Pattern Function	Default
01H	White	
02H	Black	
03H	Red	
04H	Green	
05H	Blue	
06H	Yellow	
07H	Cyan	
08H	Magenta	
09H	Gray Level 8	
0AH	Gray Level 16	
0BH	Color Bar	
0CH	Checker Board	
0DH	Cross Talk Pattern	
0EH	Horizontal Flick Pattern	
0FH	Test Pattern Auto Run Mode	

R01: Timing Controller Function Register

Bit	Name	Initial	R/W	Description
Bit[4:2]	SWD[2:0]	000b	R/W	Control and switch the relationship between the R, G, B and outputs. This register is used to match different types of color filters on LCD panel
Bit[1]	DITHB	0b	R/W	Dithering enable. Active low DITHB="0", Dithering on, (Pseudo 8-bits resolution). (Default mode) DITHB="1", Dithering off, (6-bits resolution, truncation last 2-bits of the input data)

				Note 1: Recommend user to enable this function under all modes except for 18 bit RGB input application.
Bit[0]	CFTYP	0b	R/W	Color Filter Type Select. Select Delta or Stripe mode for data arrangement. CFTYP="0", Stripe mode, Data arrangement keep in the "odd line" state of SWD[2:0] selection. CFTYP="1", Data arrangement controlled by SWD[2:0] setting.

SWD [2:0] function control:

SWD2	SWD1	SWD0	Output (n=0 to 319)				Condition
			3n+1	3n+2	3n+3		
0	0	0	R	G	B	Odd Line	
			G	B	R	Even Line	
0	0	1	G	B	R	Odd Line	
			B	R	G	Even Line	
0	1	X	B	R	G	Odd Line	
			R	G	B	Even Line	SHLR="1"
1	0	0	G	B	R	Odd Line	UPDN="1"
			R	G	B	Even Line	
1	0	1	B	R	G	Odd Line	
			G	B	R	Even Line	
1	1	X	R	G	B	Odd Line	
			B	R	G	Even Line	

Note 1: X= Don't care
Note 2: Data arrangement will keep in the "odd line" state when CFTYP=0 for stripe mode.

R02: Operation Control Register

Bit	Name	Initial	R/W	Description
Bit[7:4]	-	-	-	Reserve
Bit[3]	FPOL	0b	R/W	VCOMOUT polarity inverse control. FPOL="0": VCOMOUT normal polarity (Default mode). FPOL="1": VCOMOUT inverse polarity.
Bit[2]	VSET	0b	R/W	Gamma correction source select. VSET="0",used internal Gamma Reference voltage (VDDA). (Default mode) VSET="1",used external Gamma Reference Input (V1~V7).
Bit[1]	UPDN	1b	(R) R/W	Gate Driver Up/down scan control of gate driver. UPDN="0", Shift from down to up, First line=L240→L239→…→L2→L1=Last line UPDN="1", Shift from up to down, First line=L1→L2→…→L239→L240=Last line (Default mode)
Bit[0]	SHLR	1b	(R) R/W	Right/Left sequence control of source driver. SHLR="0", shift left: Last data=S1←S2←S3…←S960= First data. SHLR="1", shift right: First data=S1→S2→S3…→S960= Last data.

R03: Input Data Format Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	DENPOL	1b	R/W	DEN input pin polarity control. DENPOL="0", DEN negative polarity. DENPOL="1", DEN positive polarity. (Default mode)
Bit[6]	CLKPOL	0b	R/W	CLKIN pin polarity control. CLKPOL="0", CLKIN negative edge latch data. CLKPOL="1", CLKIN positive edge latch data. (Default mode)
Bit[5]	HSDPOL	0b	R/W	HSD pin polarity control. HSDPOL="0", HSD negative polarity. (Default mode) HSDPOL="1", HSD positive polarity.
Bit[4]	VSDPOL	0b	R/W	VSD pin polarity control. VSDPOL="0", VSD negative polarity. (Default mode) VSDPOL="1", VSD positive polarity
Bit[3:0]	SEL[3:0]	1100b	(R) R/W	Input data format selection. Note: Different SEL[3:0] setting resolution in different AC timing.

SEL [3:0]: Data input mode

SEL3	SEL2	SEL1	SEL0	Data input format	Operating frequency
0	x	x	x	-	-
1	0	0	0	8-bit digital RGB input format HV Mode (NTSC only)	27MHz
1	0	0	1	8-bit digital RGB input format DE Mode (NTSC only)	27MHz
1	0	1	0	8-bit digital RGB through mode input format HV Mode (NTSC only)	27MHz
1	0	1	1	8-bit digital RGB through mode input format DE Mode (NTSC only)	27MHz
1	1	0	0	24-bit digital RGB input format HV Mode(NTSC only)	6.4MHz
1	1	0	1	24-bit digital RGB input format DE Mode(NTSC only)	6.4MHz
1	1	1	*	-	-

Note: Hsync and Vsync will be ignored in DE mode

Remark:RGB through mode will bypass 3-wire SWD[2:0] function; TCON will not arrange data color mapping.

R04: Source Timing Delay Control Register

Bit	Name	Initial	R/W	Description
Bit[7:0]	DDLY[7:0]	46h	R/W	Select the HSD signal to 1st input data delay timing Under RGB 8/24 bit mode, Ths=DDLY[7:0], (Unit=CLKIN) The register value will be update to the different default value each time when SEL[3:0] changed. Read the section of 9.3 for the detail, please.

Note: DDLY function will be disabled under 8/24 bit DE mode and PINCTLB=0 condition. The default value list in the section 9.3 will be used when PINCTLB=0.

R05: Gate Timing Delay Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	-	-	-	Reserve
Bit[6:0]	HDLY[6:0]	0Dh	R/W	Select the Gate start pulse output delay timing Tvs=HDLY[6:0], (Unit=HSD) The register value will be update to the different default value each time when SEL[3:0] changed. Read the section of 9.3 for the detail, please.

Note: HDLY function will be disabled under 8/24 DE mode and PINCTLB=0 condition. The default value list in the section 9.3 will be used when PINCTLB=0.

R07: Internal Function Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	-	-	-	Reserve
Bit[5:4]	INVSL[1:0]	00b	R/W	Source Driving Mode Selection Register
Bit[3:0]	-	-	-	Reserve

INVSL [1:0]

INVSL1	INVSL0	Driving Mode	Notes
0	0	1-Line Inversion	Default
0	1	2-Line Inversion	
1	0	Frame Inversion	
1	1	Reserved	

R08: Contrast Control Register

Bit	Name	Initial	R/W	Description
Bit[7:5]	-	-	-	Reserve
Bit[4:0]	CON[4:0]	08h	R/W	Display Contrast level adjustment register. (0.125/Step) Adjust range from 0x00(level=0) to 0x1F(level=3.875) Default value 08h(level=1.0)

R09: Brightness Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	-	-	-	Reserve
Bit[6:0]	BRI[6:0]	40h	R/W	Display Brightness level adjustment register. (2/Step) Adjust range from 0x00(level=-128) to 0x7F(level=+126) Default value 0x40(level=+0)

R0B: R/B Sub-Contrast Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	SCONB[1:0]	02h	R/W	B Data Contrast level adjustment register. (0.125/Step) Adjust range from 0x00(level=0.75) to 0x0F(level=1.125) Default value 08h(level=1.0)
Bit[3:2]	SCONR[1:0]	02h	R/W	R Data Contrast level adjustment register.(0.125/Step) Adjust range from 0x00(level=0.75) to 0x0F(level=1.125) Default value 08h(level=1.0)

R0C: R Sub-Brightness Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	-	-	-	Reserve
Bit[5:0]	SBRIR[5:0]	20h	R/W	R Data Brightness level adjustment register.(1/Step) Adjust range from 0x00(level=-32) to 0x3F(level=+31) Default value 20h(level=0)

R0D: B Sub-Brightness Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	-	-	-	Reserve
Bit[5:0]	SBRIB[5:0]	20h	R/W	B Data Brightness level adjustment register.(1/Step) Adjust range from 0x00(level=-32) to 0x3F(level=+31) Default value 20h(level=0)

ROE: VCOMDC Level Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	-	-	-	Reserve
Bit[6]	OTP_BYPS	0h	R/W	VCDCSL[5:0] data source selection register OTP_BYPS="0", VCDCSL [5:0] is read from OTP memory. OTP_BYPS="1", VCDCSL [5:0] is switch to the 3-wire register memory when user want to adjust the VCOMDC level for test propose. Refer to the "TRMEN" control register for the proper OTP write operation.
Bit[5:0]	VCDCSL[5:0]	2bh	R/W	VCOMDC level control register (20mV/Step @ VDDA=5.0V) VCDCSL[5:0]=00h, VCOMDC=1.00V VCDCSL[5:0]=01h, VCOMDC=1.02V ...... VCDCSL[5:0]=10h, VCOMDC=1.32V ...... VCDCSL[5:0]=3eh, VCOMDC=2.24V VCDCSL[5:0]=3fh, VCOMDC=2.26V

Note: VCOMDC always keep 1.86V When VPSW="1". The OTP value effect in VPSW=0.

ROF VCOMAC Level Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	VGLSL	10	R/W	VGLSL level control register VGLSL Level=1V/Step
Bit[5:4]	VGHSL	10	R/W	VGHSL level control register VGHSL Level=1V/Step
Bit[3:0]	VCACSL[3:0]	0101	R/W	VCOMAC level control register VCOMAC level=0.1V/Step @ VDDA =5.0V

VCACSL [3:0]

VCSL3	VCSL2	VCSL1	VCSL0	Level(V)
0	0	0	0	4.6
0	0	0	1	4.7
0	0	1	0	4.8
0	0	1	1	4.9
0	1	0	0	5.0(Default)
0	1	0	1	5.1
0	1	1	0	5.2
0	1	1	1	5.3
1	0	0	0	5.4
1	0	0	1	5.5
1	0	1	0	-
1	0	1	1	-
1	1	*	*	-

Note: When VPSW="1". The register can't be used and VCOMAC always keep 5.0V.
Make sure to set VCOMAC < VINT1-0.3V.

VGHSL [5:4]

VGHSL1	VGHSL0	VGH(V)
0	0	12
0	1	13
1	1	14
1	0	15(default)

When VPSW="1". The register can't be used and VGH always keep 15V.

VGHSL [7:6]

VGLSL1	VGLSL0	VGL(V)
0	0	-7(default)
0	1	-8
1	1	-9
1	0	-10

When VPSW="1". The register can't be used and VGL always keep -7V.

R10: VGAM2 Level Control Register

Bit	Name	Initial	R/W	Description
Bit[7:5]	-	-	-	Reserve
Bit[4]	GAMEN	0b	R/W	GAMMA adjustment enable control register. (adjustable voltage for V2-V6) GAEN="0" or VSET=1, Gamma correction disabled. GAEN="1" & VSET=0, Gamma correction enabled.
Bit[3]	-	-	-	Reserve
Bit[2:0]	V2GAM [2:0]	100b	R/W	V2 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level=22mV /Step

R11: VGAM3/4 Level Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	-	-	-	Reserve
Bit[5:3]	V4GAM [2:0]	100b	R/W	V4 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level=22mV/Step
Bit[2:0]	V3GAM [2:0]	100b	R/W	V3 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level=22mV /Step

R12: VGAM5/6 Level Control Register

Bit	Name	Initial	R/W	Description
Bit[10:6]	-	-	-	Reserve
Bit[5:3]	V6GAM [2:0]	100b	R/W	V6 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level=22mV/Step
Bit[2:0]	V5GAM [2:0]	100b	R/W	V5 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level=22mV /Step

V2GAM/ V3GAM/ V4GAM/ V5GAM/ V6GAM Level Control Register Setting Table

VxGMA2	VxGMA1	VxGMA0	Voltage level	Unit	Note
0	0	0	+88	mV	
0	0	1	+66	mV	
0	1	0	+44	mV	
0	1	1	+22	mV	
1	0	0	+0(Default)	mV	Refer to the Gamma Table for the default voltage level of V2~V6
1	0	1	-22	mV	
1	1	0	-44	mV	
1	1	1	-66	mV	

Note: x=2, 3, 4, 5, 6

R1D: OTP Operation Control Register

Bit	Name	Initial	R/W	Description
Bit[7:0]	PDIN	00b	R/W	Program data for OTP

R1E: OTP Operation Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	PPROG	0b	R/W	Program mode enabling.
Bit[6]	PSWSL	0b	R/W	Power supply select.
Bit[5]	PWE	0b	R/W	Define program cycle.
Bit[4]	POR	0b	R/W	Generate a pulse to read OTP.
Bit[3:2]	PTM[1:0]	00b	R/W	Test mode.
Bit[1:0]	PA[1:0]	00b	R/W	Programming address.

R1F OTP Operation Control Register
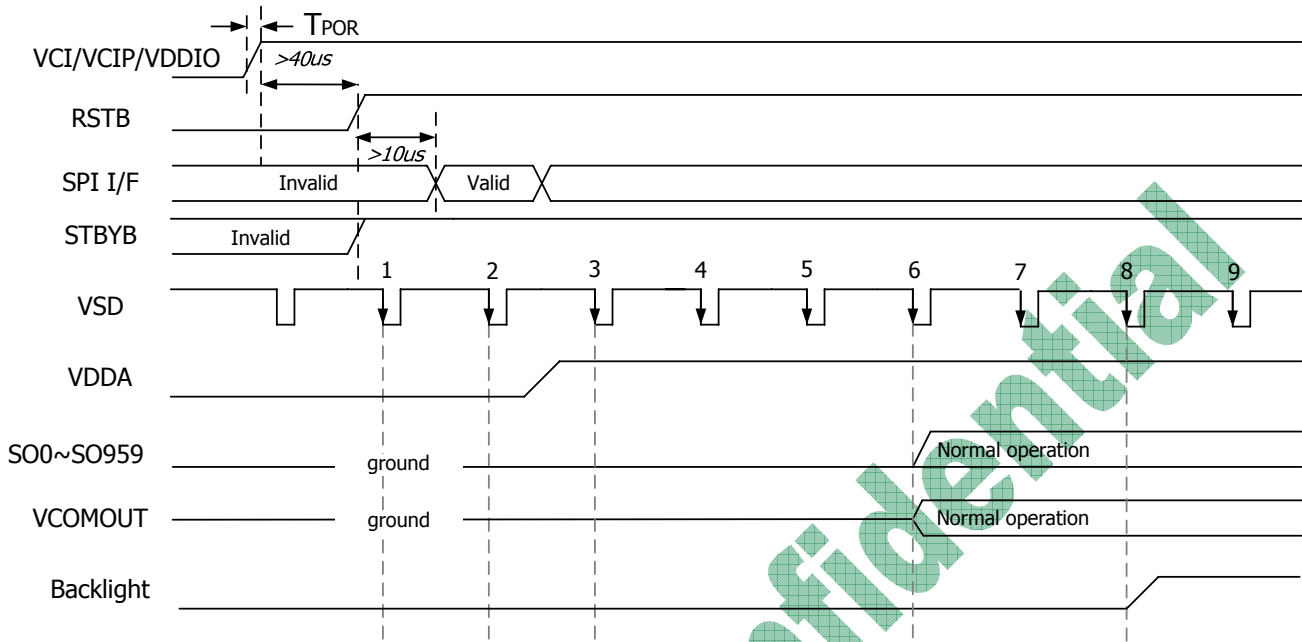
Bit	Name	Initial	R/W	Description
Bit[0]	OTPSEL	0b	R/W	OTP bank select.

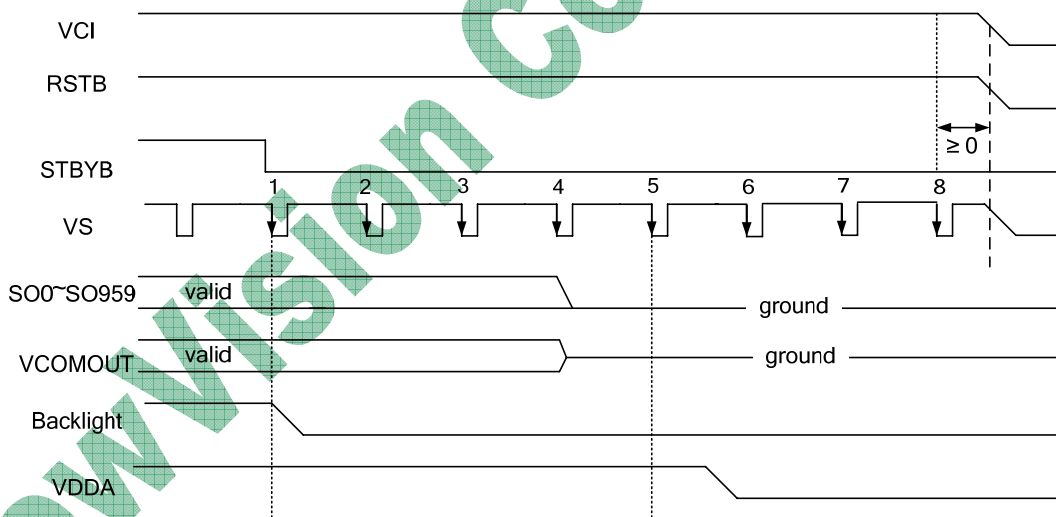Note: Burning data for VCDCSL/VCACSL **do not** need external HV power supply and can be programmed 3 times.

7. Power On/Off Sequence

7.1 Power-On Timing Sequence

7.2 Power-Off Timing Sequence

8. DC Electrical Characteristics

(Test Condition: VCI=VCIP=3.3V, VDDA=5.0V, VSS=GNDA=VSSP=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Supply Voltage	VCI	3.0	3.3	3.6	V	
I/O power supply	VDDIO	VDD	3.3	3.6	V	
Pump circuits supply	VCIP	3.0	3.3	3.6	V	
Low power supply	VDD	1.6	1.8	2.0	V	
Low Level Input Voltage	Vil	VSS	-	0.2xVDDIO	V	Digital input pins TA=25℃
High Level Input Voltage	Vih	0.8xVDDIO	-	VDDIO	V	Digital input pins TA=25℃
Input Leakage Current	Ii	-	-	±1	µA	Digital input pins
High Level Output Voltage	Voh	VDDIO-0.4	-	VDDIO	V	Digital output pins; Ioh=400µA
Low Level Output Voltage	Vol	VSS	-	VSS+0.4	V	Digital output pins; Iol= -400µA
2xVCI pump output level	VINT1	5.2	5.5	5.8	V	VCIP=3.3V, w/o panel loading
Analog power voltage	VDDA	4.5	5.0	VINT1-0.3	V	Analog circuit power from Power Block
VCOMAC output level	VCOMAC	4.6	-	VINT1-0.3	V	By VCSL[2:0] setting VCOMAC=$V_{(VCSL[3:0])}$±100mV
VCOMDC output level	VCOMDC	1.0	-	2.26	V	By VCDCSL[5:0] setting VCOMDC= $V_{(VCDCSL[5:0])}$±50mV
Positive power supply	VGH	14.5	15	15.5	V	Gate driver load + procard load
Negative power supply	VGL	-8	-7	-6	V	Gate driver load + procard load
Base drive current	IDRV	-	-	10	mA	VCIP=3.3V, DRV=0.7V
DRV output voltage	VDRV	VSS+0.1	-	VCI-0.1	V	
Feed back voltage	VFB	0.55	0.6	0.65	V	DC/DC operating, VBL current=20mA
Voltage Deviation of Outputs	Vvd	-	±20	±35	mV	Vo=0.1V~0.5V & VDDA-0.5V~VDDA-0.1V
			±15	±25	mV	Vo=0.5V~VDDA-0.5V
Low-Level Output Current of VCOMOUT	IOLF	-	-10	-	mA	Force VCOMAC=6.0V VCOMOUT output=0V V.S 0.9V
High-Level Output Current of VCOMOUT	IOHF	-	10	-	mA	Force VCOMAC=6.0V VCOMOUT output=6.0V V.S 5.1V
Source Low-Level Output Current	I_{OLS}	-	-30	-	µA	Son=Vo V.S. (Vo+0.9)
Source High-Level Output Current	I_{OHS}	-	30	-	µA	Son=Vo V.S. (Vo-0.9)
Gate Low-Level Output Current	IOLG	-	-250	-	µA	GOn; Vo=VGL V.S. (VGL+0.5)
Gate High-Level Output Current	IOHG	-	250	-	µA	GOn; Vo=VGL V.S. (VGH-0.5)
Chip Stand-by Current	Idds	-	15	50	µA	STBYB="0", all function are shutdown, CLKIN/VSD/HSD halted
Chip Operating Current	Idda	-	10	-	mA	No load, CLKIN=27MHz, Fld=15KHz

9. AC Electrical Characteristics

9.1 Input Data Format
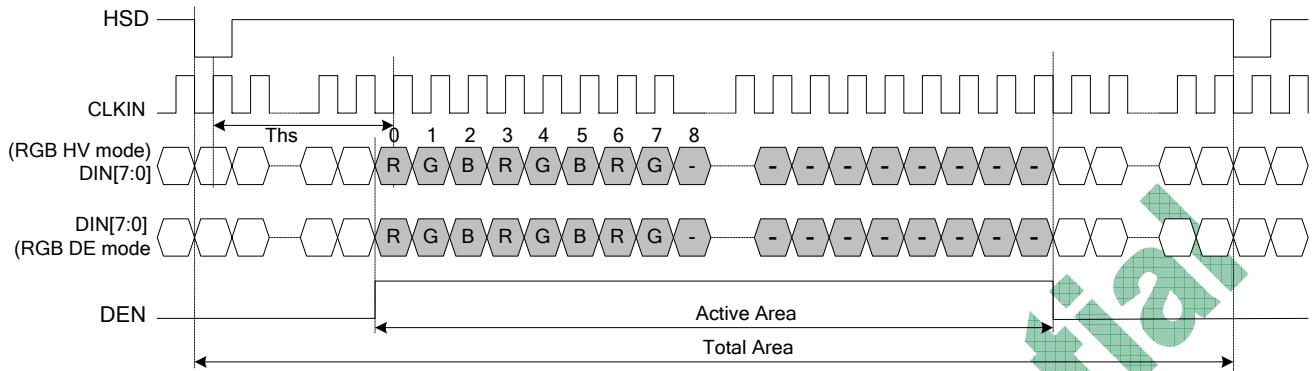
Input Format	Format Standard	CLKIN(MHz)	HSD(CLKIN)	Total Area (CLKIN)	Active Area (CLKIN)	Note
8bit RGB	8bit RGB	27	1	1716	960	960×240
24bit RGB	24bit RGB	6.4	1	408	320	

9.2 Time Diagram

Clock and Data Input Timing Diagram
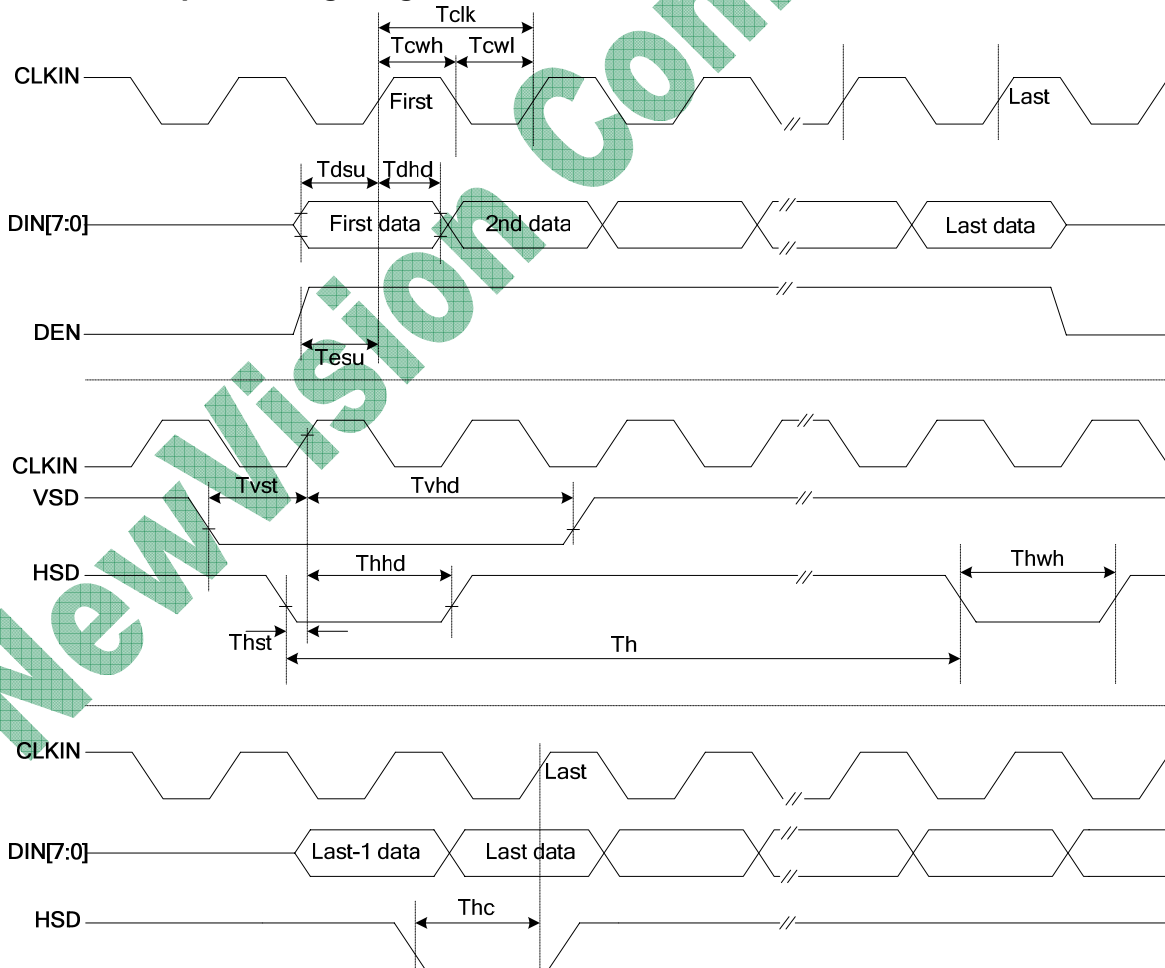
3-Wire Timing Diagram
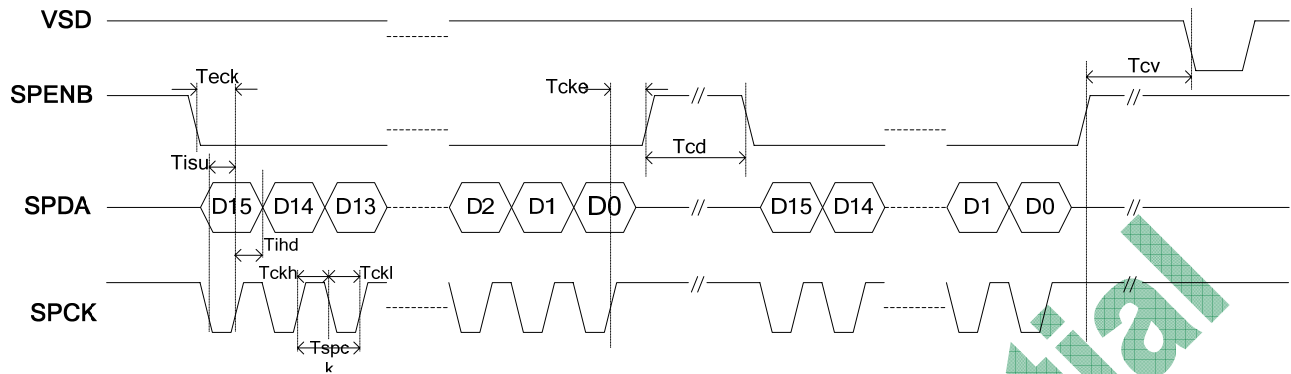
Source Driver Output Timing Diagram
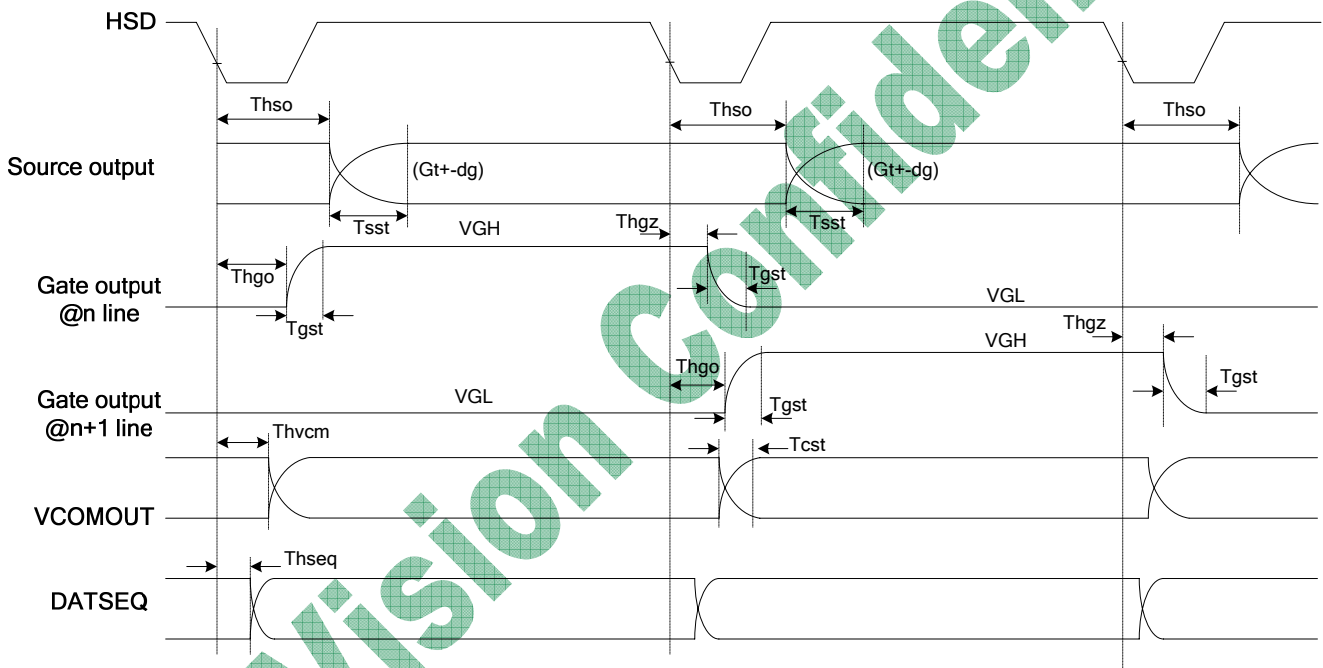
Gate Driver Output Timing Diagram
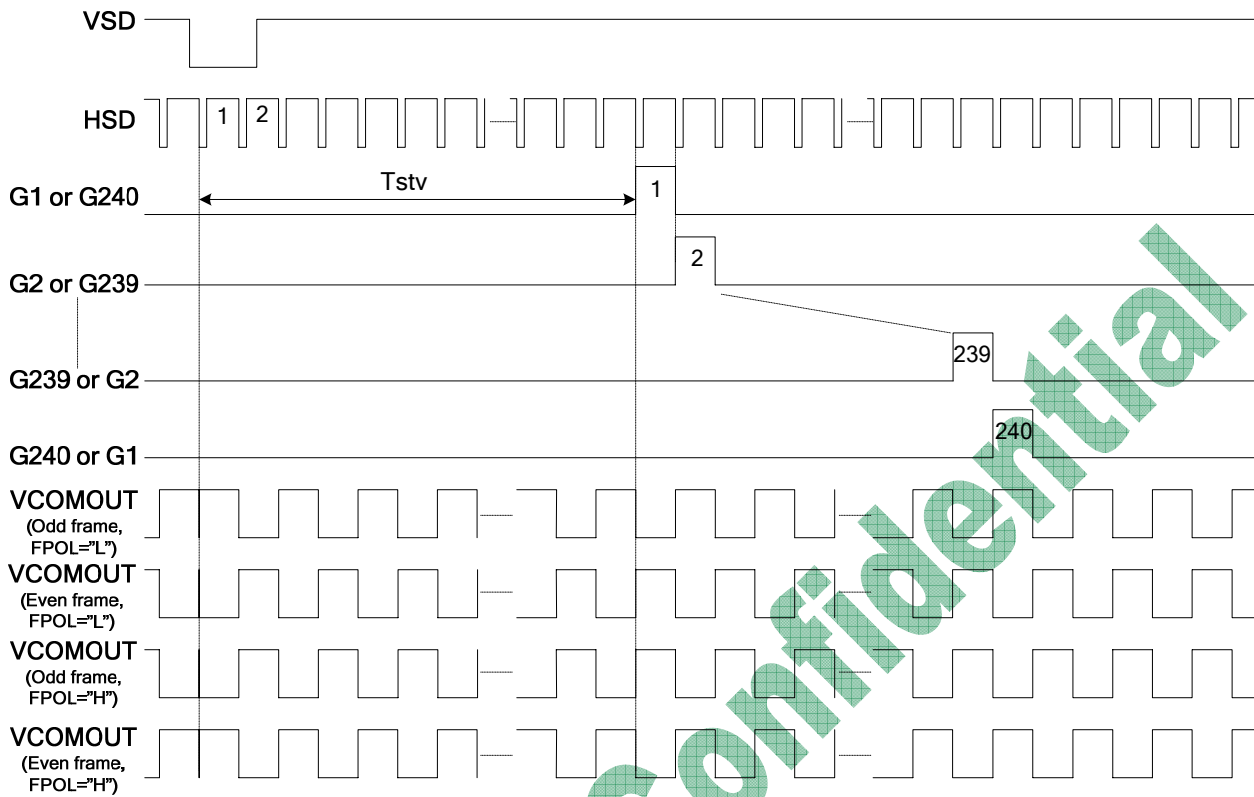
Vertical Timing Diagram (HV Mode)
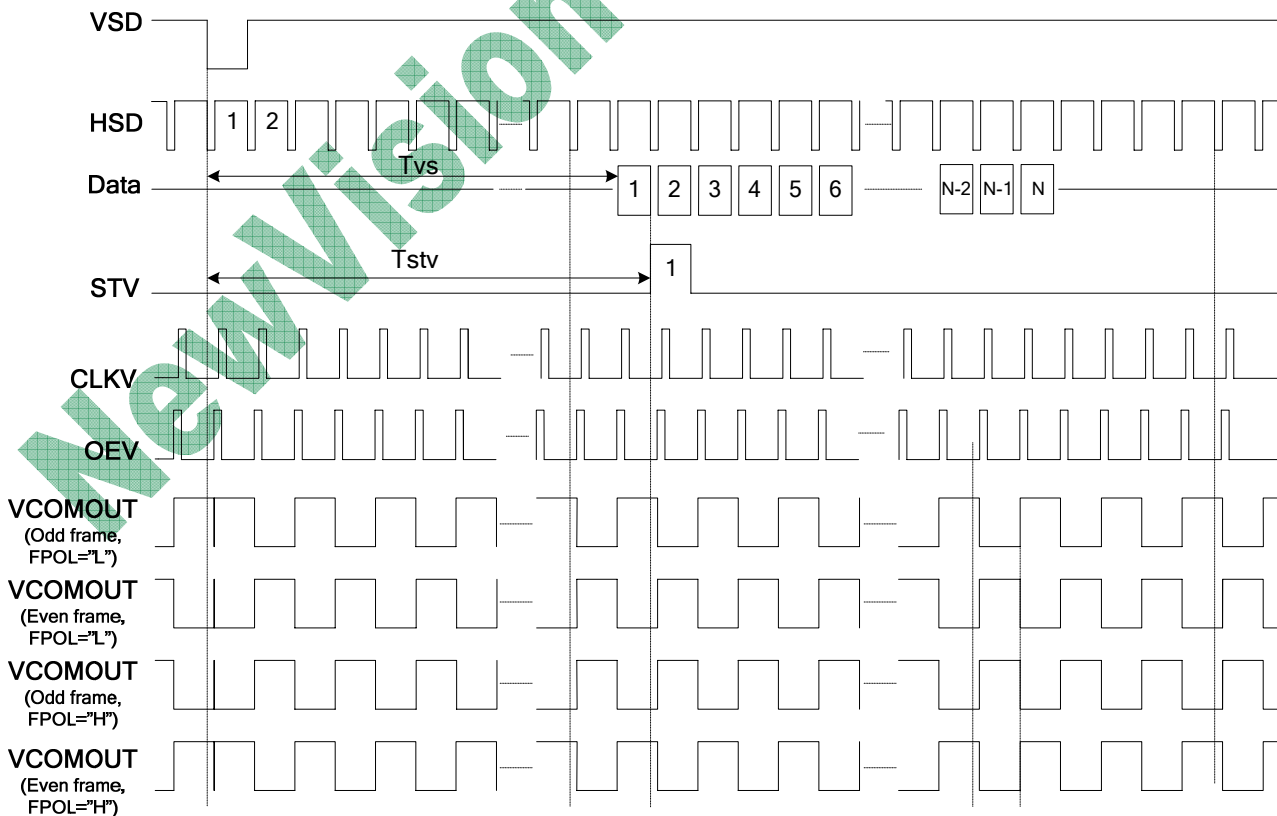
Vertical Timing Diagram (DE Mode)
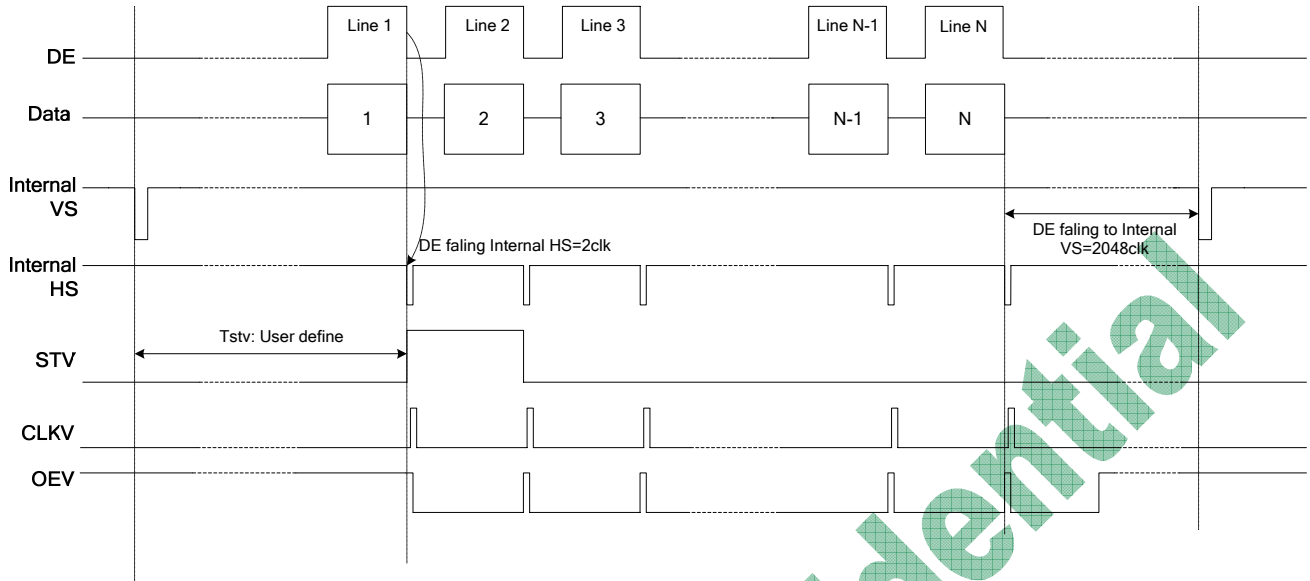
Input Data Timing (24 bit RGB mode for 960×240 @ SEL[3:0]=1100b)
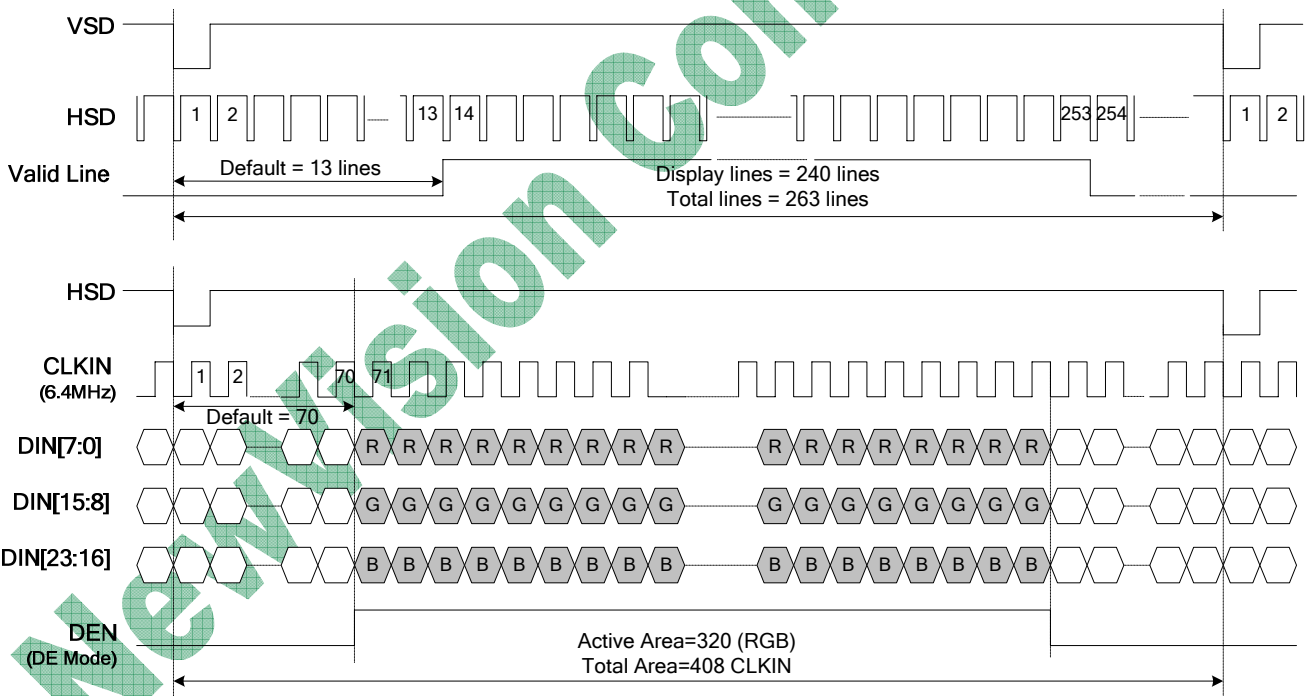
9.3 Specifications

Test Condition: (VCI=VCIP=3.3V,VDDA=5.0V,VSS=GNDA=VSSP=0V,TA=25℃)

8 Bit RGB 960 CH Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	27	30	MHz	VDD=3.0~3.6V
CLKIN cycle time	Tclk	-	37		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time that HSD to 1st data input(NTSC)	Ths	35	70	255	CLKIN	DDLY=70,Offset=0(fixed)

24 Bit RGB Mode (@ SEL[3:0]=1100 or 1101)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	6.1	6.4	8.0	MHz	VDD=3.0~3.6V
CLKIN cycle time	Tclk	125	156	164	ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time that HSD to 1st data input(NTSC)	Ths	40	70	255	CLKIN	DDLY=70,Offset=0(fixed)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
System Operation Timing						
VDD power source slew time	T$_{POR}$			1000	us	From 0V to 90% VDD
RSTB active pulse width	T$_{RSTB}$	40			us	VDD=3.3V
Input Output Timing						
CLKIN clock time	Tclk	-		35.7	ns	Please refer to timing table(P25)
HSD to CLKIN	Thc	-	-	1	CLKIN	
HSD width	Thwh	1	-	-	CLKIN	
VSD width	Tvwh	1	-	-	Th	
HSD period time	Th	60	63.56	67	us	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
Data set-up time	Tdsu	12	-	-	ns	DIN[23:0] to CLKIN
Data hold time	Tdhd	12	-	-	ns	DIN[23:0] to CLKIN
DEN setup time	Tesd	12	-		ns	DEN to CLKIN
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@CIR601/8bit RGB HV mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	12	20	28	Th	@CCIR656 NTSC mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	17	25	33	Th	@CCIR656 PAL mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@24bit RGB HV mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Source output stable time 1	Tst	-	25	30	us	96% final, CL=30pF, RL=2K
Gate output stable time	Tgst	-	500	1000	ns	96% final, CL=40pF
VCOMOUT output stable time	Tcst	-	4	8	us	96% final, CL=33nF, RL=100ohm
3-wire serial communication AC timing						
Serial clock	Tspck	320	-	-	ns	
SPCK pulse duty	Tscdut	40	50	60	%	Tckh/Tspck
Serial data setup time	Tisu	120	-	-	ns	
Serial data hold time	Tihd	120	-	-	ns	
Serial clock high/low	Tssw	120	-	-	ns	
Chip select distinguish	Tcd	1	-	-	us	
SPENA to VSD	Tcv	1	-	-	us	
SPENB input setup time	Teck	150	-	-	Ns	
SPENB input hold time	Tcke	150	-	-	ns	

10. Absolute Maximum Ratings

Logic supply voltage, VCI	-0.5V to +5V
Analog supply voltage, VDDA	-0.5V to +7.5V
Supply voltage, VCIP	-0.5V to +5.5V
Supply voltage, V1~V6	-0.3~VDDA+0.3
VGH~VGL	-0.3~+25V
Storage temperature	-55℃ to +125℃
Operating temperature	-20℃ to +85 ℃

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification are not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11. Chip Bump Information
11.1 Pad Location

Alignment Mark

Alignment mark dimension(unit:um)

| Left side | Right side |

115

20
25
25
25
20

20 25 25 25 20

115

20
25
25
25
20

20 25 25 25 20
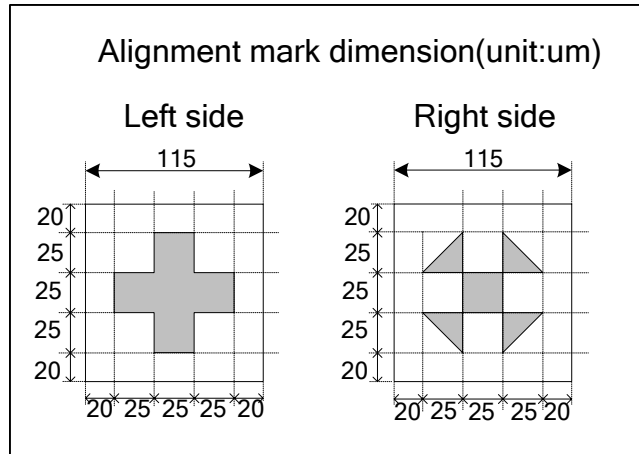
Bump Information

Symbol	Dimension(um)
B	17
B3	83
C	100
C1	127
C2	27
C4	90
D2	57
E1	21290(Max)
E2	680(Max)
E4	65(Max)
E5	57(Max)
E6	40

*Remark: Chip dimension include scribe line

11.2 Pad coordination

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
1	DUMMY	10579.575	281.5	53	G<104>	9678.75	281.5	105	G<208>	8794.9	281.5
2	G<2>	10545.6	141.5	54	G<106>	9661.75	141.5	106	G<210>	8777.925	141.5
3	G<4>	10528.6	281.5	55	G<108>	9644.75	281.5	107	G<212>	8760.925	281.5
4	G<6>	10511.6	141.5	56	G<110>	9627.75	141.5	108	G<214>	8743.925	141.5
5	G<8>	10494.6	281.5	57	G<112>	9610.75	281.5	109	G<216>	8726.925	281.5
6	G<10>	10477.6	141.5	58	G<114>	9593.775	141.5	110	G<218>	8709.925	141.5
7	G<12>	10460.6	281.5	59	G<116>	9576.775	281.5	111	G<220>	8692.925	281.5
8	G<14>	10443.6	141.5	60	G<118>	9559.775	141.5	112	G<222>	8675.925	141.5
9	G<16>	10426.6	281.5	61	G<120>	9542.775	281.5	113	G<224>	8658.925	281.5
10	G<18>	10409.625	141.5	62	G<122>	9525.775	141.5	114	G<226>	8641.95	141.5
11	G<20>	10392.625	281.5	63	G<124>	9508.775	281.5	115	G<228>	8624.95	281.5
12	G<22>	10375.625	141.5	64	G<126>	9491.775	141.5	116	G<230>	8607.95	141.5
13	G<24>	10358.625	281.5	65	G<128>	9474.775	281.5	117	G<232>	8590.95	281.5
14	G<26>	10341.625	141.5	66	G<130>	9457.8	141.5	118	G<234>	8573.95	141.5
15	G<28>	10324.625	281.5	67	G<132>	9440.8	281.5	119	G<236>	8556.95	281.5
16	G<30>	10307.625	141.5	68	G<134>	9423.8	141.5	120	G<238>	8539.95	141.5
17	G<32>	10290.625	281.5	69	G<136>	9406.8	281.5	121	G<240>	8522.95	281.5
18	G<34>	10273.65	141.5	70	G<138>	9389.8	141.5	122	COM2_L	8483.975	281.5
19	G<36>	10256.65	281.5	71	G<140>	9372.8	281.5	123	COM2_L	8449.975	281.5
20	G<38>	10239.65	141.5	72	G<142>	9355.8	141.5	124	COM2_L	8415.975	281.5
21	G<40>	10222.65	281.5	73	G<144>	9338.8	281.5	125	COM2_L	8381.975	281.5
22	G<42>	10205.65	141.5	74	G<146>	9321.825	141.5	126	COM2_L	8347.975	281.5
23	G<44>	10188.65	281.5	75	G<148>	9304.825	281.5	127	S<1>	8309	281.5
24	G<46>	10171.65	141.5	76	G<150>	9287.825	141.5	128	S<2>	8292	141.5
25	G<48>	10154.65	281.5	77	G<152>	9270.825	281.5	129	S<3>	8275	281.5
26	G<50>	10137.675	141.5	78	G<154>	9253.825	141.5	130	S<4>	8258	141.5
27	G<52>	10120.675	281.5	79	G<156>	9236.825	281.5	131	S<5>	8241	281.5
28	G<54>	10103.675	141.5	80	G<158>	9219.825	141.5	132	S<6>	8224	141.5
29	G<56>	10086.675	281.5	81	G<160>	9202.825	281.5	133	S<7>	8207	281.5
30	G<58>	10069.675	141.5	82	G<162>	9185.85	141.5	134	S<8>	8190	141.5
31	G<60>	10052.675	281.5	83	G<164>	9168.85	281.5	135	S<9>	8173.025	281.5
32	G<62>	10035.675	141.5	84	G<166>	9151.85	141.5	136	S<10>	8156.025	141.5
33	G<64>	10018.675	281.5	85	G<168>	9134.85	281.5	137	S<11>	8139.025	281.5
34	G<66>	10001.7	141.5	86	G<170>	9117.85	141.5	138	S<12>	8122.025	141.5
35	G<68>	9984.7	281.5	87	G<172>	9100.85	281.5	139	S<13>	8105.025	281.5
36	G<70>	9967.7	141.5	88	G<174>	9083.85	141.5	140	S<14>	8088.025	141.5
37	G<72>	9950.7	281.5	89	G<176>	9066.85	281.5	141	S<15>	8071.025	281.5
38	G<74>	9933.7	141.5	90	G<178>	9049.875	141.5	142	S<16>	8054.025	141.5
39	G<76>	9916.7	281.5	91	G<180>	9032.875	281.5	143	S<17>	8037.05	281.5
40	G<78>	9899.7	141.5	92	G<182>	9015.875	141.5	144	S<18>	8020.05	141.5
41	G<80>	9882.7	281.5	93	G<184>	8998.875	281.5	145	S<19>	8003.05	281.5
42	G<82>	9865.725	141.5	94	G<186>	8981.875	141.5	146	S<20>	7986.05	141.5
43	G<84>	9848.725	281.5	95	G<188>	8964.875	281.5	147	S<21>	7969.05	281.5
44	G<86>	9831.725	141.5	96	G<190>	8947.875	141.5	148	S<22>	7952.05	141.5
45	G<88>	9814.725	281.5	97	G<192>	8930.875	281.5	149	S<23>	7935.05	281.5
46	G<90>	9797.725	141.5	98	G<194>	8913.9	141.5	150	S<24>	7918.05	141.5
47	G<92>	9780.725	281.5	99	G<196>	8896.9	281.5	151	S<25>	7901.075	281.5
48	G<94>	9763.725	141.5	100	G<198>	8879.9	141.5	152	S<26>	7884.075	141.5
49	G<96>	9746.725	281.5	101	G<200>	8862.9	281.5	153	S<27>	7867.075	281.5
50	G<98>	9729.75	141.5	102	G<202>	8845.9	141.5	154	S<28>	7850.075	141.5
51	G<100>	9712.75	281.5	103	G<204>	8828.9	281.5	155	S<29>	7833.075	281.5
52	G<102>	9695.75	141.5	104	G<206>	8811.9	141.5	156	S<30>	7816.075	141.5

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
157	S<31>	7799.075	281.5	209	S<83>	6915.25	281.5	261	S<135>	6031.4	281.5
158	S<32>	7782.075	141.5	210	S<84>	6898.25	141.5	262	S<136>	6014.4	141.5
159	S<33>	7765.1	281.5	211	S<85>	6881.25	281.5	263	S<137>	5997.425	281.5
160	S<34>	7748.1	141.5	212	S<86>	6864.25	141.5	264	S<138>	5980.425	141.5
161	S<35>	7731.1	281.5	213	S<87>	6847.25	281.5	265	S<139>	5963.425	281.5
162	S<36>	7714.1	141.5	214	S<88>	6830.25	141.5	266	S<140>	5946.425	141.5
163	S<37>	7697.1	281.5	215	S<89>	6813.275	281.5	267	S<141>	5929.425	281.5
164	S<38>	7680.1	141.5	216	S<90>	6796.275	141.5	268	S<142>	5912.425	141.5
165	S<39>	7663.1	281.5	217	S<91>	6779.275	281.5	269	S<143>	5895.425	281.5
166	S<40>	7646.1	141.5	218	S<92>	6762.275	141.5	270	S<144>	5878.425	141.5
167	S<41>	7629.125	281.5	219	S<93>	6745.275	281.5	271	S<145>	5861.45	281.5
168	S<42>	7612.125	141.5	220	S<94>	6728.275	141.5	272	S<146>	5844.45	141.5
169	S<43>	7595.125	281.5	221	S<95>	6711.275	281.5	273	S<147>	5827.45	281.5
170	S<44>	7578.125	141.5	222	S<96>	6694.275	141.5	274	S<148>	5810.45	141.5
171	S<45>	7561.125	281.5	223	S<97>	6677.3	281.5	275	S<149>	5793.45	281.5
172	S<46>	7544.125	141.5	224	S<98>	6660.3	141.5	276	S<150>	5776.45	141.5
173	S<47>	7527.125	281.5	225	S<99>	6643.3	281.5	277	S<151>	5759.45	281.5
174	S<48>	7510.125	141.5	226	S<100>	6626.3	141.5	278	S<152>	5742.45	141.5
175	S<49>	7493.15	281.5	227	S<101>	6609.3	281.5	279	S<153>	5725.475	281.5
176	S<50>	7476.15	141.5	228	S<102>	6592.3	141.5	280	S<154>	5708.475	141.5
177	S<51>	7459.15	281.5	229	S<103>	6575.3	281.5	281	S<155>	5691.475	281.5
178	S<52>	7442.15	141.5	230	S<104>	6558.3	141.5	282	S<156>	5674.475	141.5
179	S<53>	7425.15	281.5	231	S<105>	6541.325	281.5	283	S<157>	5657.475	281.5
180	S<54>	7408.15	141.5	232	S<106>	6524.325	141.5	284	S<158>	5640.475	141.5
181	S<55>	7391.15	281.5	233	S<107>	6507.325	281.5	285	S<159>	5623.475	281.5
182	S<56>	7374.15	141.5	234	S<108>	6490.325	141.5	286	S<160>	5606.475	141.5
183	S<57>	7357.175	281.5	235	S<109>	6473.325	281.5	287	S<161>	5589.5	281.5
184	S<58>	7340.175	141.5	236	S<110>	6456.325	141.5	288	S<162>	5572.5	141.5
185	S<59>	7323.175	281.5	237	S<111>	6439.325	281.5	289	S<163>	5555.5	281.5
186	S<60>	7306.175	141.5	238	S<112>	6422.325	141.5	290	S<164>	5538.5	141.5
187	S<61>	7289.175	281.5	239	S<113>	6405.35	281.5	291	S<165>	5521.5	281.5
188	S<62>	7272.175	141.5	240	S<114>	6388.35	141.5	292	S<166>	5504.5	141.5
189	S<63>	7255.175	281.5	241	S<115>	6371.35	281.5	293	S<167>	5487.5	281.5
190	S<64>	7238.175	141.5	242	S<116>	6354.35	141.5	294	S<168>	5470.5	141.5
191	S<65>	7221.2	281.5	243	S<117>	6337.35	281.5	295	S<169>	5453.525	281.5
192	S<66>	7204.2	141.5	244	S<118>	6320.35	141.5	296	S<170>	5436.525	141.5
193	S<67>	7187.2	281.5	245	S<119>	6303.35	281.5	297	S<171>	5419.525	281.5
194	S<68>	7170.2	141.5	246	S<120>	6286.35	141.5	298	S<172>	5402.525	141.5
195	S<69>	7153.2	281.5	247	S<121>	6269.375	281.5	299	S<173>	5385.525	281.5
196	S<70>	7136.2	141.5	248	S<122>	6252.375	141.5	300	S<174>	5368.525	141.5
197	S<71>	7119.2	281.5	249	S<123>	6235.375	281.5	301	S<175>	5351.525	281.5
198	S<72>	7102.2	141.5	250	S<124>	6218.375	141.5	302	S<176>	5334.525	141.5
199	S<73>	7085.225	281.5	251	S<125>	6201.375	281.5	303	S<177>	5317.55	281.5
200	S<74>	7068.225	141.5	252	S<126>	6184.375	141.5	304	S<178>	5300.55	141.5
201	S<75>	7051.225	281.5	253	S<127>	6167.375	281.5	305	S<179>	5283.55	281.5
202	S<76>	7034.225	141.5	254	S<128>	6150.375	141.5	306	S<180>	5266.55	141.5
203	S<77>	7017.225	281.5	255	S<129>	6133.4	281.5	307	S<181>	5249.55	281.5
204	S<78>	7000.225	141.5	256	S<130>	6116.4	141.5	308	S<182>	5232.55	141.5
205	S<79>	6983.225	281.5	257	S<131>	6099.4	281.5	309	S<183>	5215.55	281.5
206	S<80>	6966.225	141.5	258	S<132>	6082.4	141.5	310	S<184>	5198.55	141.5
207	S<81>	6949.25	281.5	259	S<133>	6065.4	281.5	311	S<185>	5181.575	281.5
208	S<82>	6932.25	141.5	260	S<134>	6048.4	141.5	312	S<186>	5164.575	141.5

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
313	S<187>	5147.575	281.5	365	S<239>	4263.725	281.5	417	S<291>	3379.9	281.5
314	S<188>	5130.575	141.5	366	S<240>	4246.725	141.5	418	S<292>	3362.9	141.5
315	S<189>	5113.575	281.5	367	S<241>	4229.75	281.5	419	S<293>	3345.9	281.5
316	S<190>	5096.575	141.5	368	S<242>	4212.75	141.5	420	S<294>	3328.9	141.5
317	S<191>	5079.575	281.5	369	S<243>	4195.75	281.5	421	S<295>	3311.9	281.5
318	S<192>	5062.575	141.5	370	S<244>	4178.75	141.5	422	S<296>	3294.9	141.5
319	S<193>	5045.6	281.5	371	S<245>	4161.75	281.5	423	S<297>	3277.925	281.5
320	S<194>	5028.6	141.5	372	S<246>	4144.75	141.5	424	S<298>	3260.925	141.5
321	S<195>	5011.6	281.5	373	S<247>	4127.75	281.5	425	S<299>	3243.925	281.5
322	S<196>	4994.6	141.5	374	S<248>	4110.75	141.5	426	S<300>	3226.925	141.5
323	S<197>	4977.6	281.5	375	S<249>	4093.775	281.5	427	S<301>	3209.925	281.5
324	S<198>	4960.6	141.5	376	S<250>	4076.775	141.5	428	S<302>	3192.925	141.5
325	S<199>	4943.6	281.5	377	S<251>	4059.775	281.5	429	S<303>	3175.925	281.5
326	S<200>	4926.6	141.5	378	S<252>	4042.775	141.5	430	S<304>	3158.925	141.5
327	S<201>	4909.625	281.5	379	S<253>	4025.775	281.5	431	S<305>	3141.95	281.5
328	S<202>	4892.625	141.5	380	S<254>	4008.775	141.5	432	S<306>	3124.95	141.5
329	S<203>	4875.625	281.5	381	S<255>	3991.775	281.5	433	S<307>	3107.95	281.5
330	S<204>	4858.625	141.5	382	S<256>	3974.775	141.5	434	S<308>	3090.95	141.5
331	S<205>	4841.625	281.5	383	S<257>	3957.8	281.5	435	S<309>	3073.95	281.5
332	S<206>	4824.625	141.5	384	S<258>	3940.8	141.5	436	S<310>	3056.95	141.5
333	S<207>	4807.625	281.5	385	S<259>	3923.8	281.5	437	S<311>	3039.95	281.5
334	S<208>	4790.625	141.5	386	S<260>	3906.8	141.5	438	S<312>	3022.95	141.5
335	S<209>	4773.65	281.5	387	S<261>	3889.8	281.5	439	S<313>	3005.975	281.5
336	S<210>	4756.65	141.5	388	S<262>	3872.8	141.5	440	S<314>	2988.975	141.5
337	S<211>	4739.65	281.5	389	S<263>	3855.8	281.5	441	S<315>	2971.975	281.5
338	S<212>	4722.65	141.5	390	S<264>	3838.8	141.5	442	S<316>	2954.975	141.5
339	S<213>	4705.65	281.5	391	S<265>	3821.825	281.5	443	S<317>	2937.975	281.5
340	S<214>	4688.65	141.5	392	S<266>	3804.825	141.5	444	S<318>	2920.975	141.5
341	S<215>	4671.65	281.5	393	S<267>	3787.825	281.5	445	S<319>	2903.975	281.5
342	S<216>	4654.65	141.5	394	S<268>	3770.825	141.5	446	S<320>	2886.975	141.5
343	S<217>	4637.675	281.5	395	S<269>	3753.825	281.5	447	S<321>	2870	281.5
344	S<218>	4620.675	141.5	396	S<270>	3736.825	141.5	448	S<322>	2853	141.5
345	S<219>	4603.675	281.5	397	S<271>	3719.825	281.5	449	S<323>	2836	281.5
346	S<220>	4586.675	141.5	398	S<272>	3702.825	141.5	450	S<324>	2819	141.5
347	S<221>	4569.675	281.5	399	S<273>	3685.85	281.5	451	S<325>	2802	281.5
348	S<222>	4552.675	141.5	400	S<274>	3668.85	141.5	452	S<326>	2785	141.5
349	S<223>	4535.675	281.5	401	S<275>	3651.85	281.5	453	S<327>	2768	281.5
350	S<224>	4518.675	141.5	402	S<276>	3634.85	141.5	454	S<328>	2751	141.5
351	S<225>	4501.7	281.5	403	S<277>	3617.85	281.5	455	S<329>	2734.025	281.5
352	S<226>	4484.7	141.5	404	S<278>	3600.85	141.5	456	S<330>	2717.025	141.5
353	S<227>	4467.7	281.5	405	S<279>	3583.85	281.5	457	S<331>	2700.025	281.5
354	S<228>	4450.7	141.5	406	S<280>	3566.85	141.5	458	S<332>	2683.025	141.5
355	S<229>	4433.7	281.5	407	S<281>	3549.875	281.5	459	S<333>	2666.025	281.5
356	S<230>	4416.7	141.5	408	S<282>	3532.875	141.5	460	S<334>	2649.025	141.5
357	S<231>	4399.7	281.5	409	S<283>	3515.875	281.5	461	S<335>	2632.025	281.5
358	S<232>	4382.7	141.5	410	S<284>	3498.875	141.5	462	S<336>	2615.025	141.5
359	S<233>	4365.725	281.5	411	S<285>	3481.875	281.5	463	S<337>	2598.05	281.5
360	S<234>	4348.725	141.5	412	S<286>	3464.875	141.5	464	S<338>	2581.05	141.5
361	S<235>	4331.725	281.5	413	S<287>	3447.875	281.5	465	S<339>	2564.05	281.5
362	S<236>	4314.725	141.5	414	S<288>	3430.875	141.5	466	S<340>	2547.05	141.5
363	S<237>	4297.725	281.5	415	S<289>	3413.9	281.5	467	S<341>	2530.05	281.5
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Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
469	S<343>	2496.05	281.5	521	S<395>	1612.225	281.5	573	S<447>	728.375	281.5
470	S<344>	2479.05	141.5	522	S<396>	1595.225	141.5	574	S<448>	711.375	141.5
471	S<345>	2462.075	281.5	523	S<397>	1578.225	281.5	575	S<449>	694.4	281.5
472	S<346>	2445.075	141.5	524	S<398>	1561.225	141.5	576	S<450>	677.4	141.5
473	S<347>	2428.075	281.5	525	S<399>	1544.225	281.5	577	S<451>	660.4	281.5
474	S<348>	2411.075	141.5	526	S<400>	1527.225	141.5	578	S<452>	643.4	141.5
475	S<349>	2394.075	281.5	527	S<401>	1510.25	281.5	579	S<453>	626.4	281.5
476	S<350>	2377.075	141.5	528	S<402>	1493.25	141.5	580	S<454>	609.4	141.5
477	S<351>	2360.075	281.5	529	S<403>	1476.25	281.5	581	S<455>	592.4	281.5
478	S<352>	2343.075	141.5	530	S<404>	1459.25	141.5	582	S<456>	575.4	141.5
479	S<353>	2326.1	281.5	531	S<405>	1442.25	281.5	583	S<457>	558.425	281.5
480	S<354>	2309.1	141.5	532	S<406>	1425.25	141.5	584	S<458>	541.425	141.5
481	S<355>	2292.1	281.5	533	S<407>	1408.25	281.5	585	S<459>	524.425	281.5
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483	S<357>	2258.1	281.5	535	S<409>	1374.275	281.5	587	S<461>	490.425	281.5
484	S<358>	2241.1	141.5	536	S<410>	1357.275	141.5	588	S<462>	473.425	141.5
485	S<359>	2224.1	281.5	537	S<411>	1340.275	281.5	589	S<463>	456.425	281.5
486	S<360>	2207.1	141.5	538	S<412>	1323.275	141.5	590	S<464>	439.425	141.5
487	S<361>	2190.125	281.5	539	S<413>	1306.275	281.5	591	S<465>	422.45	281.5
488	S<362>	2173.125	141.5	540	S<414>	1289.275	141.5	592	S<466>	405.45	141.5
489	S<363>	2156.125	281.5	541	S<415>	1272.275	281.5	593	S<467>	388.45	281.5
490	S<364>	2139.125	141.5	542	S<416>	1255.275	141.5	594	S<468>	371.45	141.5
491	S<365>	2122.125	281.5	543	S<417>	1238.3	281.5	595	S<469>	354.45	281.5
492	S<366>	2105.125	141.5	544	S<418>	1221.3	141.5	596	S<470>	337.45	141.5
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494	S<368>	2071.125	141.5	546	S<420>	1187.3	141.5	598	S<472>	303.45	141.5
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496	S<370>	2037.15	141.5	548	S<422>	1153.3	141.5	600	S<474>	269.475	141.5
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500	S<374>	1969.15	141.5	552	S<426>	1085.325	141.5	604	S<478>	201.475	141.5
501	S<375>	1952.15	281.5	553	S<427>	1068.325	281.5	605	S<479>	184.475	281.5
502	S<376>	1935.15	141.5	554	S<428>	1051.325	141.5	606	S<480>	167.475	141.5
503	S<377>	1918.175	281.5	555	S<429>	1034.325	281.5	607	DUMMY	136.5	281.5
504	S<378>	1901.175	141.5	556	S<430>	1017.325	141.5	608	DUMMY	102.5	281.5
505	S<379>	1884.175	281.5	557	S<431>	1000.325	281.5	609	DUMMY	68.5	281.5
506	S<380>	1867.175	141.5	558	S<432>	983.325	141.5	610	DUMMY	34.5	281.5
507	S<381>	1850.175	281.5	559	S<433>	966.35	281.5	611	DUMMY	0	281.5
508	S<382>	1833.175	141.5	560	S<434>	949.35	141.5	612	DUMMY	-34.5	281.5
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511	S<385>	1782.2	281.5	563	S<437>	898.35	281.5	615	DUMMY	-136.5	281.5
512	S<386>	1765.2	141.5	564	S<438>	881.35	141.5	616	S<481>	-167.475	141.5
513	S<387>	1748.2	281.5	565	S<439>	864.35	281.5	617	S<482>	-184.475	281.5
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515	S<389>	1714.2	281.5	567	S<441>	830.375	281.5	619	S<484>	-218.475	281.5
516	S<390>	1697.2	141.5	568	S<442>	813.375	141.5	620	S<485>	-235.475	141.5
517	S<391>	1680.2	281.5	569	S<443>	796.375	281.5	621	S<486>	-252.475	281.5
518	S<392>	1663.2	141.5	570	S<444>	779.375	141.5	622	S<487>	-269.475	141.5
519	S<393>	1646.225	281.5	571	S<445>	762.375	281.5	623	S<488>	-286.475	281.5
520	S<394>	1629.225	141.5	572	S<446>	745.375	141.5	624	S<489>	-303.45	141.5

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
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626	S<491>	-337.45	141.5	678	S<543>	-1221.3	14	730	S<595>	-2105.125	141.5
627	S<492>	-354.45	281.5	679	S<544>	-1238.3	28	731	S<596>	-2122.125	281.5
628	S<493>	-371.45	141.5	680	S<545>	-1255.275	14	732	S<597>	-2139.125	141.5
629	S<494>	-388.45	281.5	681	S<546>	-1272.275	28	733	S<598>	-2156.125	281.5
630	S<495>	-405.45	141.5	682	S<547>	-1289.275	14	734	S<599>	-2173.125	141.5
631	S<496>	-422.45	281.5	683	S<548>	-1306.275	28	735	S<600>	-2190.125	281.5
632	S<497>	-439.425	141.5	684	S<549>	-1323.275	14	736	S<601>	-2207.1	141.5
633	S<498>	-456.425	281.5	685	S<550>	-1340.275	28	737	S<602>	-2224.1	281.5
634	S<499>	-473.425	141.5	686	S<551>	-1357.275	14	738	S<603>	-2241.1	141.5
635	S<500>	-490.425	281.5	687	S<552>	-1374.275	28	739	S<604>	-2258.1	281.5
636	S<501>	-507.425	141.5	688	S<553>	-1391.25	14	740	S<605>	-2275.1	141.5
637	S<502>	-524.425	281.5	689	S<554>	-1408.25	28	741	S<606>	-2292.1	281.5
638	S<503>	-541.425	141.5	690	S<555>	-1425.25	14	742	S<607>	-2309.1	141.5
639	S<504>	-558.425	281.5	691	S<556>	-1442.25	28	743	S<608>	-2326.1	281.5
640	S<505>	-575.4	141.5	692	S<557>	-1459.25	14	744	S<609>	-2343.075	141.5
641	S<506>	-592.4	281.5	693	S<558>	-1476.25	28	745	S<610>	-2360.075	281.5
642	S<507>	-609.4	141.5	694	S<559>	-1493.25	14	746	S<611>	-2377.075	141.5
643	S<508>	-626.4	281.5	695	S<560>	-1510.25	28	747	S<612>	-2394.075	281.5
644	S<509>	-643.4	141.5	696	S<561>	-1527.225	14	748	S<613>	-2411.075	141.5
645	S<510>	-660.4	281.5	697	S<562>	-1544.225	28	749	S<614>	-2428.075	281.5
646	S<511>	-677.4	141.5	698	S<563>	-1561.225	14	750	S<615>	-2445.075	141.5
647	S<512>	-694.4	281.5	699	S<564>	-1578.225	28	751	S<616>	-2462.075	281.5
648	S<513>	-711.375	141.5	700	S<565>	-1595.225	14	752	S<617>	-2479.05	141.5
649	S<514>	-728.375	281.5	701	S<566>	-1612.225	28	753	S<618>	-2496.05	281.5
650	S<515>	-745.375	141.5	702	S<567>	-1629.225	14	754	S<619>	-2513.05	141.5
651	S<516>	-762.375	281.5	703	S<568>	-1646.225	28	755	S<620>	-2530.05	281.5
652	S<517>	-779.375	141.5	704	S<569>	-1663.2	14	756	S<621>	-2547.05	141.5
653	S<518>	-796.375	281.5	705	S<570>	-1680.2	28	757	S<622>	-2564.05	281.5
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655	S<520>	-830.375	281.5	707	S<572>	-1714.2	28	759	S<624>	-2598.05	281.5
656	S<521>	-847.35	141.5	708	S<573>	-1731.2	14	760	S<625>	-2615.025	141.5
657	S<522>	-864.35	281.5	709	S<574>	-1748.2	28	761	S<626>	-2632.025	281.5
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660	S<525>	-915.35	141.5	712	S<577>	-1799.175	14	764	S<629>	-2683.025	141.5
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673	S<538>	-1136.3	281.5	725	S<590>	-2020.15	28	777	S<642>	-2903.975	281.5
674	S<539>	-1153.3	141.5	726	S<591>	-2037.15	14	778	S<643>	-2920.975	141.5
675	S<540>	-1170.3	281.5	727	S<592>	-2054.15	28	779	S<644>	-2937.975	281.5
676	S<541>	-1187.3	141.5	728	S<593>	-2071.125	14	780	S<645>	-2954.975	141.5

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
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788	S<653>	-3090.95	141.5	840	S<705>	-3974.775	14	892	S<757>	-4858.625	141.5
789	S<654>	-3107.95	281.5	841	S<706>	-3991.775	28	893	S<758>	-4875.625	281.5
790	S<655>	-3124.95	141.5	842	S<707>	-4008.775	14	894	S<759>	-4892.625	141.5
791	S<656>	-3141.95	281.5	843	S<708>	-4025.775	28	895	S<760>	-4909.625	281.5
792	S<657>	-3158.925	141.5	844	S<709>	-4042.775	14	896	S<761>	-4926.6	141.5
793	S<658>	-3175.925	281.5	845	S<710>	-4059.775	28	897	S<762>	-4943.6	281.5
794	S<659>	-3192.925	141.5	846	S<711>	-4076.775	14	898	S<763>	-4960.6	141.5
795	S<660>	-3209.925	281.5	847	S<712>	-4093.775	28	899	S<764>	-4977.6	281.5
796	S<661>	-3226.925	141.5	848	S<713>	-4110.75	14	900	S<765>	-4994.6	141.5
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800	S<665>	-3294.9	141.5	852	S<717>	-4178.75	14	904	S<769>	-5062.575	141.5
801	S<666>	-3311.9	281.5	853	S<718>	-4195.75	28	905	S<770>	-5079.575	281.5
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810	S<675>	-3464.875	141.5	862	S<727>	-4348.725	14	914	S<779>	-5232.55	141.5
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812	S<677>	-3498.875	141.5	864	S<729>	-4382.7	14	916	S<781>	-5266.55	141.5
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820	S<685>	-3634.85	141.5	872	S<737>	-4518.675	14	924	S<789>	-5402.525	141.5
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823	S<688>	-3685.85	281.5	875	S<740>	-4569.675	28	927	S<792>	-5453.525	281.5
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825	S<690>	-3719.825	281.5	877	S<742>	-4603.675	28	929	S<794>	-5487.5	281.5
826	S<691>	-3736.825	141.5	878	S<743>	-4620.675	14	930	S<795>	-5504.5	141.5
827	S<692>	-3753.825	281.5	879	S<744>	-4637.675	28	931	S<796>	-5521.5	281.5
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830	S<695>	-3804.825	141.5	882	S<747>	-4688.65	14	934	S<799>	-5572.5	141.5
831	S<696>	-3821.825	281.5	883	S<748>	-4705.65	28	935	S<800>	-5589.5	281.5
832	S<697>	-3838.8	141.5	884	S<749>	-4722.65	14	936	S<801>	-5606.475	141.5

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
937	S<802>	-5623.475	281.5	989	S<854>	-6507.325	281.5	1041	S<906>	-7391.15	281.5
938	S<803>	-5640.475	141.5	990	S<855>	-6524.325	141.5	1042	S<907>	-7408.15	141.5
939	S<804>	-5657.475	281.5	991	S<856>	-6541.325	281.5	1043	S<908>	-7425.15	281.5
940	S<805>	-5674.475	141.5	992	S<857>	-6558.3	141.5	1044	S<909>	-7442.15	141.5
941	S<806>	-5691.475	281.5	993	S<858>	-6575.3	281.5	1045	S<910>	-7459.15	281.5
942	S<807>	-5708.475	141.5	994	S<859>	-6592.3	141.5	1046	S<911>	-7476.15	141.5
943	S<808>	-5725.475	281.5	995	S<860>	-6609.3	281.5	1047	S<912>	-7493.15	281.5
944	S<809>	-5742.45	141.5	996	S<861>	-6626.3	141.5	1048	S<913>	-7510.125	141.5
945	S<810>	-5759.45	281.5	997	S<862>	-6643.3	281.5	1049	S<914>	-7527.125	281.5
946	S<811>	-5776.45	141.5	998	S<863>	-6660.3	141.5	1050	S<915>	-7544.125	141.5
947	S<812>	-5793.45	281.5	999	S<864>	-6677.3	281.5	1051	S<916>	-7561.125	281.5
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949	S<814>	-5827.45	281.5	1001	S<866>	-6711.275	281.5	1053	S<918>	-7595.125	281.5
950	S<815>	-5844.45	141.5	1002	S<867>	-6728.275	141.5	1054	S<919>	-7612.125	141.5
951	S<816>	-5861.45	281.5	1003	S<868>	-6745.275	281.5	1055	S<920>	-7629.125	281.5
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955	S<820>	-5929.425	281.5	1007	S<872>	-6813.275	281.5	1059	S<924>	-7697.1	281.5
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957	S<822>	-5963.425	281.5	1009	S<874>	-6847.25	281.5	1061	S<926>	-7731.1	281.5
958	S<823>	-5980.425	141.5	1010	S<875>	-6864.25	141.5	1062	S<927>	-7748.1	141.5
959	S<824>	-5997.425	281.5	1011	S<876>	-6881.25	281.5	1063	S<928>	-7765.1	281.5
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967	S<832>	-6133.4	281.5	1019	S<884>	-7017.225	281.5	1071	S<936>	-7901.075	281.5
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983	S<848>	-6405.35	281.5	1035	S<900>	-7289.175	281.5	1087	S<952>	-8173.025	281.5
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Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
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1100	COM1_L	-8483.975	281.5	1152	G<137>	-9389.8	141.5	1204	G<33>	-10273.65	141.
1101	G<239>	-8522.95	281.5	1153	G<135>	-9406.8	281.5	1205	G<31>	-10290.625	281.
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1103	G<235>	-8556.95	281.5	1155	G<131>	-9440.8	281.5	1207	G<27>	-10324.625	281.
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Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
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1259	DUMMY	-5715	-	1310	TP6	762	-210	1361	DIN<5>	7239	-210
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1266	vssa!	-4826	-	1317	TP1	1651	-210	1368	vdd!	8128	-210
1267	DUMMY	-4699	-	1318	DUMMY	1778	-210	1369	vdd!	8255	-210
1268	VCOMOUT	-4572	-	1319	TP0	1905	-210	1370	vdd!	8382	-210
1269	VCOMOUT	-4445	-	1320	vcc!	2032	-210	1371	vss!	8509	-210
1270	VCOMOUT	-4318	-	1321	vcc!	2159	-210	1372	vss!	8636	-210
1271	VINT1	-4191	-	1322	vcc!	2286	-210	1373	vss!	8763	-210
1272	VINT1	-4064	-	1323	vssa!	2413	-210	1374	COM2_L	8890	-210
1273	VINT1	-3937	-	1324	vssa!	2540	-210	1375	COM2_L	9017	-210
1274	DUMMY	-3810	-	1325	vssa!	2667	-210	1376	DRV	9144	-210
1275	VCOMAC	-3683	-	1326	vss!	2794	-210	1377	DRV	9271	-210
1276	VCOMAC	-3556	-	1327	vss!	2921	-210	1378	FB_PN	9398	-210
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1282	POL	-2794	-	1333	DUMMY	3683	-210	1384	VINT1	10160	-210
1283	TOSC	-2667	-	1334	SPDA	3810	-210	1385	VINT1	10287	-210
1284	VPSW	-2540	-	1335	SPSW	3937	-210	1386	DUMMY	10412	-210
1285	DUMMY	-2413	-	1336	PINCTLB	4064	-210				
1286	TP18	-2286	-	1337	SPCK	4191	-210				
1287	TP17	-2159	-	1338	SPENB	4318	-210				
1288	TP16	-2032	-	1339	DEN	4445	-210				
1289	TP15	-1905	-	1340	HSD	4572	-210				
1290	DUMMY	-1778	-	1341	VSD	4699	-210				
1291	TP14	-1651	-	1342	CLKIN	4826	-210				
1292	TP13	-1524	-	1343	DIN<23>	4953	-210				
1293	DUMMY	-1397	-	1344	DIN<22>	5080	-210				
1294	TP12	-1270	-	1345	DIN<21>	5207	-210				
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1297	TP10	-889	-	1348	DIN<18>	5588	-210				
1298	TP9	-762	-	1349	DIN<17>	5715	-210				
1299	TP8	-635	-	1350	DIN<16>	5842	-210				

Revision history

Version No	Date	Page	Introduction
0.1			New build
0.2	20120109		Update register
0.3	20120911	18	Update register