FT5x46i

True Multi-Touch Capacitive Touch Panel Controller

INTRODUCTION

The FT5x46i is single-chip capacitive touch panel controllers with built-in enhanced Micro-controller unit (MCU).It provides the benefits of full screen common mode scan technology,fast response time and high level of accuracy. It is designed for single layer sensor pattern touch panel application.

FEATURES

- Mutual Capacitive Sensing Techniques
- 5346i Supports up to 13TX + 20RX
- 5446i Supports up to 15TX + 24RX
- Support up to 10 fingers
- High immunity to inductive power noise
- Automatic mode switching (Active, Monitor,Sleep)
- Support >100Hz sampling rate
- Auto-calibration
- Support IIC (up to 400kbits/sec) interface
- Power
  - 2.75 to 3.6V Operating Voltage
  - IOVCC(Ext.or Int.) supports from 1.8V to 3.6V
- Built-in 64KB Flash
- Single Channel(TX or RX)resistance: Up to 100K Ω
- Single Channel (transmit/receive) Capacitance: 40pF
- 12-Bit ADC Accuracy
- Features “short I/O ” testing for sense pins
- Supports various type of panels with no ground shielding layer
- 3 Operating Modes
  - Active
  - Monitor
  - Sleep
- Operating Temperature Range: -40°C to +85°C
- Package:
  - QFN56L 6x6x0.6mm, 0.35mm/pitch

TABLE OF CONTENTS

1 OVERVIEW

1.1 Typical Applications

FT5x46i accommodates a wide range of applications with a set of buttons up to a 2D touch sensing device. It ‘s powerful design for below applications.

- Mobile phones
- Navigation systems, GPS
- Game consoles
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras

FT5x46i support various Touch Panel, the spec is listed in the following table,

Part Number	Package	TX	RX	Total Channels	Recommended TP Size (16:9)
FT5346i	QFN 56L 6x6x0.6mm Pitch =0.35mm	13	20	33	≤5.5inch
FT5446i		15	24	39	≤7.0inch

2 FUNCTIONAL DESCRIPTION

2.1 Architectural Overview

Figure2-1 shows the overall architecture for the FT5x46i.

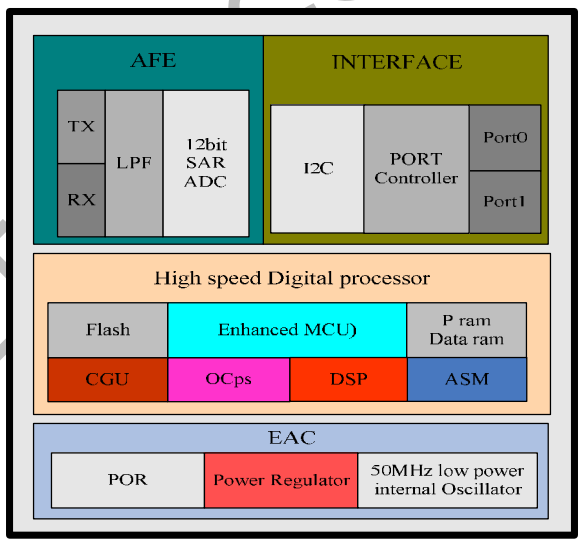


Figure 2-1 System Architecture Diagram

The FT5x46i is comprised of five main functional parts listed below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. It includes both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces.

- Enhanced MCU with DSP accelerator

For the Enhanced MCU, larger program and data memories are supported. Furthermore, a Flash memory is implemented to store programs and some key parameters.
Complex signal processing algorithms are implemented by MCU and DSP accelerator to detect the touches

reliably and efficiently. Communication protocol software is also implemented in this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RSTN: an external low signal reset the chip. The port is also use to wake up the FT5x46i from the Sleep mode.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply
- Power On Reset (POR) is active until VDDD is higher than some level and hold decades of μs.

2.2 MCU

This section describes some critical features and operations supported by the enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- A DSP accelerator cooperates with MCU to process the complex algorithms
- Timer: A number of timers are available to generate different clocks
- Clock Manager: To control various clocks under different operation conditions of the system

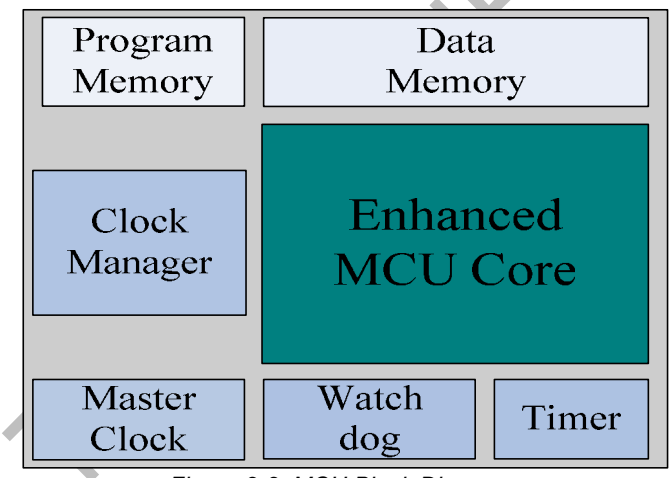


Figure 2-2 MCU Block Diagram

2.3 Operation Modes

FT5x46i offers following three modes:

- **Active Mode**

When in this mode, FT5x46i actively scans the panel. The default scan rate is 100 frames per second. The host processor can configure it to speed up or to slow down.

- **Monitor Mode**

In this mode, FT5x46i scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. In this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5x46i shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- **Sleep Mode**

In this mode, the chip is set in a power down mode. It shall only respond to the “RESET” signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

2.4 Host Interface

Figure 2-3 shows the interface between a host processor and FT5x46i. This interface consists of the following

three sets of signals:

- Serial Interface
- Interrupt from FT5x46i to the Host
- Reset Signal from the Host to FT5x46i

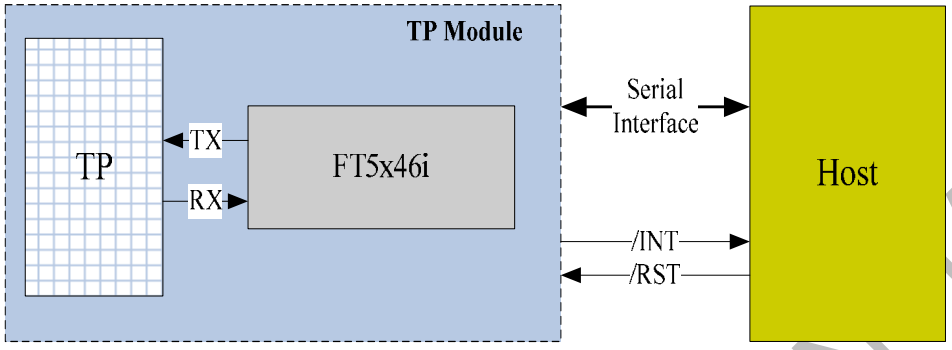


Figure 2-3 Host Interface Diagram

The serial interface of FT5X46I is I2C. The detail of the interface is described in detail in Section 2.5. The interrupt signal (/INT) is used for FT5x46i to inform the host that data are ready for the host to receive. The /RST signal is used for the host to wake up FT5x46i from the Sleep mode. After resetting, FT5x46i shall enter the Active mode.

2.5 Serial Interface

FT5x46i supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4**.

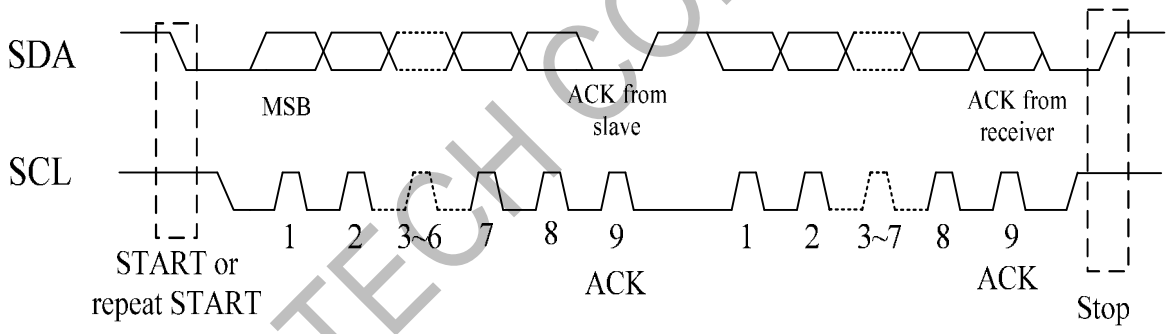


Figure 2-4 I2C Serial Data Transfer Format

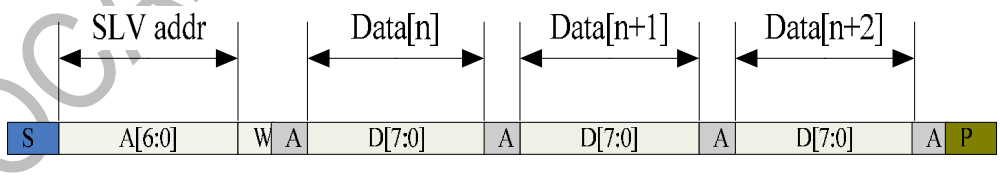


Figure 2-5 I2C master write, slave read

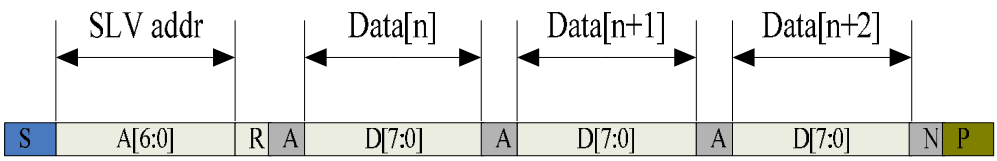


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup time for STOP condition	0.6		us
Rise time of both SDA and SCL signals	20	300	ns
Fall time of both SDA and SCL signals	20x (VDD/5.5V)	300	ns

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDD3 – VSS	2.75 ~ 3.6	V	1
I/O Digital Voltage	IOVCC	1.71~3.6	V	1
Operating Temperature	Topr	-40 ~ +85	℃	1
Storage Temperature	Tstg	-55 ~ +150	℃	1

Notes

1. If used beyond the absolute maximum ratings, FT5x46i may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDD (high) ≥VSSA (low)

3.2 DC Characteristics

Table 3-2 DC Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC	
Input low –level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high –level voltage	VOH	V	IOH=3mA	0.7 x IOVCC	--	--	
Output low –level voltage	VOL	V	IOL=4.5mA	--	--	0.3 x IOVCC	
I/O leakage current	ILI	uA	Vin=0~VDD3	-1	--	1	
Current consumption （Normal operation mode）	Ioprr	mA	VDD3 = 3V Ta=25℃	--	11	--	
Current consumption （Monitor mode）	Imon	mA	VDD3 = 3V Ta=25℃	--	0.43	--	
Current consumption （Sleep mode）	Islp	uA	VDD3 = 3V Ta=25℃	--	42	--	
Step-up output voltage	VDD5	V	VDD3= 2.8V		0.25		
Step-up output voltage	VDD10	V	VDD3= 2.8V		0.5		
Output voltage	VDD5	V	VDD3= 2.8V	5		6.25	
Output voltage	VDD10	V	VDD3= 2.8V	7		11.5	
Power Supply voltage	VDD3	V		2.7	--	3.6	

Notes: This consumption data is intended for design guidance only. Actual current will depend on the particular sensor design and firmware options.

3.3 AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3 = 2.8V; Ta=25℃	49	50	51	

Table 3-3 AC Characteristics of TX & RX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		100	150	400	KHz	
TX output rise time	Ttxr		--	TBD	--	nS	
TX output fall time	Ttxf		--	TBD	--	nS	
RX input voltage	Trxi		1.2	TBD	1.6	V	

3.4 I/O Ports Circuits

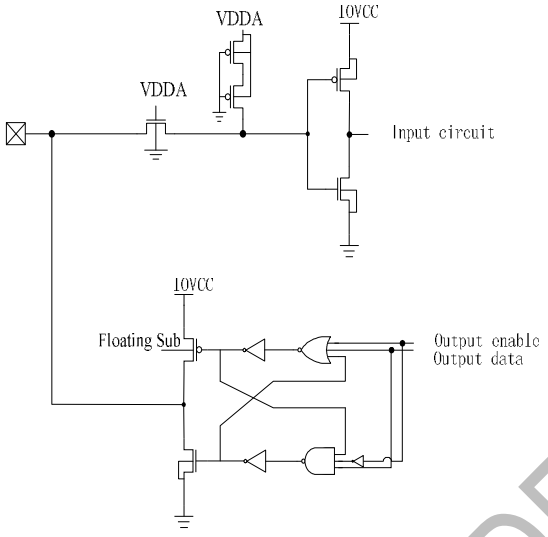


Figure 3-1 General Purpose *In/Out Port Circuit*.

The input/output property can be configured via firmware setting. The firmware can also control its output behavior as push-pull or as open-drain that SDA of I2C interface is required.

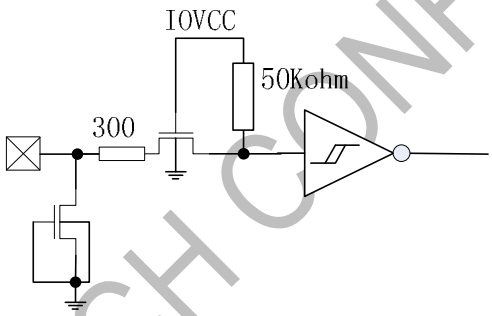


Figure 3-2 Reset Input Port Circuits

3.5 POWER ON/Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

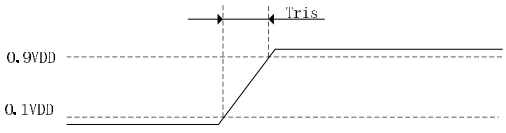


Figure 3-3 Power on time

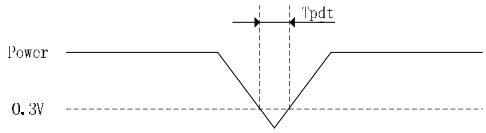


Figure 3-4 Power Cycle requirement

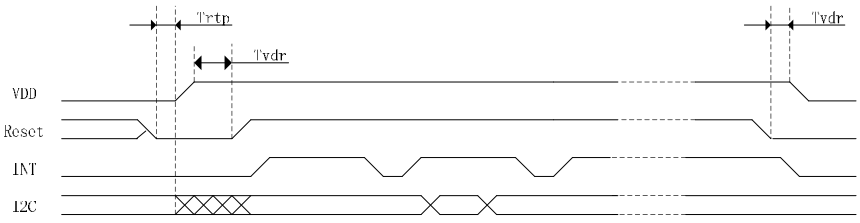


Figure 3-5 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

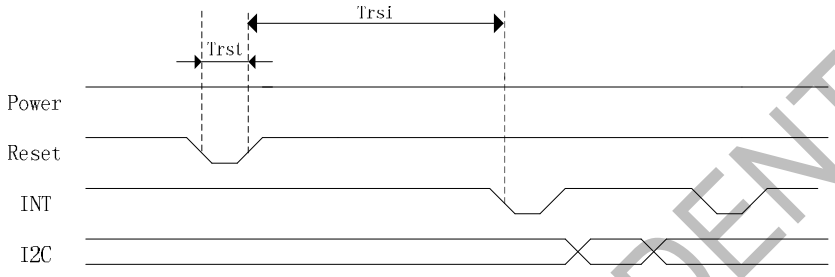


Figure 3-6 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tpon	Time of starting to report point after powering on	--	200	ms
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	1	--	ms

4 PIN CONFIGURATIONS

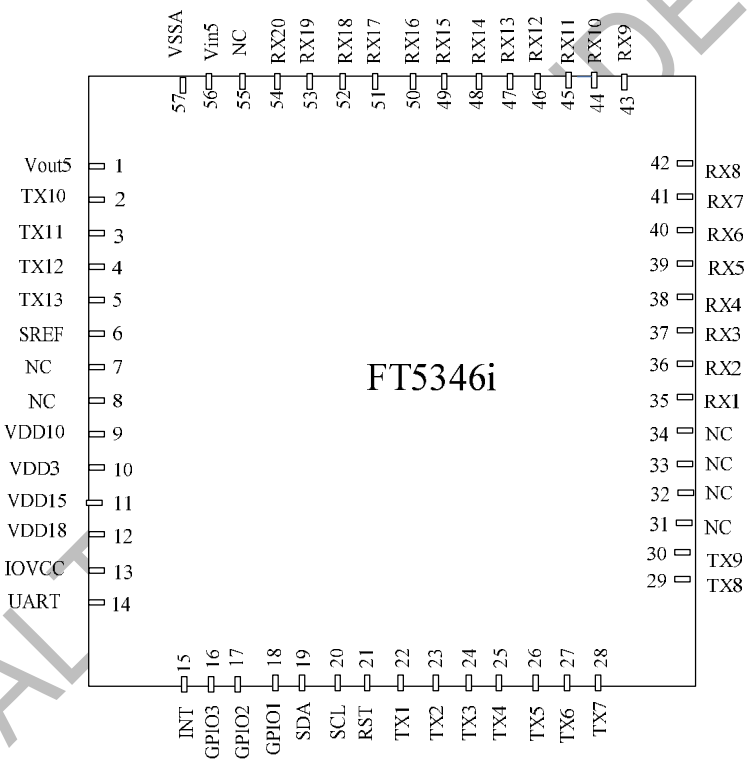
Pin List of FT5x46i

Table 4-1 Pin Definition

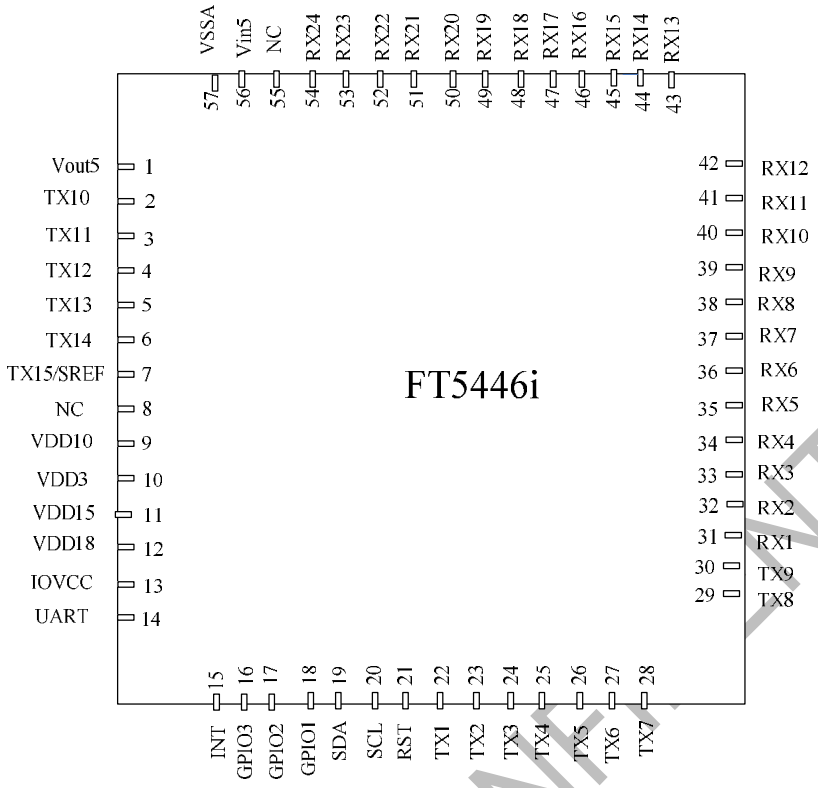
Name	Pin No. 5346i	Pin No. 5446i	Type	Description
RX24		54	I	Receiver input pins
RX23		53	I	Receiver input pins
RX22		52	I	Receiver input pins
RX21		51	I	Receiver input pins
RX20	54	50	I	Receiver input pins
RX19	53	49	I	Receiver input pins
RX18	52	48	I	Receiver input pins
RX17	51	47	I	Receiver input pins
RX16	50	46	I	Receiver input pins
RX15	49	45	I	Receiver input pins

RX14	48	44	I	Receiver input pins
RX13	47	43	I	Receiver input pins
RX12	46	42	I	Receiver input pins
RX11	45	41	I	Receiver input pins
RX10	44	40	I	Receiver input pins
RX9	43	39	I	Receiver input pins
RX8	42	38	I	Receiver input pins
RX7	41	37	I	Receiver input pins
RX6	40	36	I	Receiver input pins
RX5	39	35	I	Receiver input pins
RX4	38	34	I	Receiver input pins
RX3	37	33	I	Receiver input pins
RX2	36	32	I	Receiver input pins
RX1	35	31	I	Receiver input pins
NC		55	NC	NC
VDD5_IN	56	56	PWR	internal generated 5V power supply, A 1μF ceramic capacitor to ground is required.
VSSA	57	57	PWR	Analog ground
VDD5 Out	1	1	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
TX10	2	2	O	Transmit output pin
TX11	3	3	O	Transmit output pin
TX12	4	4	O	Transmit output pin
TX13	5	5	O	Transmit output pin
TX14		6	O	Transmit output pin
TX15/SREF	6	7	O	Transmit output pin / Sensor reference channel
NC		8	NC	NC
VDD10	9	9	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
VDD3	10	10	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
VDD15	11	11	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
VDD18	12	12	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
IOVCC	13	13	PWR	I/O power supply
UART	14	14	I/O	General Purpose Input/Output port
INT	15	15	I/O	Interrupt request to the host, or Wakeup request from the host.
GPIO3	16	16	I/O	General Purpose Input/Output port
GPIO2	17	17	I/O	General Purpose Input/Output port Support PS2_Data
GPIO1	18	18	I/O	General Purpose Input/Output port Support PS2_CLK
SDA	19	19	I/O	I2C data input and output
SCL	20	20	I/O	I2C clock input

RSTN	21	21	I	External Reset, Low is active
TX1	22	22	O	Transmit output pin
TX2	23	23	O	Transmit output pin
TX3	24	24	O	Transmit output pin
TX4	25	25	O	Transmit output pin
TX5	26	26	O	Transmit output pin
TX6	27	27	O	Transmit output pin
TX7	28	28	O	Transmit output pin
TX8	29	29	O	Transmit output pin
TX9	30	30	O	Transmit output pin



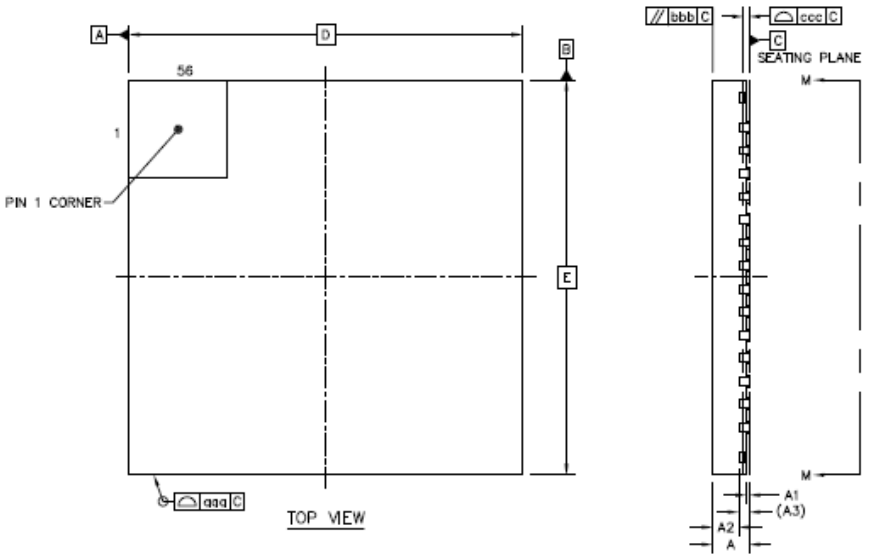
FT5346i Package Diagram

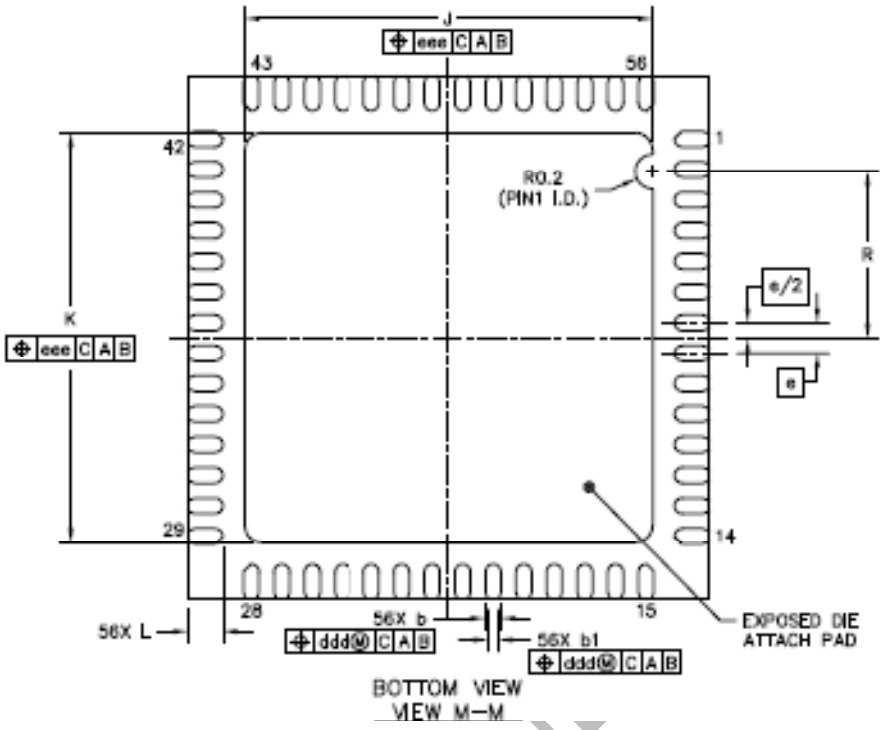


FT5446i Package Diagram

5 PACKAGE INFORMATION

5.1 Package Information of QFN-6x6-56L Package





Item		Symbol	Millimeter		
			Min	Type	Max
Total Thickness		A	0.5	0.55	0.6
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	----	0.4	----
L/F Thickness		A3		0.152 REF	
Lead Width		b	0.13	0.18	0.23
		b1	0.07	0.12	0.17
Body Size	X	D		6 BSC	
	Y	E		6 BSC	
Lead Pitch		e		0.35 BSC	
EP Size	X	J	3.9	4	4.1
	Y	K	3.9	4	4.1
Lead Length		L	0.35	0.4	0.45
		R	1.45	1.55	1.65
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Co Planarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	

Appendix: IC Revision history of FT5X46i Specification

Version	Change Items	Effective Date
0.1	1st Preliminary	27-Jun-14
0.2	Updated Y Drive	1-Aug-14
0.3	Updated Table 3-2 DC Characteristics	18-Aug-14
1.0	1.Removed Hibernation 2.updated Tpon<=200ms 3.updated Trsi<=200ms 4.updated I2C Timing Characteristics	23-Sept-14
1.1	1.Add FT5346i;	31-Jan-15
1.2	Update POWER ON/Reset Sequence	10-Sept-15
1.4	Update *package diagram and pin NO.*	1-Dec-15

END OF DATASHEET