DATA SHEET

(DOC No. HX8279-D01-DS)

HX8279-D01

1803 CH TFT LCD Source Driver with MIPI TCON

Version 04 May, 2019

Himax Technologies, Inc.
http://www.himax.com.tw

Revision History

May, 2019

Version	Date	Description of Changes
01	2016/12/19	New setup.
02	2017/10/26	Page 24 1. Modify application power circuit. Page 68, 70 2. Add the min. value of V/H porch. Page 111 3. Add current SPEC condition. 4. Add ULPS current SPEC.
03	2018/03/08	Page 68, 70 1. Correct min. value of H porch Page 83 2. Correct TCON configuration 2-truth tablet Page 111 3. Modify source output deviation SPEC
04	2019/05/17	Page 110 1. Modify VGH-VGL SPEC Page 115 2. Modify MIPI data-clock timing SPEC

List of Contents

List of Figures

1. General Description

HX8279-D01 is 1803 channel outputs source driver with MIPI TCON. The TCON generates the horizontal and vertical control timing to source driver and gate driver.

The source driver is for high-end displays. It is most suitable for 1200RGBx1920, 1080RGBx1920, 1200RGBx1600, and 600RGBx1024 and full 8bit output which are more superior in color depth. Since the output circuit of this source driver incorporates an operational amplifier with low power dissipation, and performs wide voltage supply range and small output deviation. Therefore, a high quality display with less crosstalk can be achieved.

2. Features

- MIPI interface support 2/4 lanes
- Support Multi-Drop and R/L type MIPI interface
- Two chip cascade solution for high resolution TFT LCD driver
- 1803 channel output, build in source driver and TCON
  - Channel number 1803 is for zigzag panel(M+1 and M+3) only
- Resolution:
  - Two chip solution for 1200RGBx1920, 1080RGBx1920, and 1200RGBx1600
  - One chip solution for 600RGB x 1024
- Support gamma curve adjustment by analog gamma and the RGB separated positive/negative digital gamma **(It can set thru MIPI command)**
- 256 gray scale driving output compliant to 8bit display data
- Driving scheme support 1/2/1+2/4 dot, and column inversion
- Support CABC function
- Support Color enhancement function
- Support external gate driver controlled signals and GOA function
- Support BIST mode
- Support stripe and zigzag panel
- Support VGH & VGL external charge pump controlled signals
- Support 8 times OTP for VCOM and 1 time OTP for gamma programming
- Only request three powers(VDD,VSP,VSN) from HOST
- Digital power range VDD:1.7V~2.0V
- Analog power range VSP:4.5V~6.0V VSN:-4.5V~-6.0V
- Output bump pitch is 12μm
- COG package

3. Block Diagram

3.1 Function block diagram

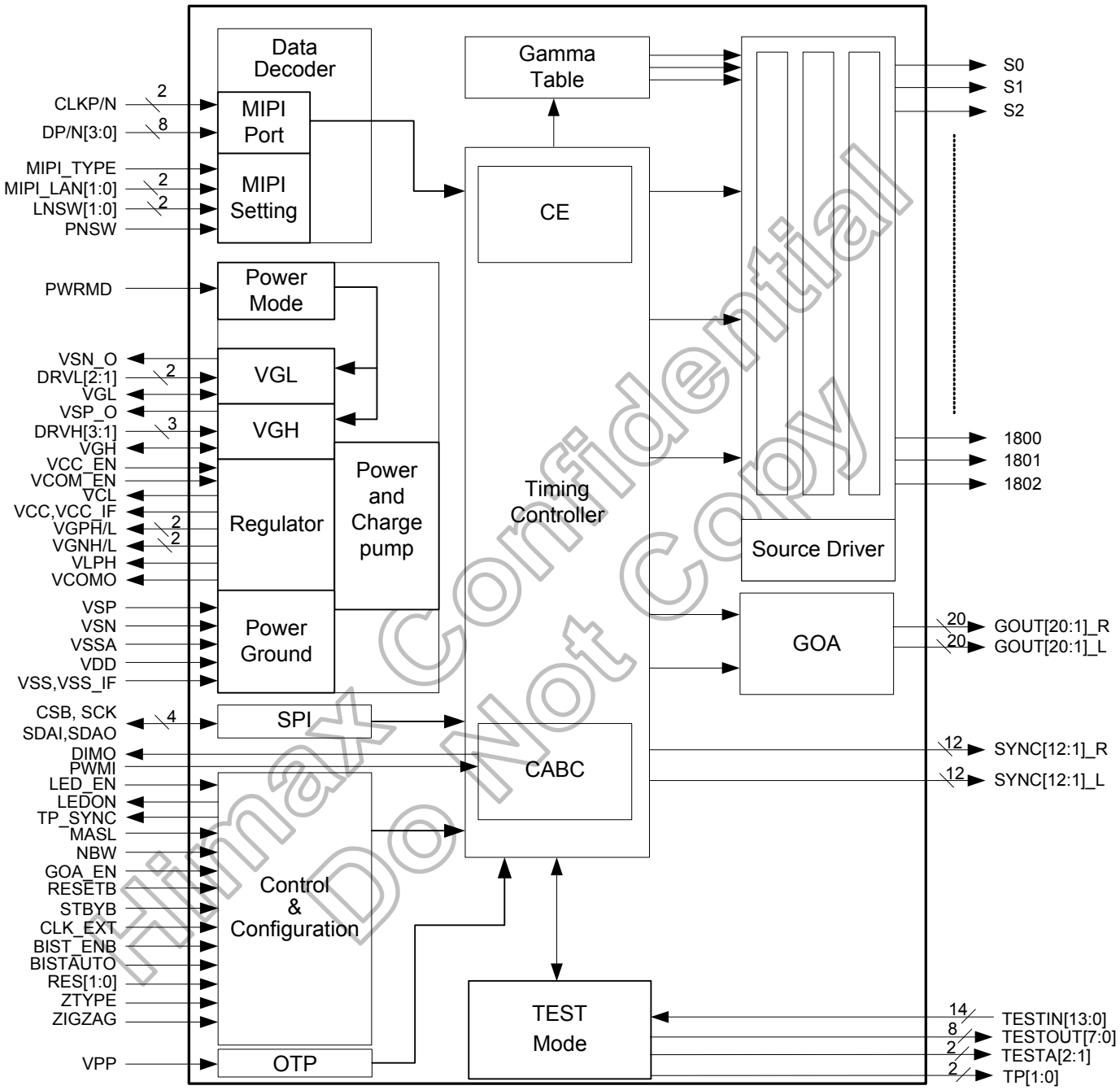


Figure 3.1: System function block diagram

4. Pin Description

4.1 Pin description

4.1.1 Global pin

Pin name	I/O	I/O power	Description
RESETB	In	VDD	Global reset. **(Default pull high)**
STBYB	In	VDD	Standby mode selection.**(Default pull high)** STBYB=H,Normal mode. STBYB=L,Standby mode. (AND reg page0 0xB2[6])
ZIGZAG	In	VCC	Enable zigzag driver method. **(Default pull high)** ZIGZAG=H, Panel type is zigzag. ZIGZAG=L, Panel type is stripe. (XOR reg page0 0xB2[3])
ZTYPE	In	VCC	Zigzag panel type selection. **(Default pull high)** ZTYPE=L, Zigzag panel type is TYPE0. ZTYPE=H, Zigzag panel type is TYPE1. (XOR reg page0 0xB2[2])
PWRMD	In	VCC	Power mode selection. **(Default pull high)** HX8279-D01 can use charge pump to generate VGH, and VGL These function is enabled by PWRMD. PWRMD=H,Use external VGH/VGL PWRMD=L,Use internal VGH/VGL (XOR reg page0 0xB3[4])
MASL	In	VCC	Define chip is master or slave.**(Default pull high)** MASL=H, Chip is master. MASL=L, Chip is slave.
RES0 RES1	In	VCC	Resolution display selection. **(Default RES[1:0]=11b)** 600RGBx1024 is for one chip application only. **(X means no disable channel)** **RES1 / RES0 / Resolution / Disable channel** 0 / 0 / 1200RGBx1600 / X 0 / 1 / 1080RGBx1920 / 811~990 1 / 0 / 600RGBx1024 / X 1 / 1 / 1200RGBx1920 / X (XOR reg page0 0xB3[1:0])
MIPI_TYPE	In	VCC	MIPI type selection.**(Default pull low)** MIPI_TYPE=H, R/L type. MIPI_TYPE=L, Multi-drop type. (XOR reg page0 0xB8[4])
LNSW1 LNSW0	In	VCC	MIPI data lane swap. **(Default LNSW[1:0]=11b)** Please refer chapter 4.4. (XOR reg page0 0xB8[3:2])
MIPI_LAN0 MIPI_LAN1	In	VCC	MIPI lane number configuration.**(Default MIPI_LAN[1:0]=11b)** **MIPI_LAN1 / MIPI_LAN0 / MIPI Lane number** 0 / 0 / Reserve 0 / 1 / 2 Lanes 1 / 0 / Reserve 1 / 1 / 4 Lanes (XOR reg page0 0xB8[1:0])
PNSW	In	VCC	MIPI data lane P/N swap. **(Default pull low)** PNSW=H,P/N swap PNSW=L,P/N normal (XOR reg page0 0xB8[5])
GOA_EN	In	VCC	GOA function enable. **(Default pull high)** GOA_EN=H, GOA function is enable. GOA_EN=L, GOA function is disable. (XOR reg page0 0xB8[7])

Pin name	I/O	I/O power	Description
NBW	In	VCC	Normal display selection. **(Default pull high)** NBW=H, Normal black panel type. NBW=L, Normal white panel type. (XOR reg page0 0xB2[1])
CLK_EXT	In	VCC	External CLK input for TCON. This pin is for Test only. Float it if not used. **(Default pull high)**
CSB	In	VDD	SPI chip select. Suggest reserving test pad for debug. **(Default pull high)**
SCK	In	VDD	SPI clock input. Suggest reserving test pad for debug. **(Default pull high)**
SDAI	In	VDD	SPI data input. Suggest reserving test pad for debug. **(Default pull high)**
SDAO	Out	VDD	SPI data output. Suggest reserving test pad for debug. Float it if not used.
BIST_ENB	In	VCC	BIST pattern selection. **(Default pull high)** BIST_ENB=H, Self test mode is disable. BIST_ENB=L, Self test mode is enable. (XOR reg page0 0xB2[0])
BISTAUTO	In	VCC	BIST display automatically change pattern. **(Default pull high)** BISTAUTO=H, Automatically change pattern BISTAUTO=L,Fix pattern
LED_EN	In	VCC	LEDON output control. **(Default pull high)** LED_EN=H, LEDON output enable LED_EN=L, LEDON output disable (XOR reg page0 0xB3[2])
LEDON	Out	VDD	LED driver enable/ disable control signal. Float it if not used. Control by pin LED_EN XOR reg page0 0xB3[2] and power on/off sequence
DIMO	Out	VDD	PWM control signal for brightness of the LED backlight. This pin is connected to the external LED driver. Float it if not used.
PWMI	In	VDD	PWM signal input for DIMO. Control by page4 0xB7[2]. **(Default pull high)**
TP_SYNC	Out	VDD	Sync signal for touch panel. Float it if not used.
VCC_EN	In	VDD	VCC regulator output selection. **(Default pull high)** VCC_EN=H.VCC output regulator is enable. VCC_EN=L.VCC output regulator is disable.
VCOM_EN	In	VCC	VCOM OP enable. **(Default pull high)** VCOM_EN=H, VCOM OP enable,ouput VCOM VCOM_EN=L, VCOM OP disable,outut floating
RP1EN	In	VCC	1st repair OP on/off control. **(Default pull high)** RP1EN=H,Rrepair OP enable RP1EN=L, Repair OP disable (XOR reg page0 0xB6[6])
RP2EN	In	VCC	2nd repair OP on/off control. **(Default pull high)** RP2EN=H, Repair OP enable RP2EN=L, Repair OP disable (XOR reg page0 0xB6[5])

4.1.2 Synchronize pin

Pin name	I/O	Description
SYNC1_R ~ SYNC12_R	In/Out	Synchronized signals between master and slave. These pins at right side of chip.
SYNC1_L ~ SYNC12_L	In/Out	Synchronized signals between master and slave. These pins at left side of chip.

4.1.3 MIPI interface

Pin name	I/O	Description
CLKP/CLKN	In	MIPI clock input pin.
DP0/DN0 DP1/DN1 DP2/DN2 DP3/DN3	In	MIPI data input pin.

Note: (1) IO cell voltage is VCC_IF.

4.1.4 Gate driver (GOA) control pin

Pin name	I/O	Description
GOUT1_R ~ GOUT20_R	Out	GOA control signal at right side.
GOUT1_L ~ GOUT20_L	Out	GOA control signal at left side.

Note: (1) IO cell voltage is between VGH and VGL.

4.1.5 Source output pin

Pin name	I/O	Description
S0	Out	Source output pin. It is available when zigzag function enable.
S1~S1800	Out	Source output pin.
S1801,S1802	Out	Source output pin. It is available when zigzag function enable.

Note: (1) IO cell voltage is between VSP and VSN.

4.1.6 Charge pump and regulator pin

Pin name	I/O	Description
VCC	Out	Regulator voltage for digital circuit. **(1.55V)**
VCC_IF	Out	Regulator voltage for MIPI interface circuit. **(1.55V)**
VGPH	Out	Regulator high voltage for positive gamma. **(4V ~ 5.5V)**
VGPL	Out	Regulator low voltage for positive gamma. **(0.1V ~ 1.6V)**
VGNH	Out	Regulator high voltage for negative gamma. **(-4V ~ -5.5V)**
VGNL	Out	Regulator low voltage for negative gamma. **(-0.1V ~ -1.6V)**
VLPH	Out	Regulator output for MIPI LP mode. **(1.2V)**
VCOMO	Out	VCOM op output. **(-0.2V ~ -2.75V)**
VCL	Out	Regulator output voltage for source level shift. **(-2.4V)**
DRVH3 DRVH2 DRVH1	Out	VGH charge pump control signals. Float it if not used.
DRVL2 DRVL1	Out	VGL charge pump control signals. Float it if not used.
VSP_O	Out	VGH charge pump control signals. Float it if not used.
VSN_O	Out	VGL charge pump control signals. Float it if not used.
RP1O	Out	1st repair OP output. Float it if not used.
RP2O	Out	2nd repair OP output. Float it if not used.
RP1I	In	1st repair OP input. Float it if not used.
RP2I	In	2nd repair OP input. Float it if not used.

Note: (1) IO cell voltage is based on supply capability.

4.1.7 Power and ground pin

Pin name	I/O	Description
VDD	Power	Power supply for digital power regulator. **(1.7V~2.0V)**
VSN	Power	Power supply for analog circuit. **(-4.5V ~ -6V)**
VSP	Power	Power supply for analog circuit. **(4.5V ~ 6V)**
VGL	Power	Power supply for GOA and gate drive. It provides from internal or external power. This supply voltage must be connected to the chip, even GOA function doesn't use. **(-6.7V ~ -16.0V)**
VGL1_L/R	Power	Power supply for Gait provides different voltage level for GOUT_R7/GOUT_R8/GOUT_L7/GOUT_L8 output. If don't use, connect the pins to VGL. **(-6.7V ~ -16.0V)**
VGH	Power	Power supply for GOA and gate drive. It provides from internal or external power. This supply voltage must be connected to the chip, even GOA function doesn't use. **(8.7V ~ 18.0V)**
VPP	Power	Power supply for OTP. Reserve 0.1 CAP. connected to GND for using internal VPP.Float it for normal operation. **(8.5V)**
VSS	GND	Ground for digital circuit. **(0V)**
VSS_IF	GND	Ground for MIPI interface. **(0V)**
VSSA	GND	Ground for analog circuit. **(0V)**

4.1.8 Others

Pin name	I/O	Description
TESTOUT0 ~ TESTOUT7	Out	Test pin. Float these pin for normal operation.
TESTIN0 ~ TESTIN13	In	Test pin. Float these pin for normal operation.
TESTA1 TESTA2	Out	Test pin. Float these pin for normal operation.
TP0,TP1	In	Test pin. Float these pin for normal operation.
COMR1 COMR2	-	VCOM through pin.
COML1 COML2	-	VCOM through pin.
COM3~5	-	Bonding impedance measure pin.
SHIELDING	-	Chip shielding pads. It is floating internal.

4.2 Value of wiring resistance to each pin

The input wiring resistance values affect power or signal integrity and the display quality. So be sure to design using values that do not exceed those recommendations as below.

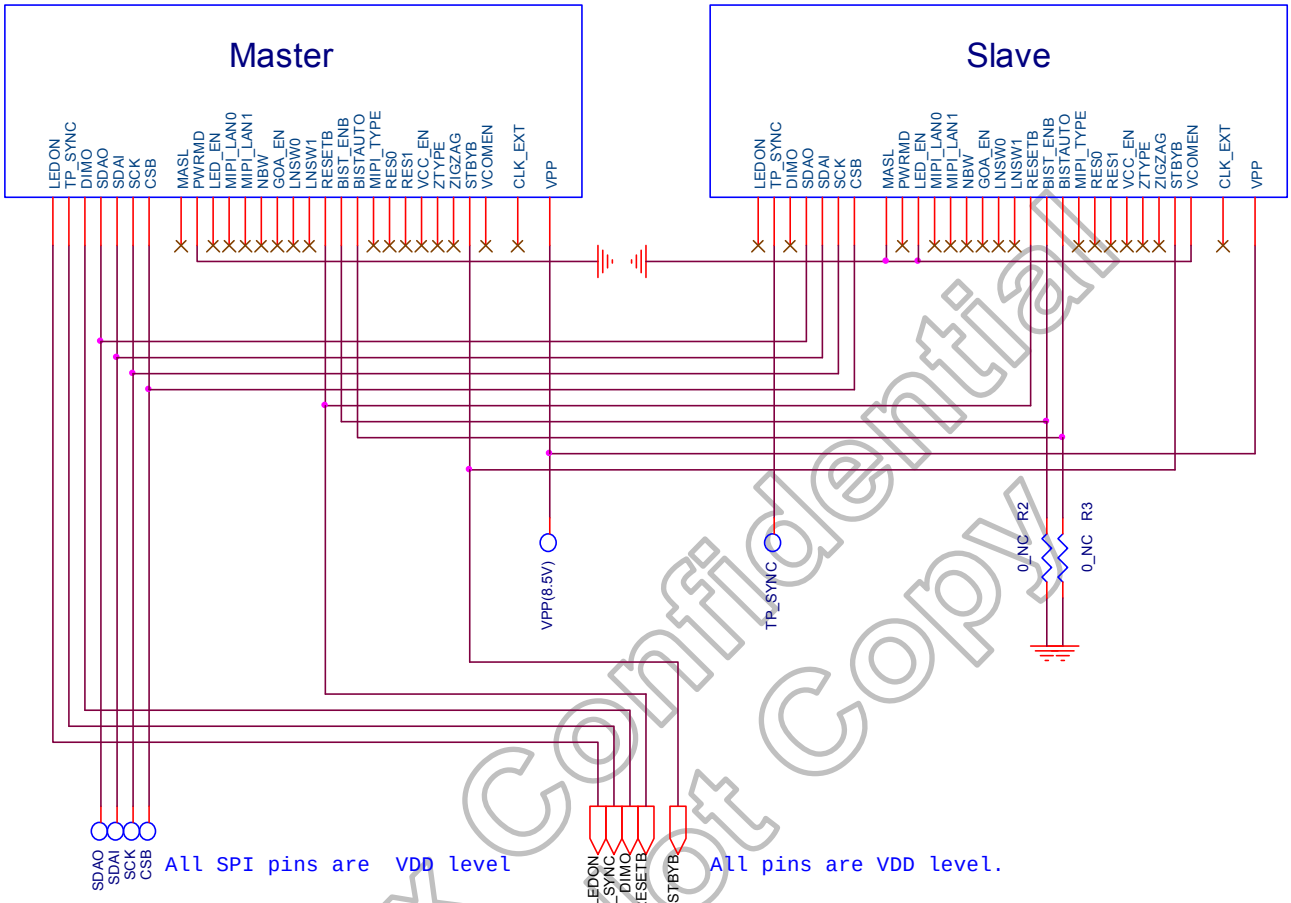
Pin Type	Pin Name	Resistance value(Ω)	Capacitance value(pF)
Power & Ground	VDD	< 3	-
	VSP, VSN	< 3	-
	VSS	< 3	-
	VSS_IF	< 5	-
	VCC_IF	< 5	-
	VCC	< 3	-
	VSSA	< 3	-
Charge Pump & Regulator	VLPH	< 5	-
	VGL/VGL1	< 5	-
	VGH	< 5	-
	VCOMO	< 10	-
	VGPH	< 10	-
	VGPL	< 10	-
	VGNH	< 10	-
	VGNL	< 10	-
	VCL	< 5	-
	DRVH1,DRVH2,DRVH3	< 5	-
	VSP_O, VSN_O	< 3	-
	DRVL1,DRVL2,DRVL3	< 5	-
GOA	GOUT1_R~GOUT20_R	<100	-
	GOUT1_L~GOUT20_L	<100	-
MIPI Interface	CKP, CLKN	< 10	< 0.9
	DP0, DN0	< 10	< 0.9
	DP1, DN1	< 10	< 0.9
	DP2, DN2	< 10	< 0.9
	DP3, DN3	< 10	< 0.9
Synchronized signals	SYNC1_L	RC < 40ns	RC < 40ns
	SYNC2_L	RC < 40ns	RC < 40ns
	SYNC3_L	RC < 40ns	RC < 40ns
	SYNC4_L	RC < 40ns	RC < 40ns
	SYNC5_L	RC < 40ns	RC < 40ns
	SYNC6_L	RC < 40ns	RC < 40ns
	SYNC7_L	RC < 40ns	RC < 40ns
	SYNC8_L	RC < 40ns	RC < 40ns
	SYNC9_L	RC < 40ns	RC < 40ns
	SYNC10_L	RC < 40ns	RC < 40ns
	SYNC11_L	RC < 40ns	RC < 40ns
	SYNC12_L	RC < 40ns	RC < 40ns
	SYNC1_R	RC < 40ns	RC < 40ns
	SYNC2_R	RC < 40ns	RC < 40ns
	SYNC3_R	RC < 40ns	RC < 40ns
	SYNC4_R	RC < 40ns	RC < 40ns
	SYNC5_R	RC < 40ns	RC < 40ns
	SYNC6_R	RC < 40ns	RC < 40ns
	SYNC7_R	RC < 40ns	RC < 40ns
	SYNC8_R	RC < 40ns	RC < 40ns
	SYNC9_R	RC < 40ns	RC < 40ns
	SYNC10_R	RC < 40ns	RC < 40ns
	SYNC11_R	RC < 40ns	RC < 40ns
	SYNC12_R	RC < 40ns	RC < 40ns

Pin Type	Pin Name	Resistance value(Ω)	Capacitance value(pF)
Control & Hardware Configuration	ZIGZAG	< 200	-
	ZTYPE	< 200	-
	PWRMD	< 200	-
	RES0, RES1	< 200	-
	MIPI_TYPE	< 200	-
	BISTAUTO	< 200	-
	BIST_ENB	< 200	-
	CLK_EXT	< 100	-
	RESETB	< 100	-
	LNSW0, LNSW1	< 200	-
	GOA_EN	< 200	-
	NBW	< 200	-
	MIPI_LAN0, MIPI_LAN1	< 200	-
	MASL	< 200	-
	RP1EN	< 200	-
	RP2EN	< 200	-
	VCC_EN	< 200	-
	VCOM_EN	< 200	-
	LED_EN	< 200	-
	LEDON	< 200	-
	DIMO	< 200	< 20
	PWMI	< 200	< 20
	CSB	< 200	-
	SCK	< 200	-
	SDAI	< 200	-
	SDAO	< 200	< 20

Table 4.1: Wiring resistance values

4.3 Hardware pin configuration for FPC/PCB

Here is shows hardware pin configuration of Master and Slave.



Note: (1) PWRMD is low. The system only needs to supply three powers VDD, VSP and VSN.
(2) The settings apply to 1200RGBx1920 GOA zigzag type0 panel and use 4 lanes multi-drop mipi input.
(3) Use internal VCOM.

Figure 4.1: Hardware pin configuration example

4.4 MIPI interface pin mapping table

This table shows the mapping with pad name and MIPI lanes. It could configure by hardware pin LNSW0 and LNSW1.

- LNSW0 and LNSW1 are for swap MIPI data pair.

Pad Name / Configuration		DP3	DN3	DP2	DN2	CLKP	CLKN	DP1	DN1	DP0	DN0
LNSW0	LNSW1	MIPI lanes mapping table									
0	0	DP0	DN0	DP3	DN3	CLKP	CLKN	DP2	DN2	DP1	DN1
1	0	DP2	DN2	DP3	DN3	CLKP	CLKN	DP0	DN0	DP1	DN1
0	1	DP3	DN3	DP0	DN0	CLKP	CLKN	DP1	DN1	DP2	DN2
1	1	DP3	DN3	DP2	DN2	CLKP	CLKN	DP1	DN1	DP0	DN0

Note: (1) Mark is default.

Table 4.2: MIPI interface mapping table

4.5 MIPI interface type selection

There are two types of MIPI interface in this chip – Multi-Drop and RL.

Multi-drop type consist of two chips and works through same MIPI bus. The buses have the advantage of simplicity, but bad latency is between two chips.

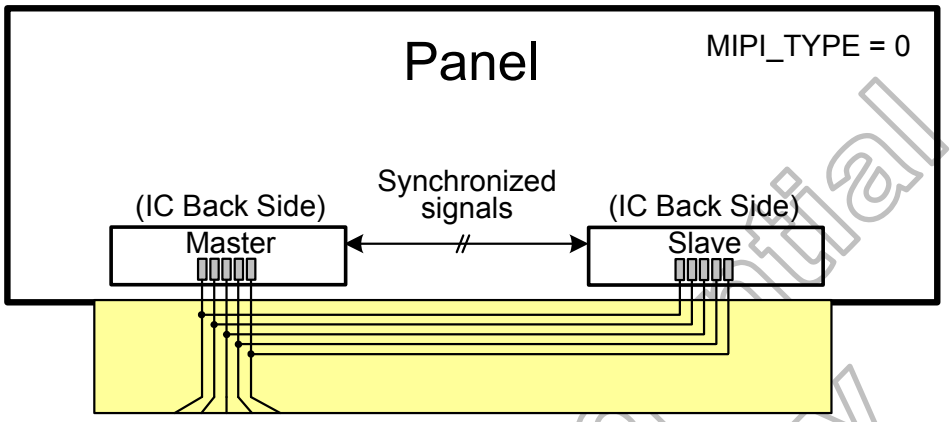


Figure 4.2: MIPI multi drop type interface

RL type is a point-to-point interconnect between the application processor and HX8279-D01. The buses have the advantage of high band width and low latency.

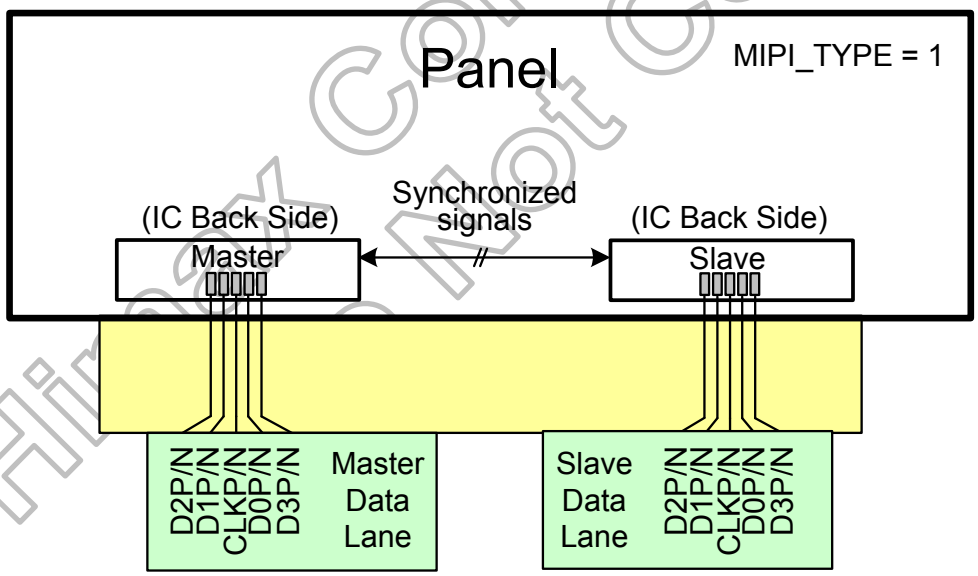


Figure 4.3: MIPI RL type interface

4.6 Application block diagram

Here is shows application for HX8279-D01.If use external VGH/VGL, VGH/VGL must connect to HX8279-D01 in all application.

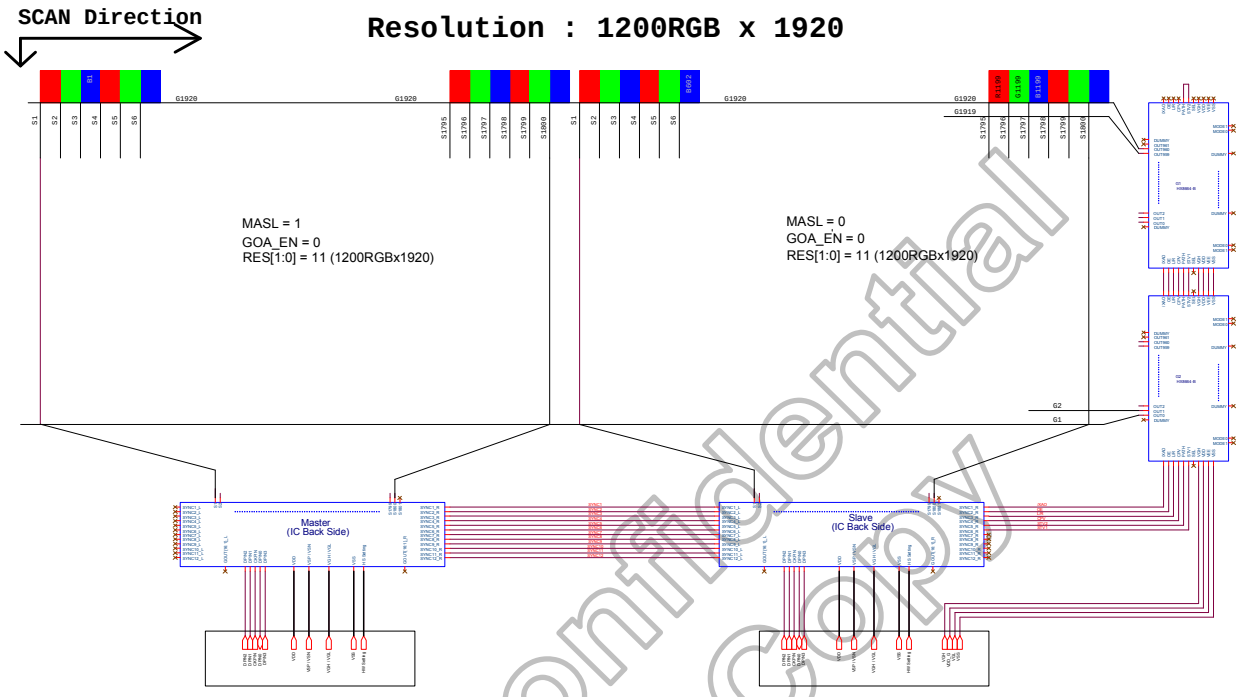


Figure 4.4: Application for 1200RGBx1920 with external GD

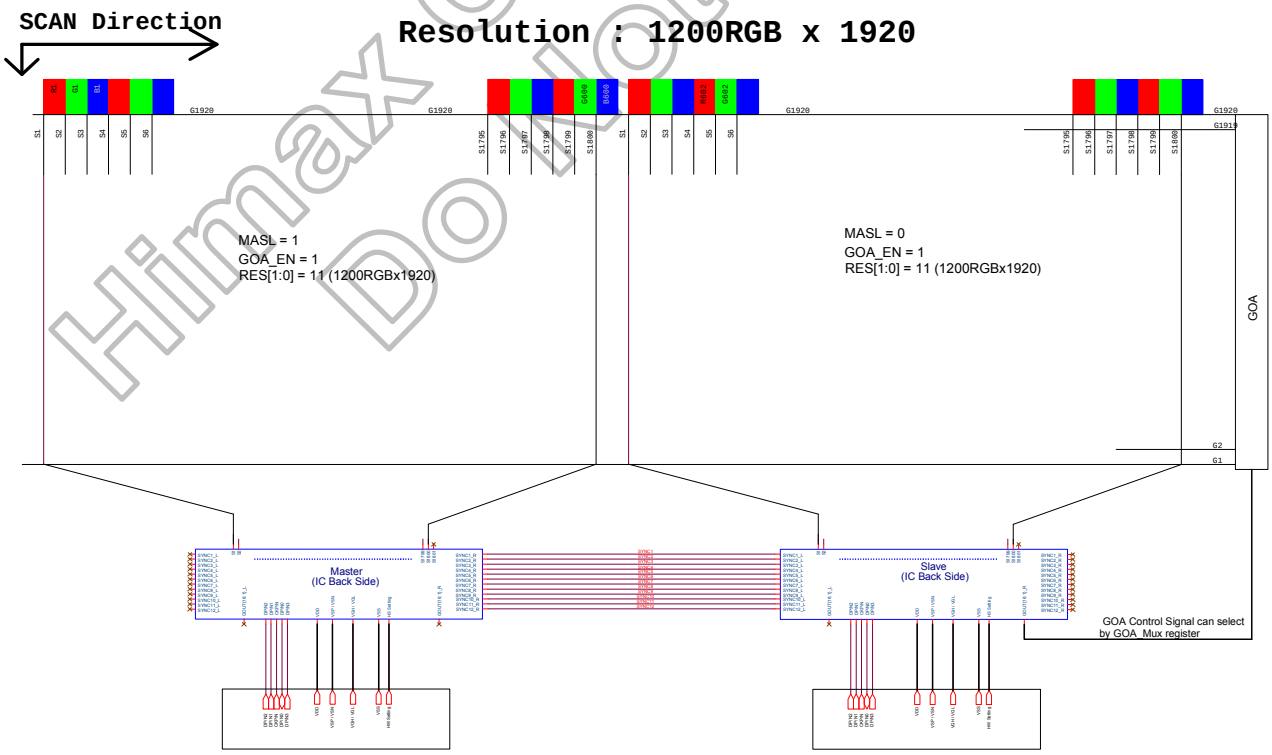


Figure 4.5: Application for 1200RGBx1920 with single side of GOA

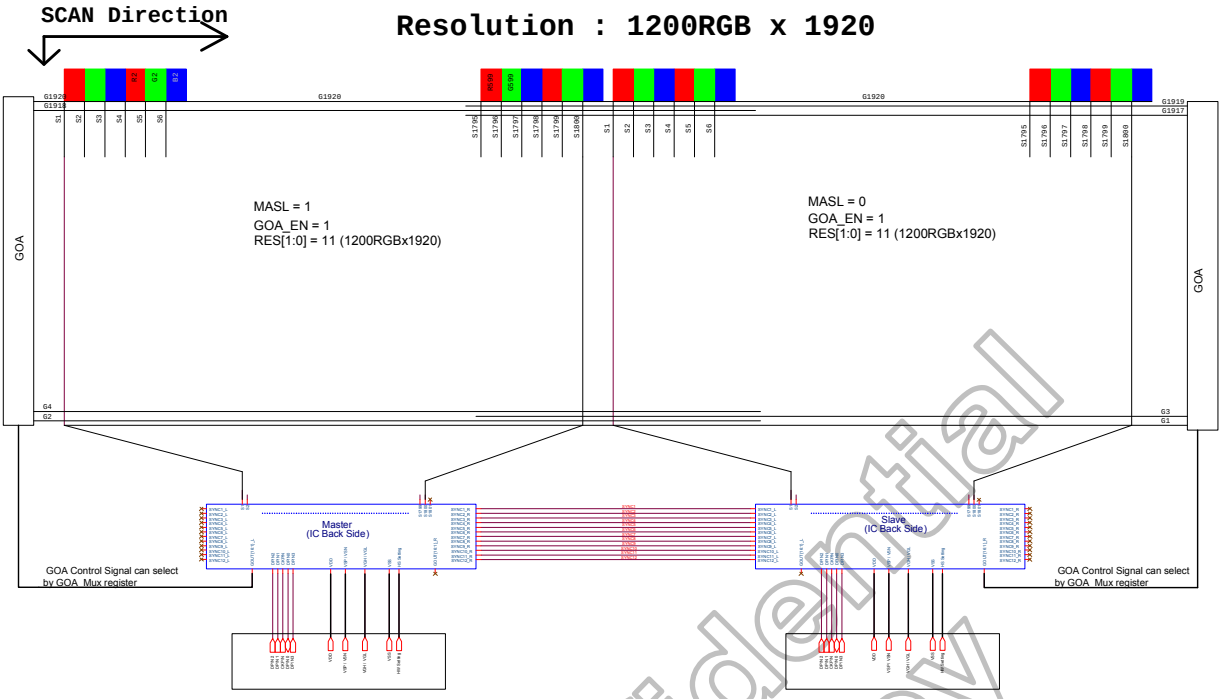


Figure 4.6: Application for 1200RGBx1920 with two side of GOA

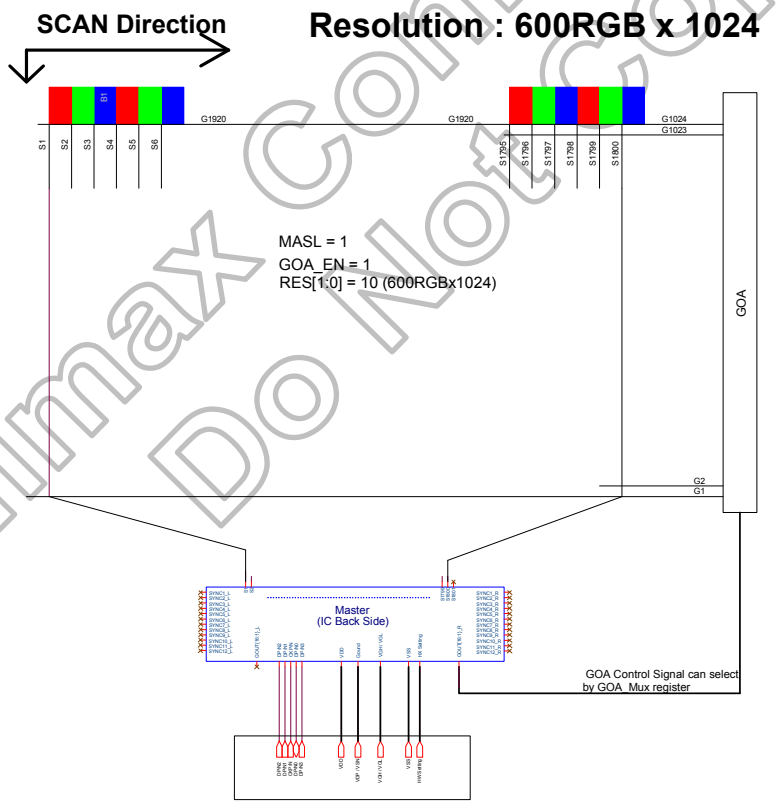


Figure 4.7: Application for 600RGBx1024 with single side of GOA

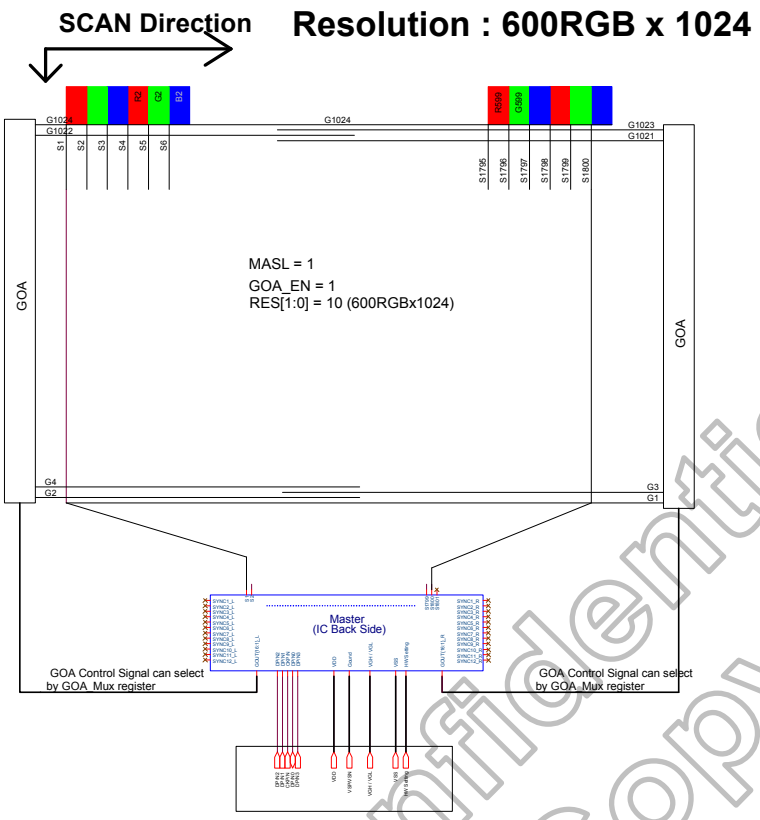


Figure 4.8: Application for 600RGBx1024 with two side of GOA

5. Power Application

5.1 Application power circuit

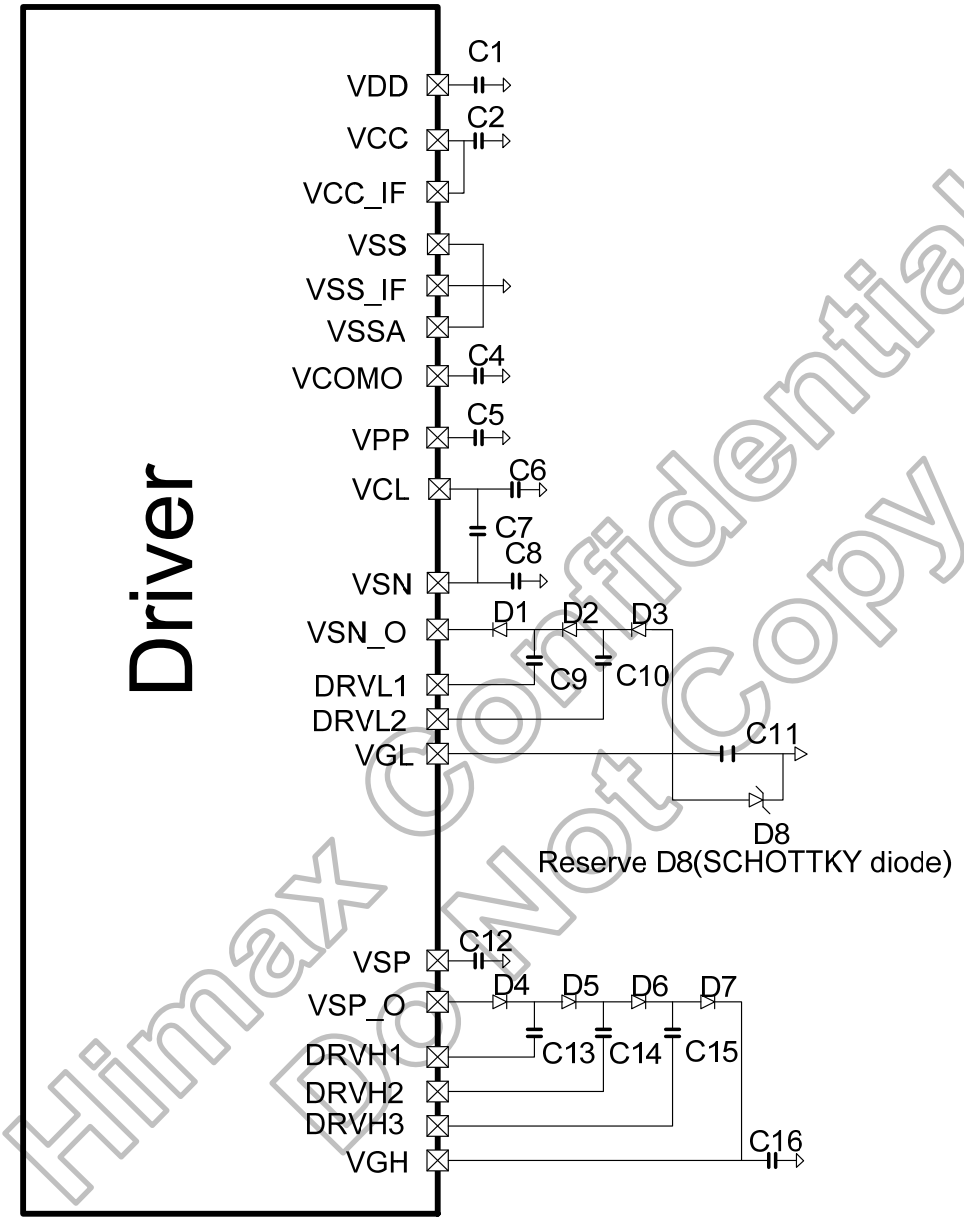


Figure 5.1: Power function typical application

5.2 Power generation diagram

5.2.1 Power generation diagram

The HX8279-D01 incorporates external charge pump control signals for VGH/VGL.

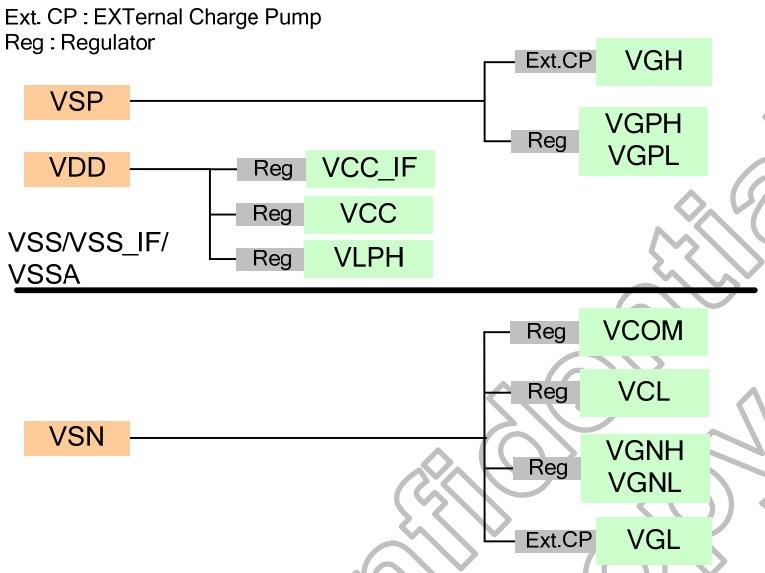


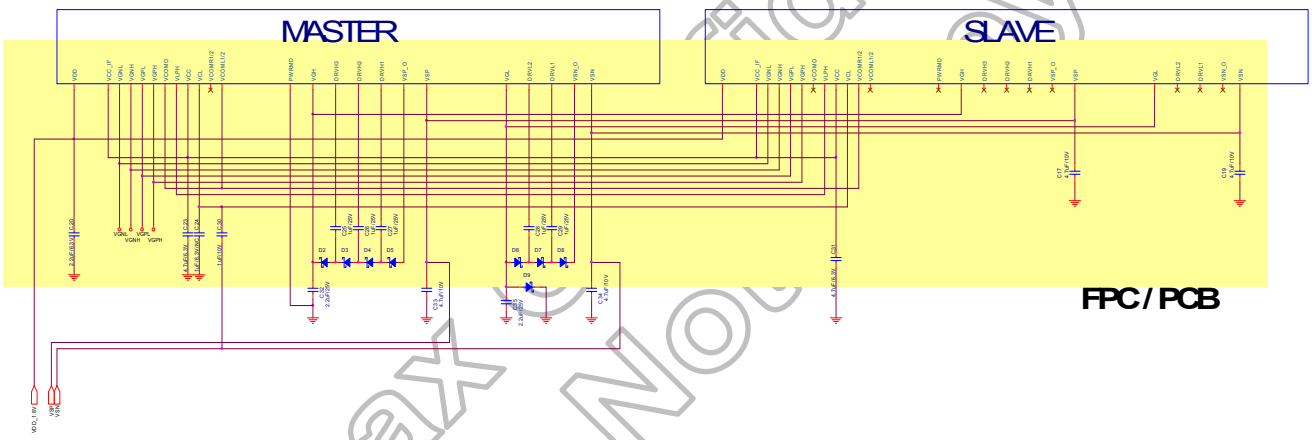
Figure 5.2: Power architecture

5.3 Power circuit structure

5.3.1 Internal VGH/VGL

This case is used external VSP/VSN to generate VGH/VGL.

- Main voltages from external power IC, then supply to master and slave
  - VDD
- External voltage supply to master and slave
  - VSP and VSN
- Voltages are generated by external charge pump of master, then supply to slave
  - VGL and VGH
- Voltages are generated by regulator of master, then supply to slave.
  - VCL,VCOM, VGPH, VGPL, VGNH, and VGNL
- Voltages are generated by regulator of Master and Slave, then to connect wire together each other
  - VCC, VCC_IF, and VLPH



HW Set	Master	Slave
PWRMD	L	X
VCC_EN	H	H

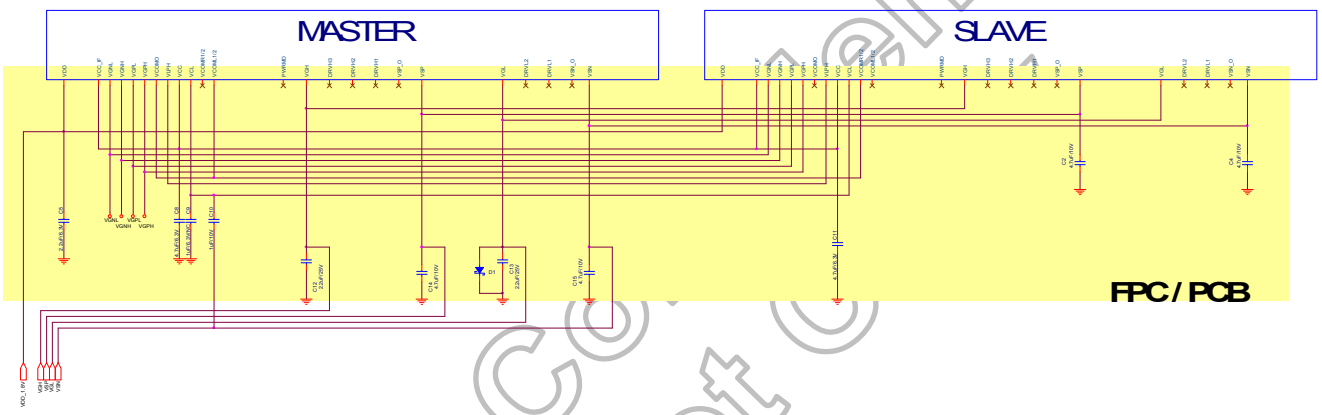
Note: (1) Slave IC only enables regulator for VCC, VCC_IF, and VLPH. Others power functions are all disable when cascade mode is used.
(2) Reserve D9 to prevent latch up issue.
(3) "X" means don't care. It can set to high, low or floating.

Figure 5.3: External VSP/VSN and internal VGH/VGL power structure

5.3.2 External VGH/VGL

This case is used all external power supply voltage

- Main voltages from external power IC, then supply to Master and Slave.
  - VDD
- External voltage supply to Master and Slave.
  - VSP, VSN, VGH, and VGL
- Voltages are generated by regulator of Master, then supply to Slave.
  - VCL,VCOM, VGPH, VGPL, VGNH, and VGNL
- Voltages are generated by regulator of Master and Slave, then to connect wire together each other.
  - VCC, VCC_IF, and VLPH



HW Set	Master	Slave
PWRMD	H	H
VCC_EN	H	H

Note: (1) Slave IC only enables regulator for VCC, VCC_IF, and VLPH. Others power functions are all disable when cascade mode is used.

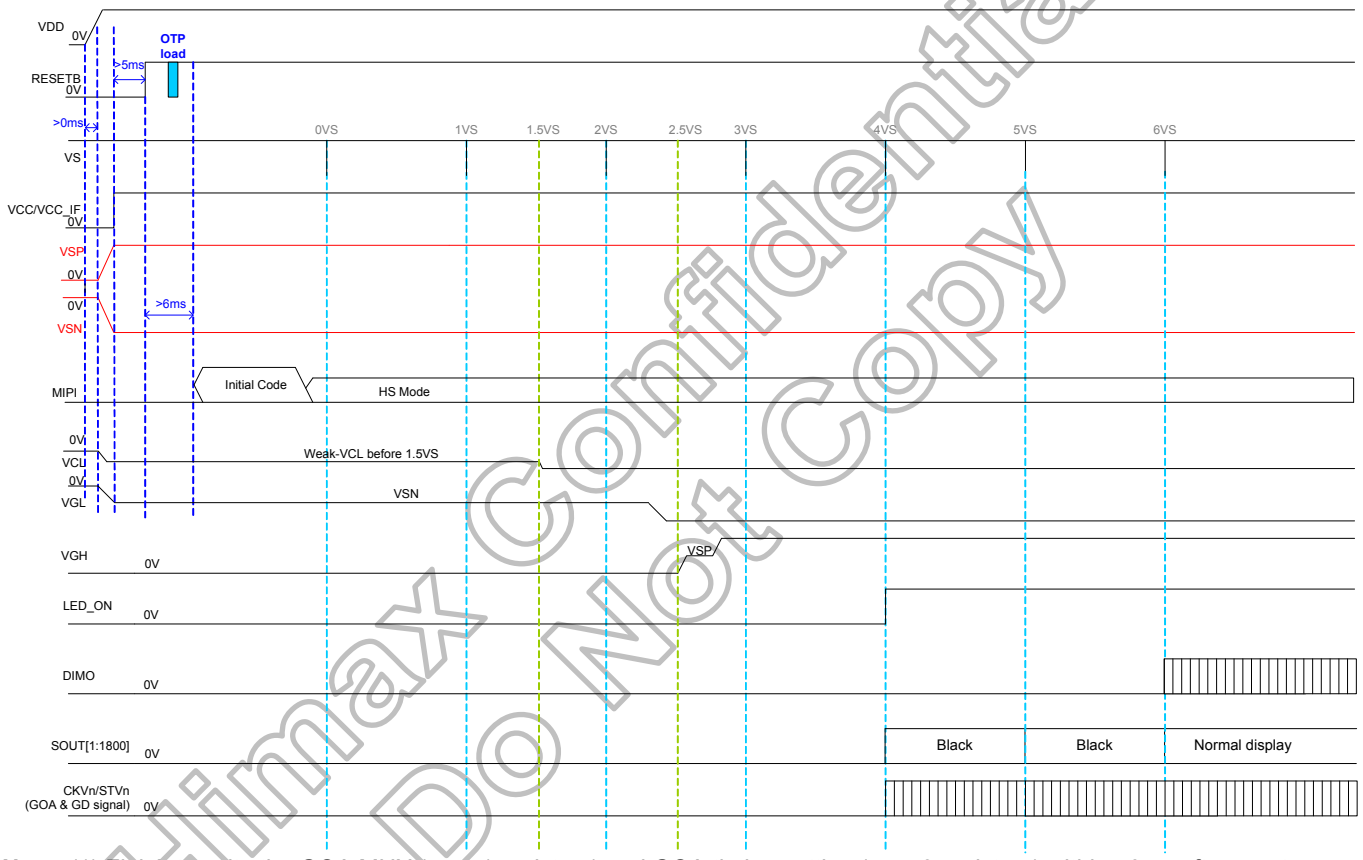
Figure 5.4: All power is from external power IC

5.4 Power on/off sequence

5.4.1 Power on sequence PWRMD=0 ➔ Max. Power on time=7.0VS

After reset state or exit STB mode, the power on sequence will start.

To prevent the device from damage due to latch up, The VGL will be earlier than VGH. At 2.25VS the VGL negative high voltage will be generated via the external charge pump circuit. Then at 2.5VS the VGH positive high voltage can be generated via the external charge pump circuit. One SCHOTTKY diode is necessary between VGL and GND when VDD and VSP start at the same time.



Note: (1) Finish to write the GOA MUX (page1 registers) and GOA timing setting (page3 registers) within 50ms after reset pulls to high.

Figure 5.5: Power on sequence with PWRMD=0 and repair OP disable

5.4.2 Power off sequence PWRMD=0 ➔ Max. Power off time=5.0VS

When enter STB mode, the STBYB signal will be set to low. The power off sequence will start.

Power-off sequence
External VSP/VSN. Internal VGH/VGL.

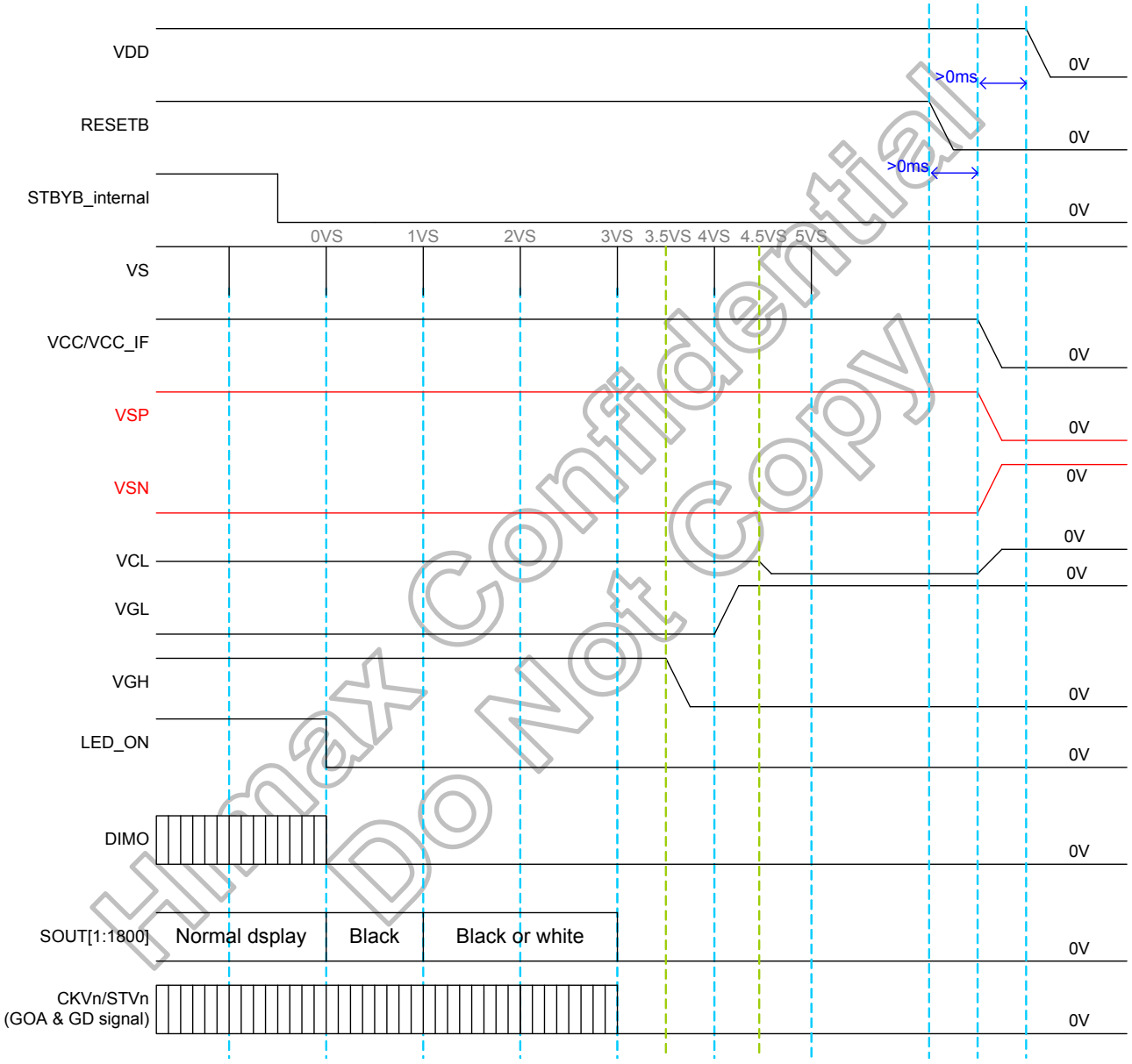
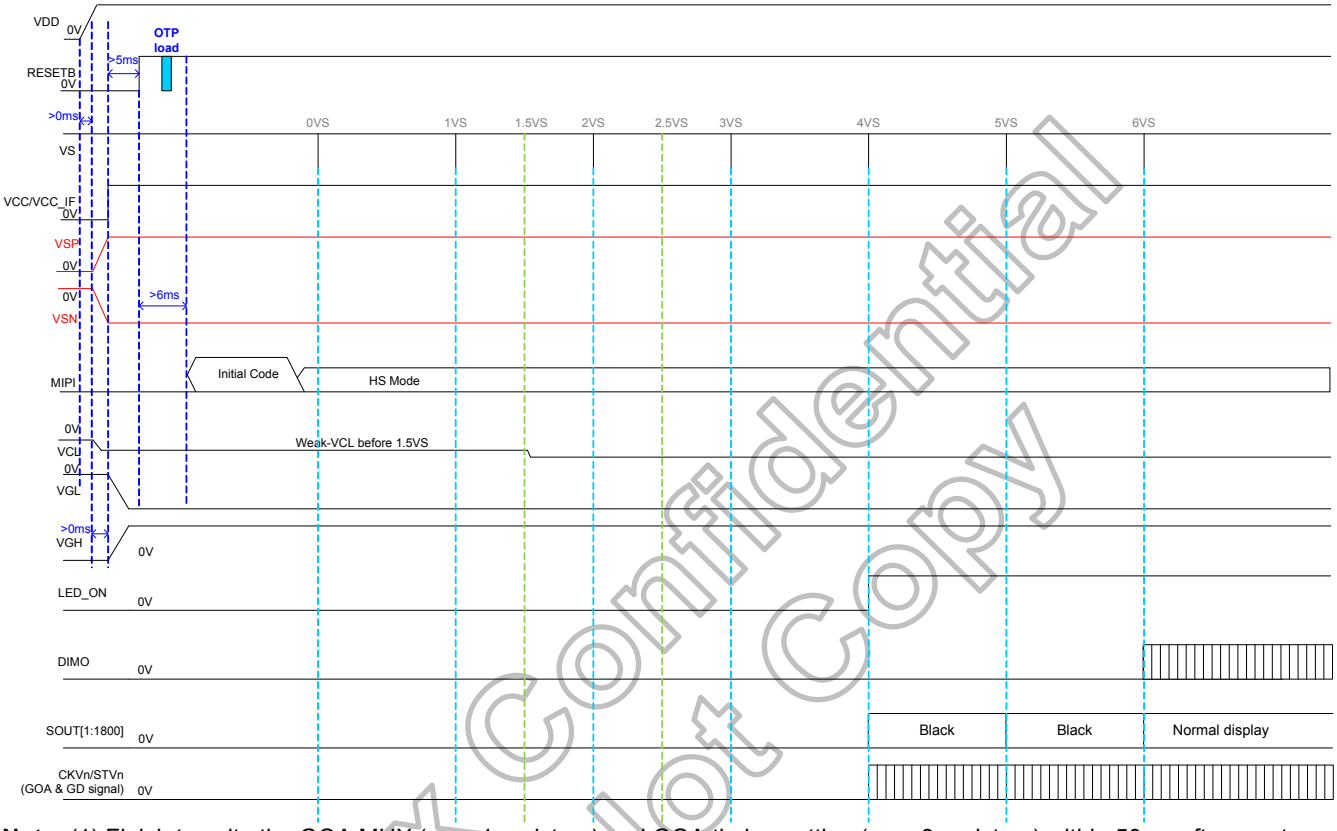


Figure 5.6: Power off sequence with PWRMD=0

5.4.3 Power on sequence PWRMD=1 ➔ Max. Power on time=6.0VS

After reset state or exit STB mode, the power on sequence will start. One SCHOTTKY diode is necessary between VGL and GND when VDD and VSP start at the same time.



Note: (1) Finish to write the GOA MUX (page1 registers) and GOA timing setting (page3 registers) within 50ms after reset pulls to high

Figure 5.7: Power on sequence with PWRMD=1 and repair OP disable

5.4.4 Power off sequence PWRMD=1 ➔ Max. Power off time=4.5VS

When enter STB mode, the STBYB signal will be set to low then the power off sequence will start.

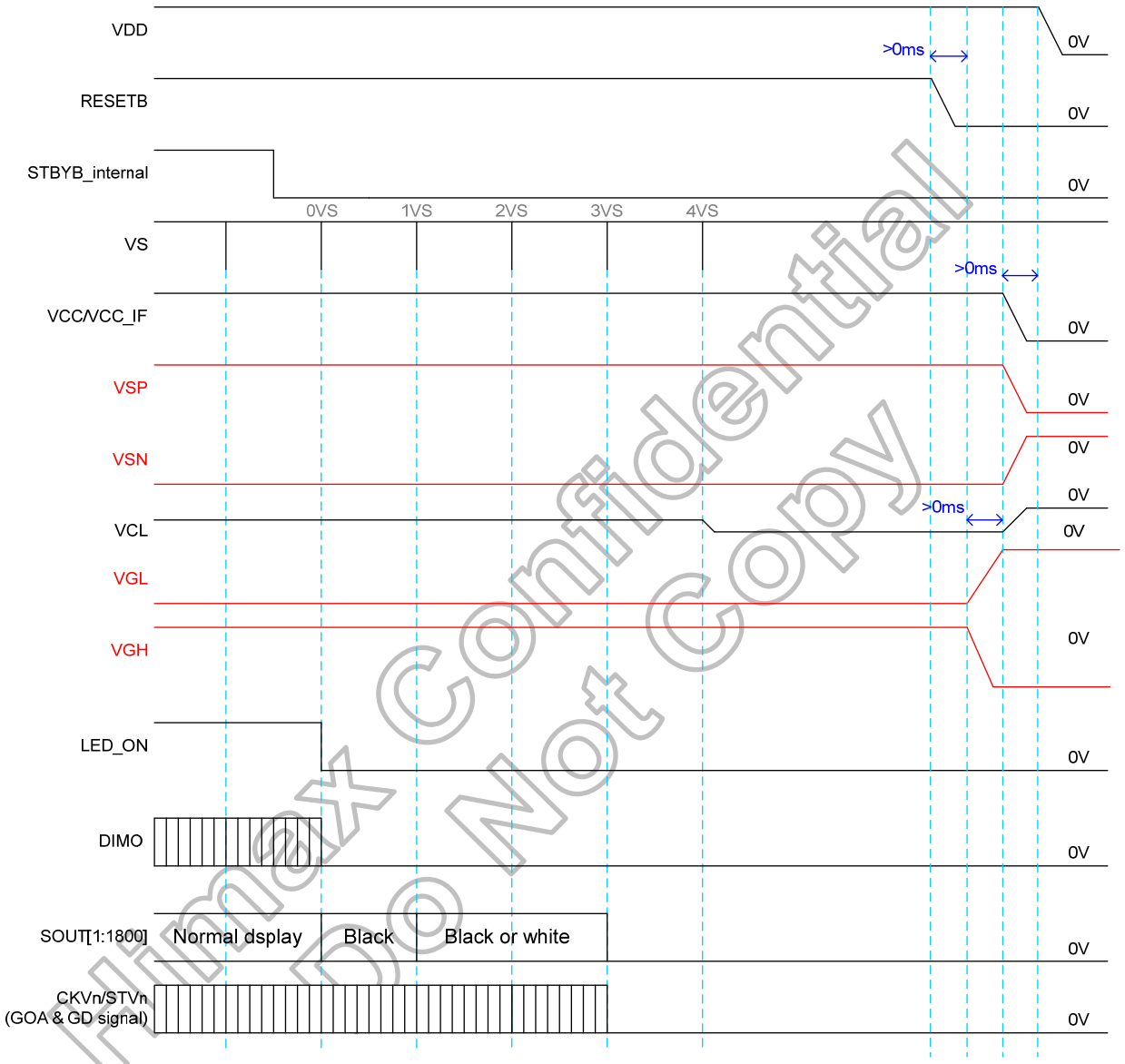


Figure 5.8: Power off sequence with PWRMD=1

6. Panel Application

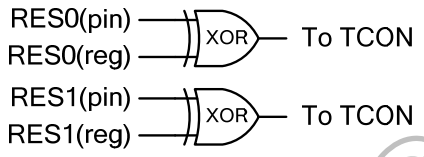
HX8279-D01 can support display resolution up to 1920 for vertical active line, and 1200RGB for horizontal active line. It also can support 2 type of driving method – Stripe and Zigzag. When horizontal display resolution is over 600RGB, the chip cascade mode must be used. A cascade connection can synchronize signals between 2 chips. We are called master and slave.

HX8279-D01 also can generate gate controller timing. These signals can support for general gate driver or GOA **(Gate driver on Array)**.

6.1 Display resolution

6.1.1 Display resolution configuration

Resolution selection can set by hardware or register. Hardware pin name is RES0 ~ RES1. Register address is locates 0xB3[1:0] at page0. The relationship between pin and register is shows below.

Combination Logic	Formula		
	RES0(1)(PIN)	RES0(1)(REG)	RES0(1)(TCON)
	0	0	0
	0	1	1
	1	0	1
	1	1	0

TCON RES[1:0]	Resolution
00	1200RGB x 1600 (default)
01	1080RGB x 1920
10	600RGB x 1024
11	1200RGB x 1920

Note: (1) 600RGBx1024 only for one chip application.

Table 6.1: Display resolution setting

6.1.2 Source output channel valid range

The channel of available output depends on the horizontal resolution, and non-available channel always locate at centre channel numbers. The source output pin must be floating if don't used.

Horizontal resolution	Master IC			Slave IC		
	Enable channel	Disable channel	Enable channel	Enable channel	Disable channel	Enable channel
1200 RGB	1 - 900	x	901 - 1800	1 - 900	x	901 - 1800
1080 RGB	1 - 810	811 - 990	991 - 1800	1 - 810	811 - 990	991 - 1800
600 RGB	1 - 900	x	901 - 1800	x		

Note: (1) 600RGB is only for one chip application.

Table 6.2: Source output enable/disable channel for stripe panel

Channel number 0, 1801 and 1802 is only for zigzag driving method.

Horizontal resolution	Master IC			Slave IC		
	Enable channel	Disable channel	Enable channel	Enable channel	Disable channel	Enable channel
1200 RGB	0 - 900	x	901 – 1800	0 - 900	x	901 – 1802
1080 RGB	0 - 810	811- 990	991 – 1800	0 - 810	811 - 990	991 – 1802
600 RGB	0 - 900	x	901 – 1802	x		

Note: (1) 600RGB is only for one chip application.

Table 6.3: Source output enable/disable channel for zigzag panel

6.2 Cascade connection

6.2.1 Cascade mode of synchronized signals

Synchronized signal is for synchronization with master and slave. Others function is gate control signal. The gate timing can be for external gate driver. This gate control signals isn't support dual gate timing.

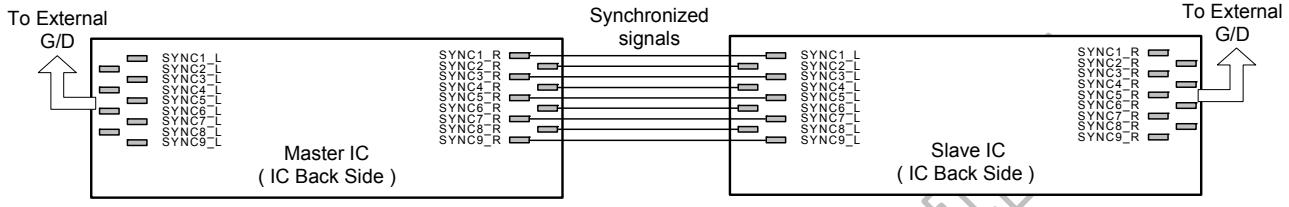


Figure 6.1: Cascade mode of synchronized signals

6.2.2 Synchronized signals of two chips cascade

Name	I/O	Description of master	I/O	Description of slave
SYNC1_R	O	POL sync signal to Slave.	O	/XAO: Gate output all on.
SYNC2_R	O	GAS sync signal to Slave.	O	OE: Output enables control.
SYNC3_R	O	NO_MIPI sync signal to Slave / BIST sync signal to Slave.	O	UD: Shift direction control signal.
SYNC4_R	I	CABC sync signal from Slave / DPHY scan in.	O	CPV to external GD.
SYNC5_R	O	CABC sync signal to Slave	O	UD=0, STV output control signal. UD=1, This pin is Hi-z.
SYNC6_R	O	CABC sync signal to Slave / DPHY scan out.	O	UD=1, STV output control signal. UD=0, This pin is Hi-z.
SYNC7_R	I	CABC sync signal from Slave	O	-
SYNC8_R	I/O	No MIPI signal between master and Slave.	O	-
SYNC9_R	O	Internal sync signal	O	Internal sync signal
SYNC10_R	O	Internal sync signal	O	Internal sync signal
SYNC11_R	O	Internal sync signal	O	Internal sync signal
SYNC12_R	O	Internal sync signal	O	Internal sync signal
Name	**I/O**	**Description of master**	**I/O**	**Description of slave**
SYNC1_L	O	/XAO: Gate output all on.	I	POL sync signal from Master.
SYNC2_L	O	OE: Output enables control.	I	GAS sync signal from Master.
SYNC3_L	O	UDB: Shift direction control signal. **(UDB always is inversion of UD)**	I	NO_MIPI sync signal from Master / BIST sync signal from Master.
SYNC4_L	O	CPV to external GD.	O	CABC sync signal to Master / DPHY scan out.
SYNC5_L	O	UDB=1, STV output control signal. UDB=0, This pin is Hi-z.	I	CABC sync signal from Master
SYNC6_L	O	UDB=0, STV output control signal. UDB=1, This pin is Hi-z.	I	CABC sync signal from Master / DPHY scan in.
SYNC7_L	O	-	O	CABC sync signal to Master
SYNC8_L	O	-	I/O	No MIPI signal between master and Slave.
SYNC9_L	O	Internal sync signal	O	Internal sync signal
SYNC10_L	O	Internal sync signal	O	Internal sync signal
SYNC11_L	O	Internal sync signal	O	Internal sync signal
SYNC12_L	O	Internal sync signal	O	Internal sync signal

Table 6.4: Synchronized signals decryption with two chip cascade

6.2.3 Synchronized signals of one chip application

The chip is used for one chip application. Both side of chip are synchronized signals.

Name	I/O	Description of SYNC_R	I/O	Description of SYNC_L
SYNC1	O	/XAO: Gate output all on.	O	/XAO: Gate output all on.
SYNC2	O	OE: Output enables control.	O	OE: Output enables control.
SYNC3	O	UD: Shift direction control signal.	O	UDB: Shift direction control signal. **(UDB always is inversion of UD)**
SYNC4	O	CPV to external GD.	O	CPV to external GD.
SYNC5	O	UD=H, This pin is Hi-z. UD=L, STV output control signal.	O	UDB=H, STV output control signal. UDB=L, This pin is Hi-z.
SYNC6	O	UD=H, STV output control signal. UD=L, This pin is Hi-z.	O	UDB=H, This pin is Hi-z. UDB=L, STV output control signal.
SYNC7	O	-	O	-
SYNC8	O	-	O	-
SYNC9_L	O	-	O	-
SYNC10_L	O	-	O	-
SYNC11_L	O	-	O	-
SYNC12_L	O	-	O	-

Table 6.5: Synchronized signals description with one chip application

6.3 GOA function

The HX8279-D01 can support GOA/GIP **(Gate driver on array)** function. The function enable can set by hardware or register. Hardware pin name is GOA_EN. Register address is locates 0xB8[7] at page0. The relationship between pin and register is shows below.

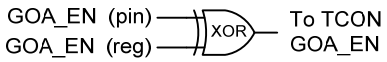
Combination Logic	Truth table		
	**PIN**	**REG**	**To TCON**
	0	0	0
	0	1	1
	1	0	1 **(Default)**
	1	1	0

Table 6.6: Truth table of GOA enable

SEL[5:0]	GOA Output
0x00	VGL
0x01	STV1
0x02	STV2
0x03	STV3
0x04	STV4
0x05	CKV1
0x06	CKV2
0x07	CKV3
0x08	CKV4
0x09	CKV5

SEL[5:0]	GOA Output
0x0A	CKV6
0x0B	CKV7
0x0C	CKV8
0x0D	CLR1
0x0E	CLR2
0x0F	CLR3
0x10	CLR4
0x11	FLC1
0x12	FLC2
0x13	GCKA

SEL[5:0]	GOA Output
0x14	GCKB
0x15	DIR
0x16	DIRB
0x17	STV5
0x18	STV6
0x19	STV7
0x1A	STV8
0x1B	CKV9
0x1C	CKV10
0x1D	CKV11

SEL[5:0]	GOA Output
0x1E	CKV12
0x1F	CKV13
0x20	CKV14
0x21	CKV15
0x22	CKV16
0x23	FLC1B
0x24	FLC2B
0x26	VGH

Table 6.7: GOA pin mapping table

6.4 Panel structure

6.4.1 Driving method for panel structure

HX8279-D01 can support 2 types of driving method – stripe and zigzag. The normal application is stripe. However for special case will be used zigzag. The number 0, 1801 and 1802 of source output channel is for zigzag.

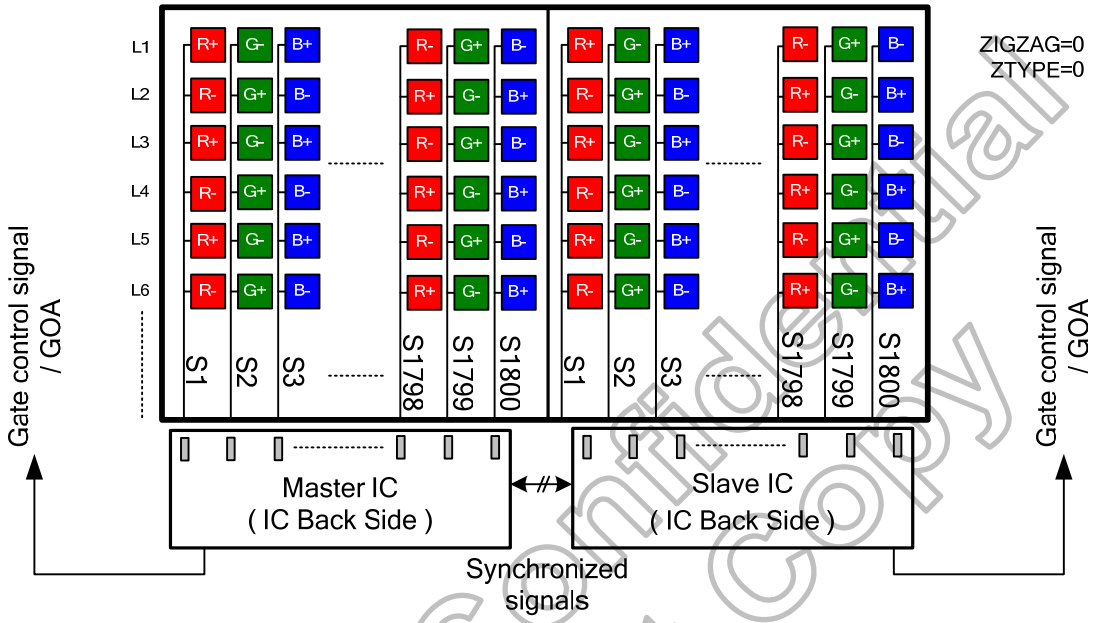
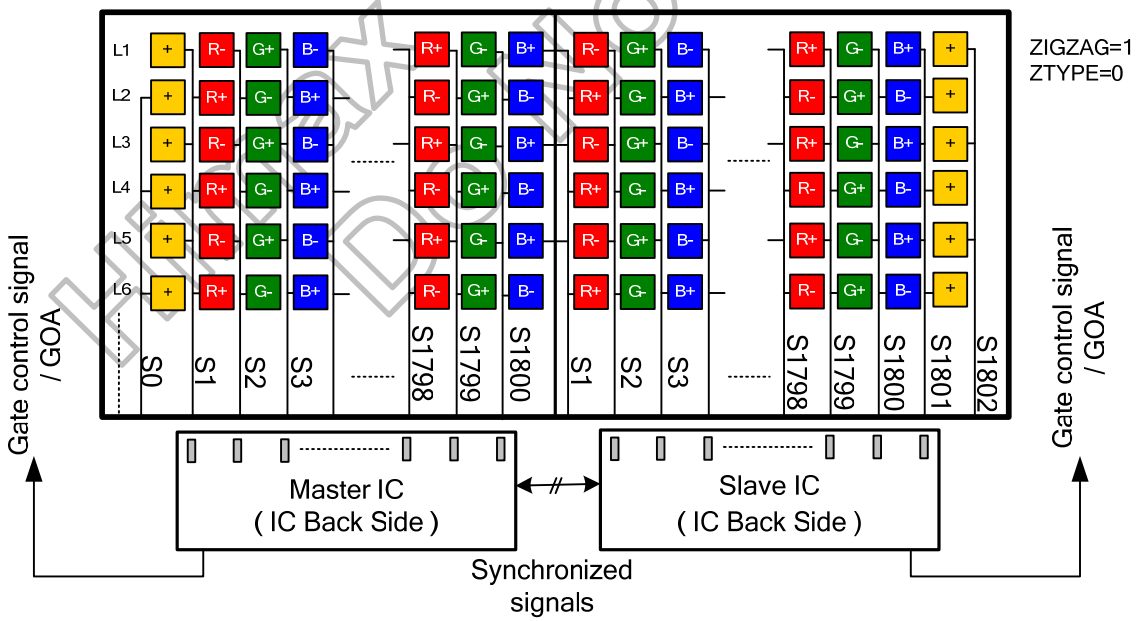
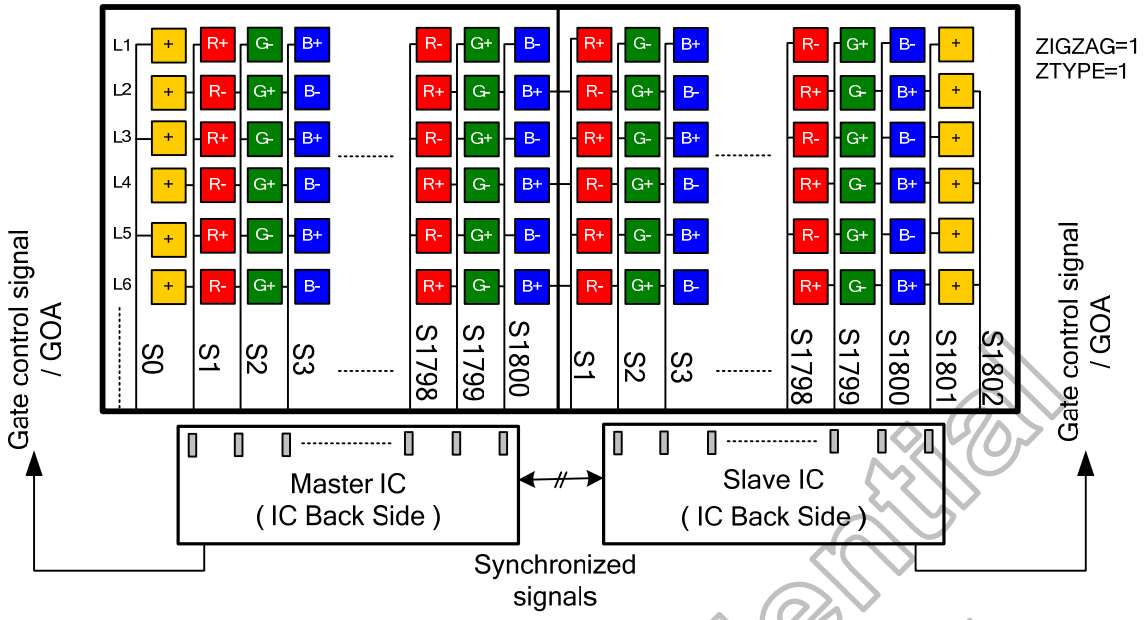


Figure 6.2: 1200RGBx1600 stripe driving method



Note: (1) Dummy data is setting by ZDATA[7:0] of register(reg page0 0xB5).
(2) Ztype is "0", the zigzag type is 0.

Figure 6.3: 1200RGBx1600 zigzag type0 driving method



Note: (1) Dummy data is setting by ZDATA[7:0] of register(reg page0 0xB5).
(2) Ztype is "1", the zigzag type is 1.

Figure 6.4: 1200RGBx1600 zigzag type1 driving method

7. MIPI Interface

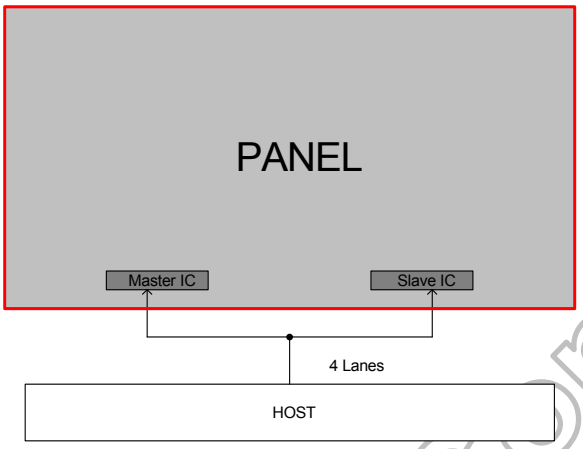
HX8279-D01 supports 2 types MIPI:

- Multi-Drop type, support 2 Lanes and 4 Lanes only.
- Left/right type, support 2+2 Lanes and 4+4 Lanes only.

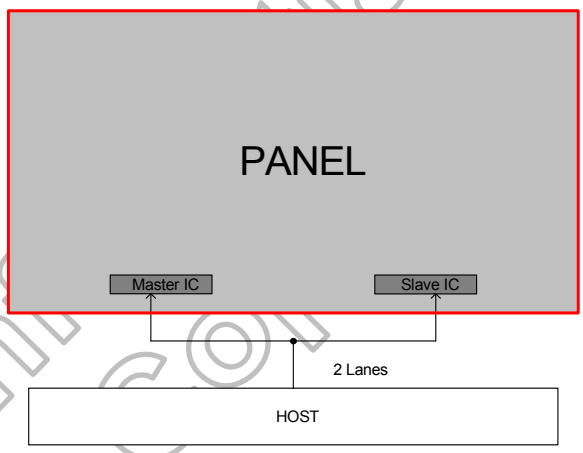
7.1 MIPI total bandwidth and maximal operation frequency

The maximum operation frequency per lane = 1Gbps.

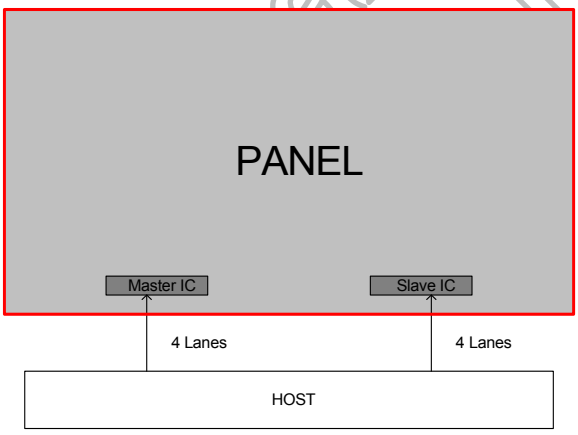
Multi-Drop MIPI (4 Lanes) :



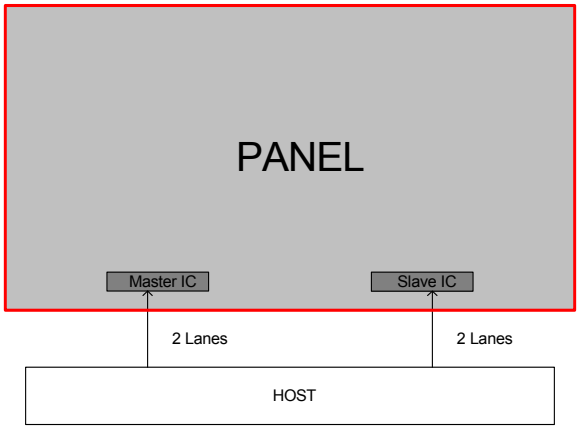
Multi-Drop MIPI (2 Lanes) :



Left / Right MIPI (4 Lanes) :

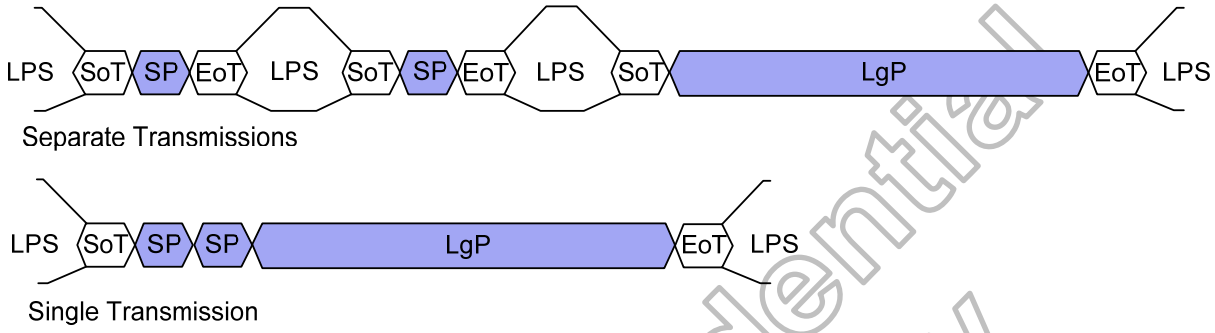


Left / Right MIPI (2 Lanes) :



7.2 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Below figure is illustrates multiple HS Transmission packets.

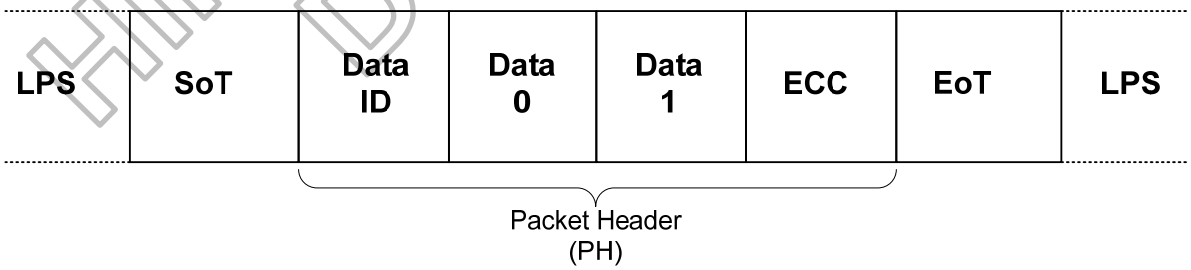


Note: (1) LPS: Low Power State;
SoT: Start of Transmission
SP: Short Packet
LgP: Long Packet
EoT: End of Transmission

Figure 7.1: Multiple packets transmission

The packet includes two types which are Long packet and Short packet. The first byte of the packet, the Data Identifier **(DI)**, includes information specifying the type of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

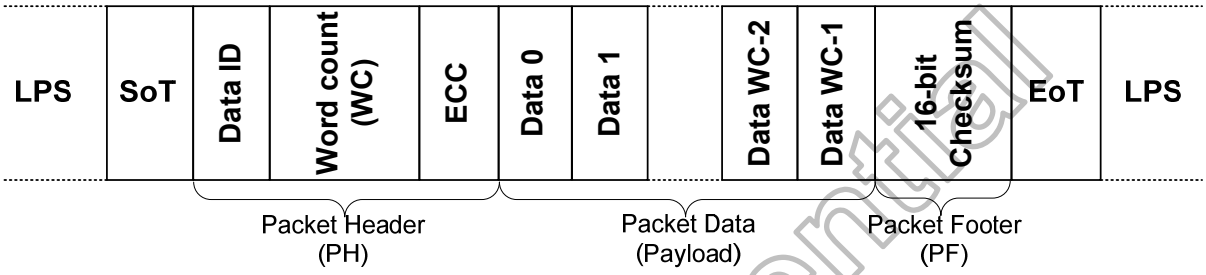
Short packets are four bytes in length including the ECC. Short packet is used for most Command Mode commands and associated parameters. Where Short packets format include an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC. Below figure is shows the structure of the Short packet.



Note: (1) DI **(Data ID)**: Contain Virtual Channel Identifier and Data Type.
ECC **(Error Correction Code)**: The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Short Packet.

Figure 7.2: Structure of the short packet

Long packets specify the payload length using a two-byte Word Count Field and then the payload maybe from 0 to 65,535 bytes in length. Thus Long packets permit transmission of large blocks of pixel or other data. Figure 7.3 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. An application-specific Data Payload has Word Count * bytes following the Packet Header. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length. Where 65,541 bytes = 4 bytes PH + (2^{16}-1) bytes Payload + 2 bytes PF



Note: (1) DI **(Data ID)**: Contain Virtual Channel Identifier and Data Type.
WC **(Word Count)**: The receiver uses WC to determine the packet end.
ECC **(Error Correction Code)**: The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
PF **(Packet Footer)**: Mean 16-bit Checksum.

Figure 7.3: Structure of the long packet

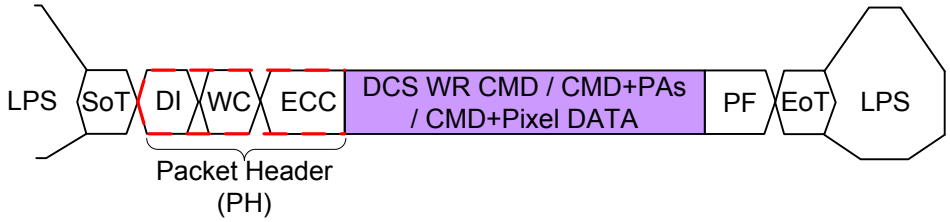
According to packet form, basic elements include DI and ECC. Below Table is shows format of Data ID.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC **(Virtual Channel)**		DT **(Data Type)**					

Note: (1) DI[7:6]→These two bits identify the data as directed to one of four virtual channels.
DI[5:0]→These six bits specify the Data Type, which specifies the size, format, and in some case, the interpretation of the packet contents.

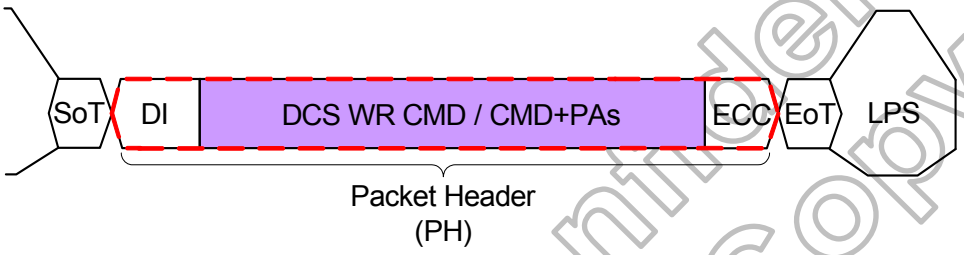
Table 7.1: Format of data ID

Due to Data Type **(DT)** mean format of transmission type. Below Figure 7.5 is shows short / long-packet transmission command sequence. Long packet writes command / parameters / pixel Data



Note: (1) DI: Write suitable Data type.
WC: Write number of Payload Data.
Ex: One CMD write, WC setting as 1.
CMD+PAs write, WC setting as number of **(CMD+PAs)**.
CMD+DATA write, WC setting as number of **(CMD+Pixel DATA)**.

Figure 7.4: Long packet writes command / parameters



Note: (1) D I: Write suitable Data type.
Ex: One CMD write, DI+DCS WR CMD
CMD+PAs write, DI+DCS WR CMD+PAs.

Figure 7.5: Show short-packet / long-packet transmission command sequence

7.3 Processor to peripheral (forward direction) packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 6.2 Data Types for Processor-sourced Packets.

Data type (Hex)	Data type (Binary)	Description packet	Size
01h	00_0001	Sync Event, V Sync Start	Short
11h	01_0001	Sync Event, V Sync End	Short
21h	10_0001	Sync Event, H Sync Start	Short
31h	11_0001	Sync Event, H Sync End	Short
08h	00_1000	End of Transmission packet **(EoTp)**	Short
22h	10_0010	Shut Down Peripheral Command	Short
32h	11_0010	Turn On Peripheral Command	Short
03h	00_0011	Generic Short WRITE, no parameter	Short
13h	01_0011	Generic Short WRITE, 1 parameter	Short
23h	10_0011	Generic Short WRITE, 2 parameter	Short
04h	00_0100	Generic READ, no parameter	Short
14h	01_0100	Generic READ, 1 parameter	Short
24h	10_0100	Generic READ, 2 parameter	Short
05h	00_0101	DCS Short WRITE, no parameter	Short
15h	01_0101	DCS Short WRITE, 1 parameter	Short
06h	00_0110	DCS READ, no parameters	Short
37h	11_0111	Set Maximum Return Packet Size	Short
09h	00_1001	Null Packet, no data	Long
19h	01_1001	Blanking Packet, no data	Long
29h	10_1001	Generic Long Write	Long
39h	11_1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00_1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01_1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10_1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11_1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
x0h and xFh, unspecified	xx_0000 xx_1111	DO NOT USE All unspecified codes are reserved	-

Table 7.2: Data types for processor-sourced packets

Under tables list all detail function of all data types

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type (Hex)	**Function description**	**Number of byte**
01h	V Sync start, Start of VSA pulse.	4 bytes **(DI+00h+00h+ECC)**
11h	V Sync End, End of VSA pulse.	
21h	H Sync Start, Start of HSA pulse.	
31h	H Sync End, End of HSA pulse.	

Note: (1) V Sync Start and V Sync End event represents the start and end of the VSA, respectively. Similarly H Sync Start and H Sync End event represents the start and end of the HSA, respectively.

End of Transmission packet (EoT)		
Data type (Hex)	**Function description**	**Number of byte**
08h	End of Transmission packet **(EoTp)**.	4 bytes **(DI+00h+00h+ECC)**

Display status (shutdown command, turn-on command)		
Data type (Hex)	**Function description**	**Number of byte**
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	4 bytes **(DI+00h+00h+ECC)**
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	

Note: (1) When use shutdown command; interface shall remain powered in order to receive the turn-on, or wake-up, command.

Generic Short WRITE Packet with 0,1,2 parameter		
Data type (Hex)	**Function description**	**Number of byte**
03h	Generic Short WRITE, no parameter.	**(DI+00h+00h+ECC)**
13h	Generic Short WRITE, 1 parameter.	**(DI+P1+00h+ECC)**
23h	Generic Short WRITE, 2 parameter.	**(DI+P1+P2+ECC)**

Note: (1) P1=parameter1, P2=parameter2

Generic READ Request with 0,1,2 parameter		
Data type (Hex)	**Function description**	**Number of byte**
04h	Generic READ no parameter.	**(DI+00h+00h+ECC)**
14h	Generic READ 1 parameter.	**(DI+P1+00h+ECC)**
24h	Generic READ 2 parameter.	**(DI+P1+P2+ECC)**

Note: (1) P1=parameter1, P2=parameter2

DCS Show WRITE Command with 0,1 parameter		
Data type (Hex)	**Function description**	**Number of byte**
05h	DCS Short WRITE, no parameter.	**(DI+DCS+00h+ECC)**
15h	DCS Short WRITE, 1 parameter.	**(DI+DCS+P1+ECC)**

Note: (1) P1=parameter1, DCS=DCS Command

DCS command setting		
Data type (Hex)	**Function description**	**Number of bytes**
06h	DCS Read command, the returned data may be of Short or Long packet format.	4 bytes **(DI+DCS CMD+00h+ECC)**
39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65541 bytes **(DI+WC+ECC+DCS CMD +Payload DATA+PF)**

Note: (1) For write part, If DCS Short Write command is followed by BTA, the peripheral shall respond with ACK when no error was detected in the transmission **(Host → Slave)**. Unless an error was detected, the peripheral shall respond with Acknowledge with Error Report.

(2) When use DCS Read Command, the Set Max Return Packet Size command will limit the size of returning packets.

(3) The peripheral shall respond to DCS Read Command Request in one of the following ways:

- If an error was detected and corrected in Packet Header field by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
- If no error was detected by the peripheral, it shall send the requested READ packet **(Short or Long)** with appropriate ECC and Checksum, if either or both features are enabled.

(4) One byte <= Length of payload DATA <= 2^{16}-1

Return packet size setting		
Data type (Hex)	**Function description**	**Number of bytes**
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	4 bytes **(DI+Maximum Return Packet Size+ECC)**

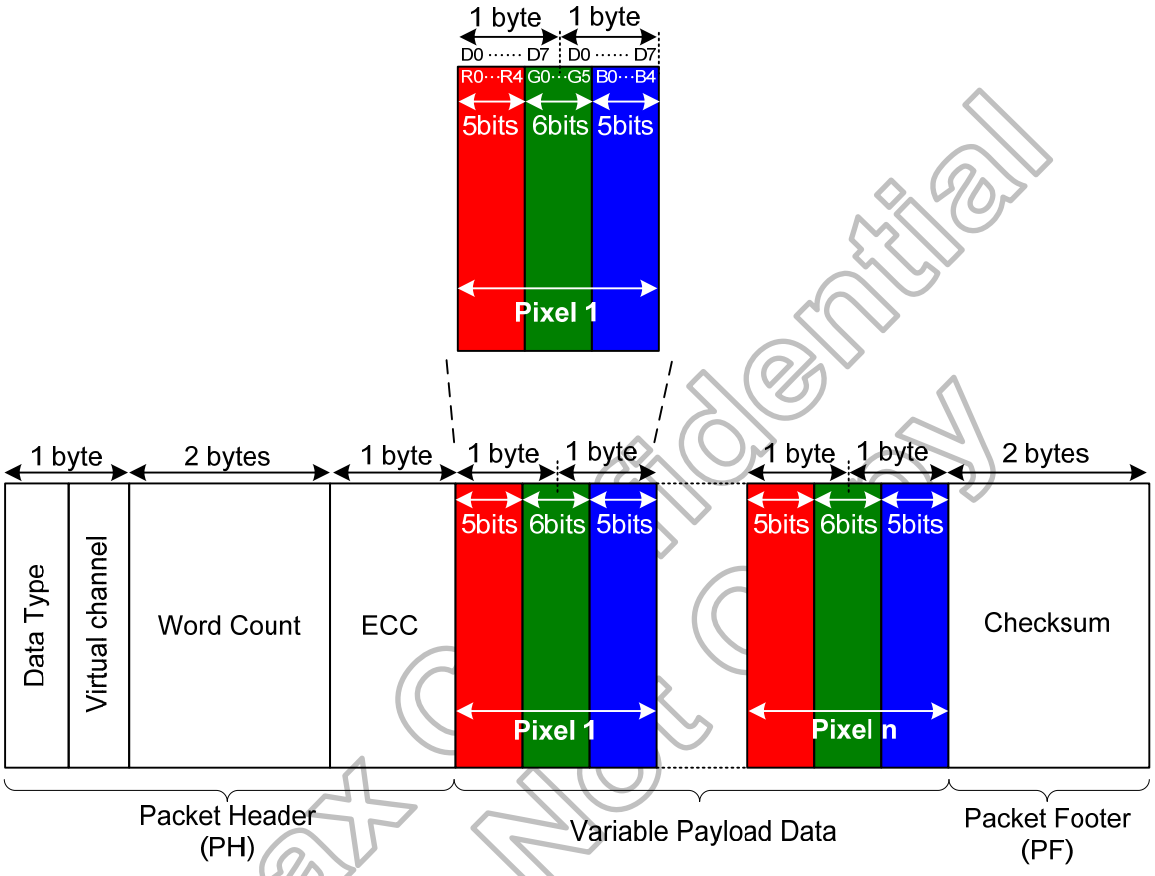
Note: (1) The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.

Variable data packet		
Data type (Hex)	**Function description**	**Number of bytes**
09h	Null Packet is a mechanism for keeping the serial Data Lane**(s)** in High-Speed mode while sending dummy data.	Up to 65541 bytes **(DI+WC+ECC+DCS CMD+Payload DATA +PF)**
19h	Blanking packet is used to convey blanking timing information in a Long packet.	

Note: (1) When Null Packet, the Payload Data belong “null” Data, actual data values sent are irrelevant because the peripheral does not capture or store the data.

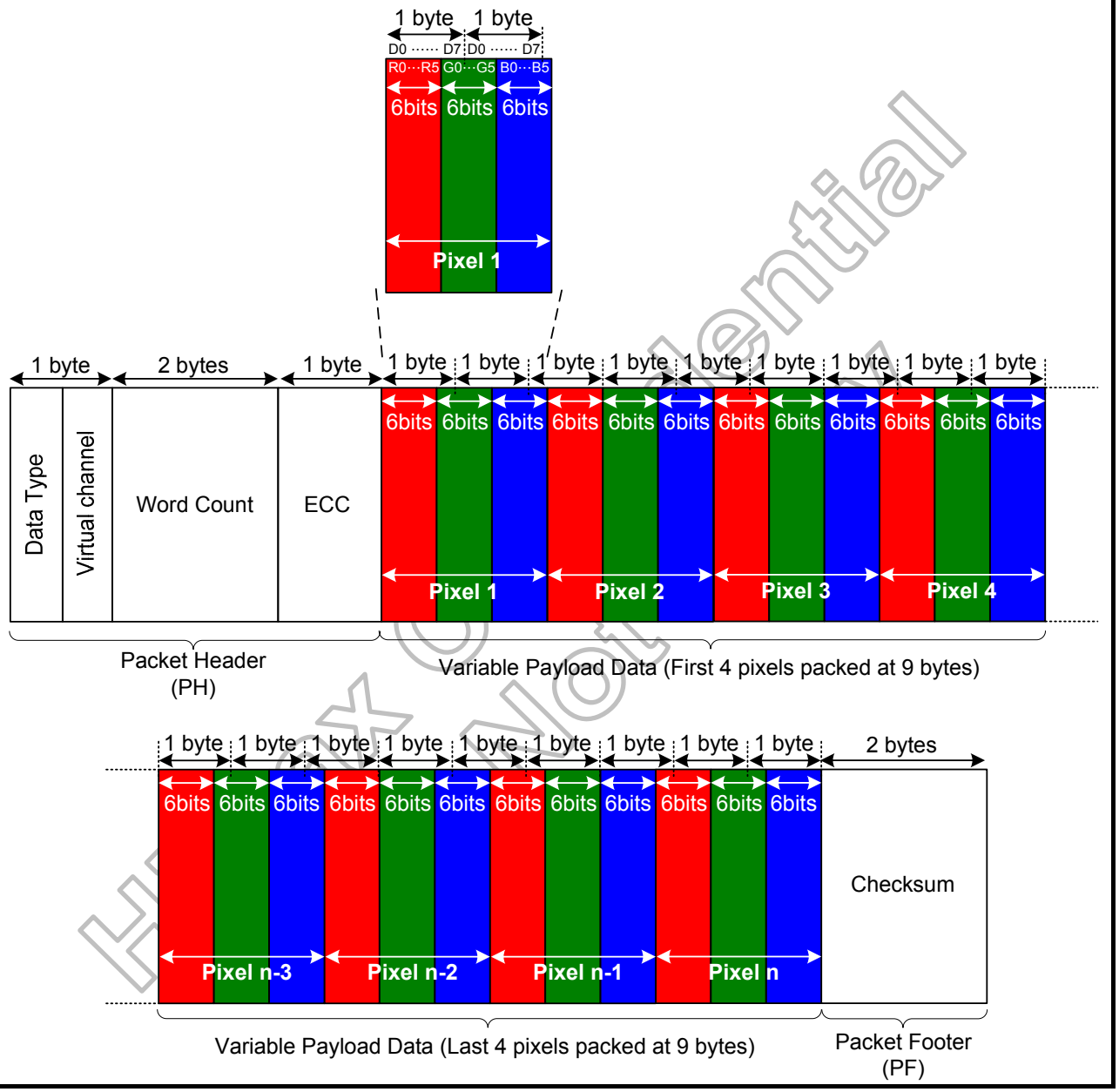
(2) When Blanking packet, the packet represents a period between active scan lines of a Video Mode display.

Data stream format – 16bit Format		
Data type (Hex)	**Function description**	**Number of bytes**
0Eh	Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "**(5-bit)** red, **(6-bit)** green and **(5-bit)** blue".	Up to 65541 bytes **(DI+WC+ECC+DCS CMD+Payload DATA+ PF)**



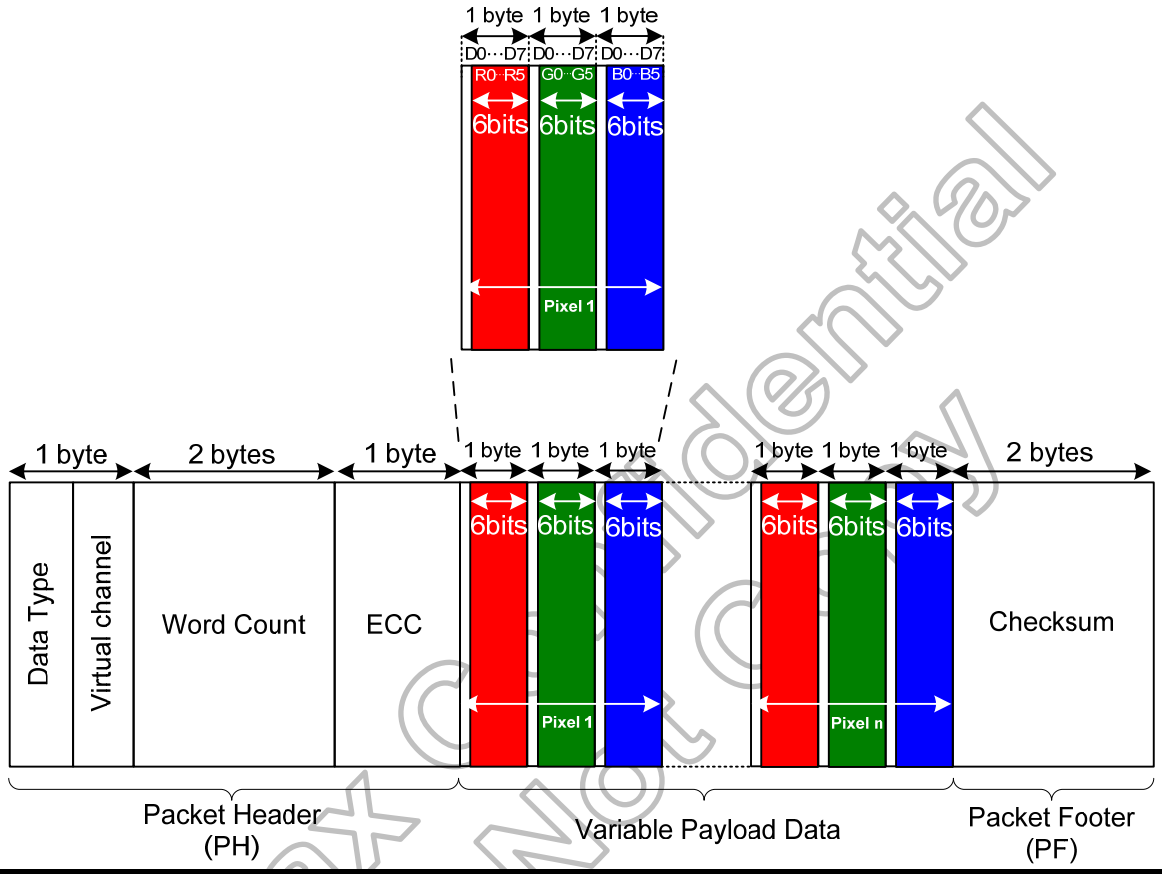
Note: (1) Within a color component, the "LSB is sent first, the MSB last ".

Data stream format – 18bit Format		
Data type (Hex)	**Function description**	**Number of bytes**
1Eh	Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is "**(6-bit)** red, **(6-bit)** green and **(6-bit)** blue".	Up to 65541 bytes **(DI+WC+ECC+DCS CMD+Payload DATA+PF)**



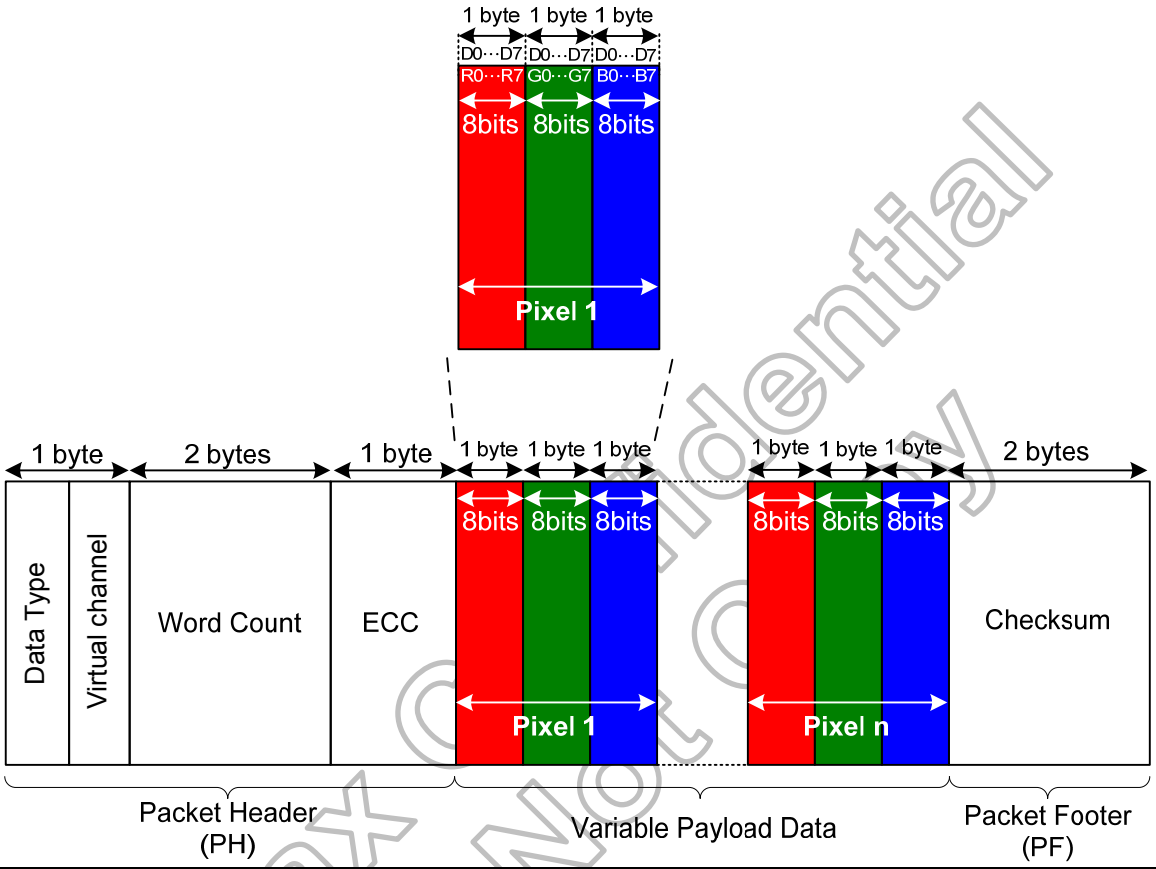
Note: (1) Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels **(nine bytes)**. Preferably, display modules employing this format have a horizontal extent **(width in pixels)** evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a "clean start" for the next line.

Data stream format – 18bit Format		
Data type (Hex)	**Function description**	**Number of bytes**
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is "**(6-bit)** red, **(6-bit)** green and **(6-bit)** blue".	Up to 65541 bytes **(DI+WC+ECC+DCS CMD+Payload DATA+PF)**



Note: (1) Within a color component, the LSB is sent first, the MSB last and with this format, pixel boundaries line up with byte boundaries every three bytes.

Data stream forma – 24bit Format		
Data Type (Hex)	**Function Description**	**Number of bytes**
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is **(8-bit)** red, **(8-bit)** green and **(8-bit)** blue.	Up to 65541 bytes **(DI+WC+ECC+DCS CMD +Payload DATA+PF)**

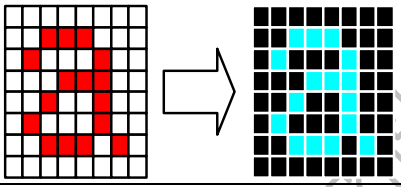


Note: (1) Within a color component, the LSB is sent first, the MSB last and with this format, pixel boundaries line up with byte boundaries every three bytes.

7.4 Display command set (DCS)

Command	Hex	Description	Number of Parameters
Enter invert mode	21h	Displayed image colors are inverted.	0
Enter sleep mode	10h	Power for the display panel is off.	0
Exit invert mode	20h	Displayed image colors are not inverted.	0
Exit sleep mode	11h	Power for the display panel is on.	0
Get display mode	0Dh	Get the current display mode from the peripheral.	1
Get power mode	0Ah	Get the current power mode.	1
Get signal mode	0Eh	Get display module signaling mode.	1
Nop	00h	No operation.	0
Set address mode	36h	Set the data order for transfers from the host to the display module and from the frame memory to the display device.	1
Set display off	28h	Blanks the display device.	0
Set display on	29h	Show the image on the display device.	0
Set tear off	34h	Synchronization information is not sent from the display module to the host processor.	0
Set tear on	35h	Synchronization information is sent from the display module to the host processor at the start of VFP	1
Set tear scan line	44h	Synchronization information is sent from the display module to the host processor when the display device refresh reaches the provided scan line.	2
Soft reset	01h	Software Reset.	0

7.4.1 Enter_invert_mode (21h)

21H	Enter_invert_mode (Display Inversion On)→INVON									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	0	0	0	0	1	21
Parameter	NO PARAMETER									
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) memory display 									
Restriction	This command has no effect when module is already in inversion no mode.									

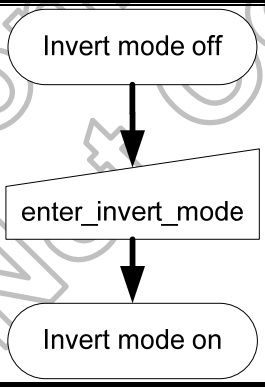
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

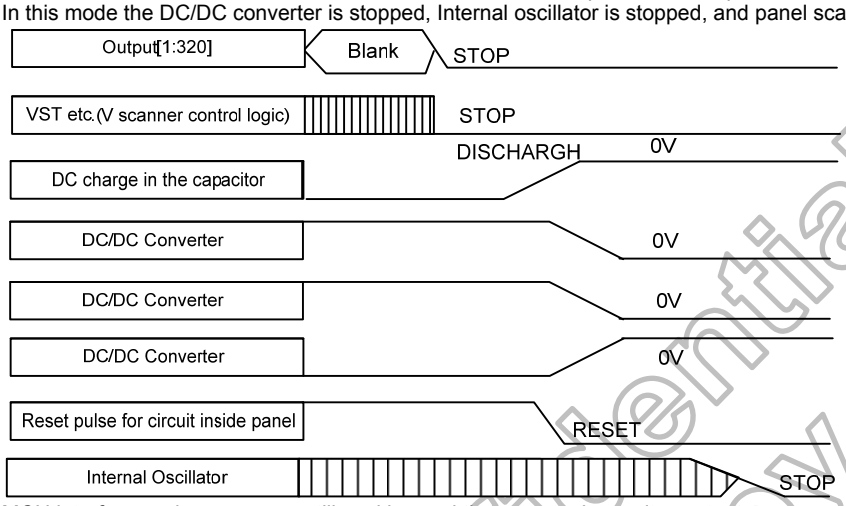
Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



7.4.2 Enter_sleep_mode (10h)

10H	Enter_sleep_mode (Sleep In)→SLPIN									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	1	0	0	0	0	10
Parameter	NO PARAMETER									
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.  MCU interface and memory are still working and the memory keeps its contents.									
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command **(11h)**. It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command **(when in Sleep In Mode)** before Sleep In command can be sent.									

Register Availability

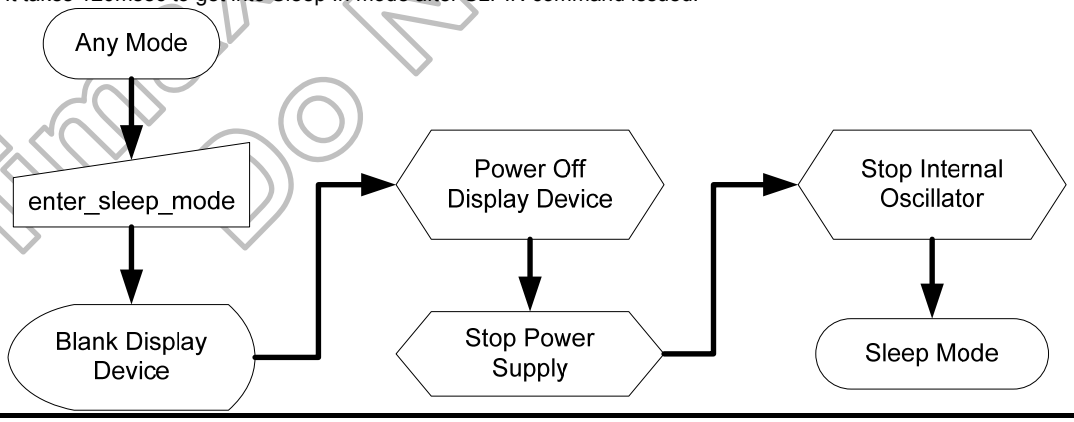
Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

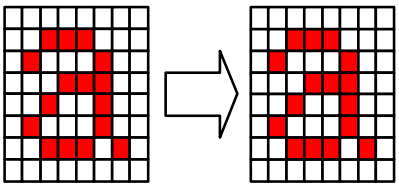
Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flowchart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



7.4.3 Exit_invert_mode (20h)

20H	Exit_invert_mode (Display Inversion Off)→INVOFF									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	0	0	0	0	0	20
Parameter	NO PARAMETER									
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display 									
Restriction	This command has no effect when module is already in inversion off mode.									

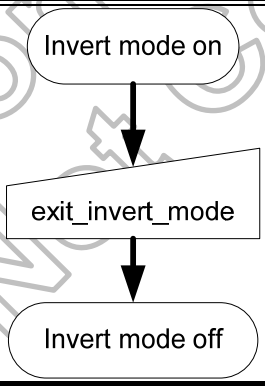
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

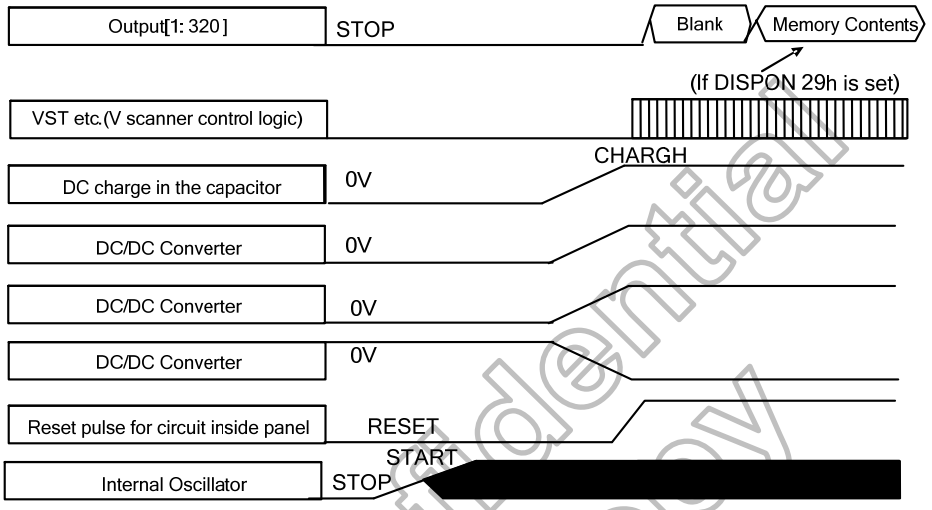
Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



7.4.4 Exit_sleep_mode (11h)

11H	Exit_sleep_mode (Sleep Out)→SLPOUT									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER									
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.									
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.									



Register Availability

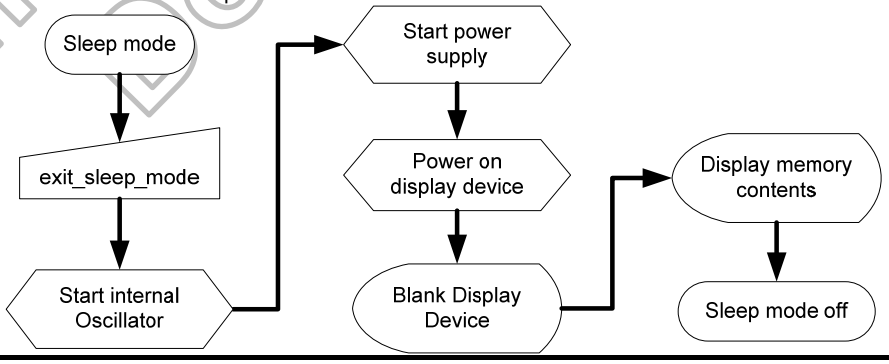
Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart

It takes 120msec to become Sleep Out mode after SLPOUT command issued.



7.4.5 Get_display_mode (0Dh)

0DH	Get_display_mode (Read Display Image Mode)→RDDIM									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	1	1	0	1	0D
1st parameter	D→H	0	0	D5	0	0	0	0	0	xx
Description	This command indicates the current status of the display : **Bit D5 – Inversion On/Off** '0' = Inversion is Off. '1' = Inversion is On. **Bit D7,D6,D4,D3,D2,D1,D0- Not Defined** Set to '0'									
Restrictions	-									

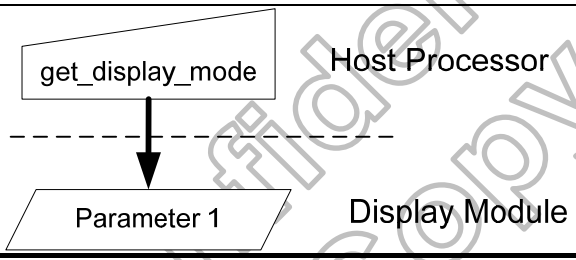
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No change
H/W Reset	00h

Flow Chart



7.4.6 Get_pixel_format (0Ch)

0C H	Get_pixel_format (Read Display COLMOD)→RDDCOLMOD									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	1	1	0	0	0C
1st parameter	D→H	0	D6	D5	D4	0	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Reserved	Set to '0'
D6	DPI Interface Pixel format	-
D5		-
D4		-
D3	Reserved	Set to '0'
D2	DBI Interface Pixel format -> Not Defined	Set to '0'
D1		Set to '0'
D0		Set to '0'

Bits D6, D5, D4 – DPI Pixel Format Definition
Bits D2, D1, D0 – DBI Pixel Format Definition-> Not Defined.

Interface Color Format	D6	D5	D4
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
24 bit/pixel	1	1	1

If a particular interface, either DSI or DPI, is not used then the corresponding bits in the parameter returned from the display module are undefined.

Restrictions

-

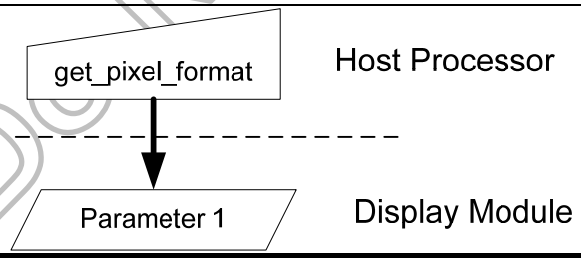
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24-bit/pixel
S/W Reset	24-bit/pixel
H/W Reset	24-bit/pixel

Flow Chart



7.4.7 Get_power_mode (0Ah)

0AH	Get_power_mode (Read Display Power Mode)→RDDPM									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	1	0	1	0	0A
1st parameter	D→H	0	0	0	D4	0	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Not Defined	Set to '0'
D6	Not Defined	Set to '0'
D5	Not Defined	Set to '0'
D4	Sleep In/Out	-
D3	Not Defined	Set to '0'
D2	Display On/Off	-
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Bit D4 – Sleep In/Out
'0' = Sleep In Mode.
'1' = Sleep Out Mode.
Bit D2 – Display On/Off
'0' = Display is Off.
'1' = Display is On.
Bit D7,D6,D5,D3,D1,D0 – Not Defined
Set to '0'

Restrictions

-

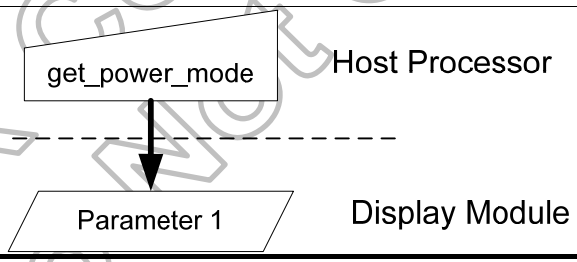
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



7.4.8 Get_signal_mode (0Eh)

0EH	Get_signal_mode (Read Display Signal Mode)→RDDSM									
	Direction	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	H→D	0	0	0	0	1	1	1	0	0E
1st parameter	D→H	D7	D6	0	0	0	0	0	0	xx
Description	This command indicates the current status of the display as described in the table below: **Bit D7 – Tearing Effect Line On/Off** '0' = Tearing Effect Line Off. '1' = Tearing Effect On. **Bit D6 – Tearing Effect Line Output Mode** See section set_tear_on **(35h)** for mode definitions. '0' = Mode 0. **(M=0)** '1' = Mode 1. **(M=1)** **Bit [D5:D0]** –reserved Set to '0'.									
Restrictions	-									

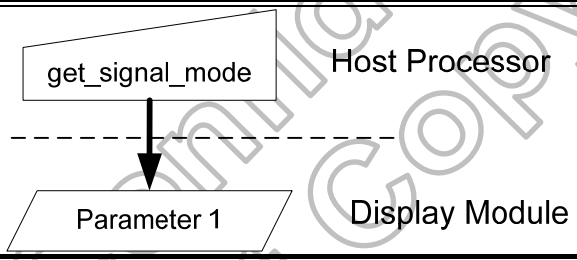
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



7.4.9 NOP (00h)

00H	NOP (No Operation)									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER									
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write as described in RAMWR **(Memory Write)** or RAMRD **(Memory Read)** command.									
Restriction	-									
Register Availability	**Status** / **Availability** Sleep Out / Yes Sleep In / Yes									
Default	**Status** / **Default Value** Power On Sequence / N/A S/W Reset / N/A H/W Reset / N/A									
Flow Chart	-									

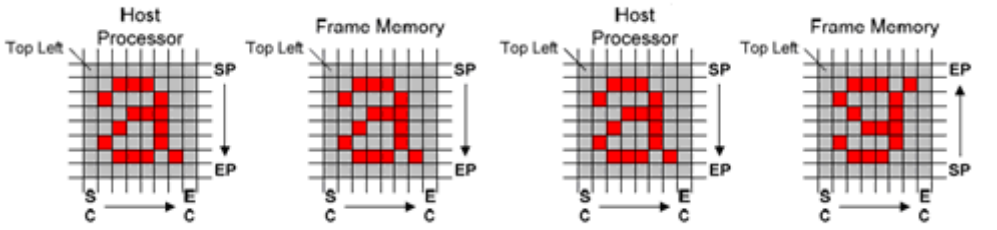
7.4.10 Set_address_mode (36h)

36H	Set_address_mode (Memory Access Control)→MADCTL									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	0	1	1	0	36
1st parameter	H→D	0	0	0	0	BGR	0	MX	MY	-

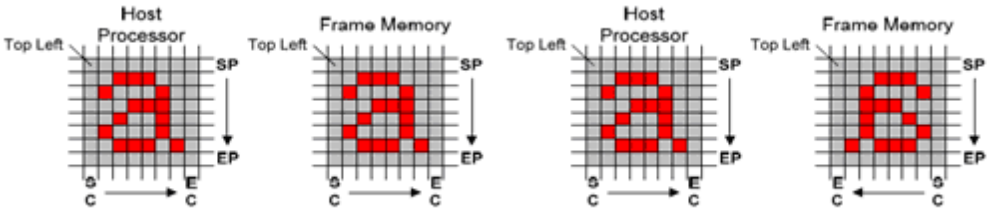
Description

This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status. Below table is bit assignment.

Bit	Name	Description
B7	Not Defined	-
B6	Not Defined	-
B5	Not Defined	-
B4	Not Defined	-
B3	RGB-BGR ORDER (BGR)	Color selector switch control 0=RGB color filter panel, 1=BGR color filter panel
B2	Not Defined	-
B1	COLUMN ADDRESS ORDER (MX)	0= left to right , 1= right to left
B0	PAGE ADDRESS ORDER (MY)	0= top to bottom , 1= bottom to top



D0=0 D0=1



D1=0 D1=1

D3=0

D3=1

Restriction

-

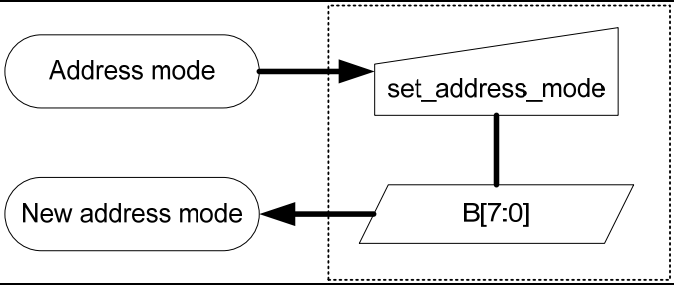
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

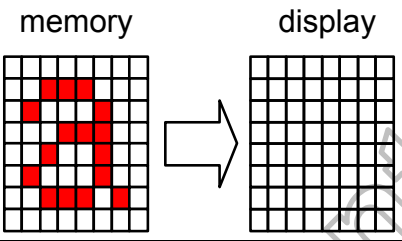
Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No change
H/W Reset	00h

Flow Chart



7.4.11 Set_display_off (28h)

28H	Set_display_off (Display Off)→DISPOFF									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	0	1	0	0	0	28
Parameter	NO PARAMETER									
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) 									
Restriction	This command has no effect when module is already in display off mode.									

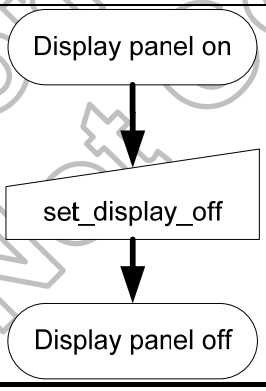
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

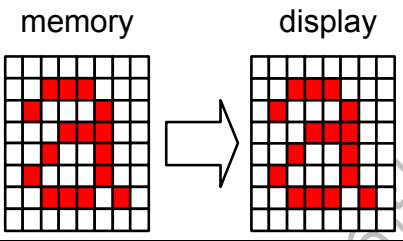
Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



7.4.12 Set_display_on (29h)

29H	Set_display_on (Display On)→DISPON									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	0	1	0	0	1	29
Parameter	NO PARAMETER									
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 									
Restriction	This command has no effect when module is already in display on mode.									

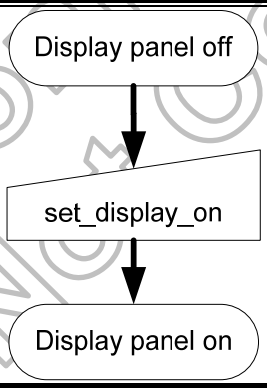
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



7.4.13 Set_tear_off (34h)

34H	Set_tear_off (Tearing Effect Line OFF)→TEOFF									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	0	1	0	0	34
Parameter	No Parameter									
Description	This command is used to turn OFF the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when Tearing Effect output is already OFF.									

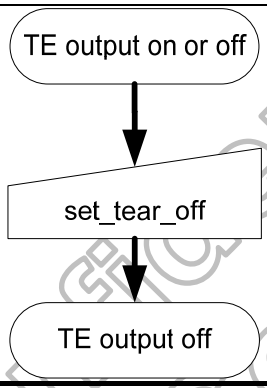
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect Off
S/W Reset	Tearing Effect Off
H/W Reset	Tearing Effect Off

Flow Chart



7.4.14 Set_tear_on (35h)

35H	Set_tear_off (Tearing Effect Line ON)→TEON									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	0	1	0	1	35
1stparameter	H→D	-	-	-	-	-	-	-	M	-

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. **(X=Don't Care)**

When **M=0 (mode0)** :
The Tearing Effect Output line consists of V-Blanking information only:

When **M=1 (mode1)** :
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

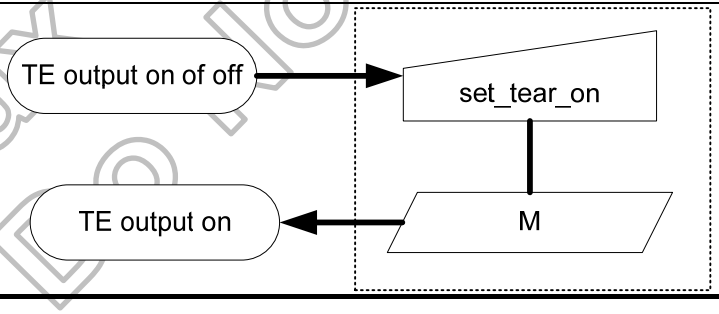
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

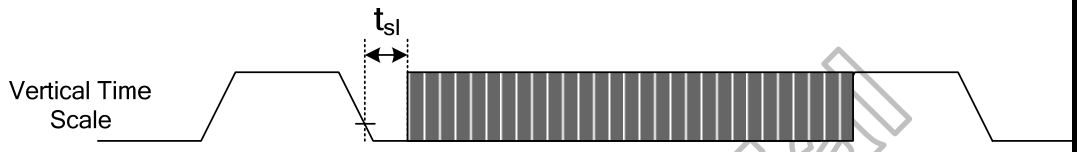
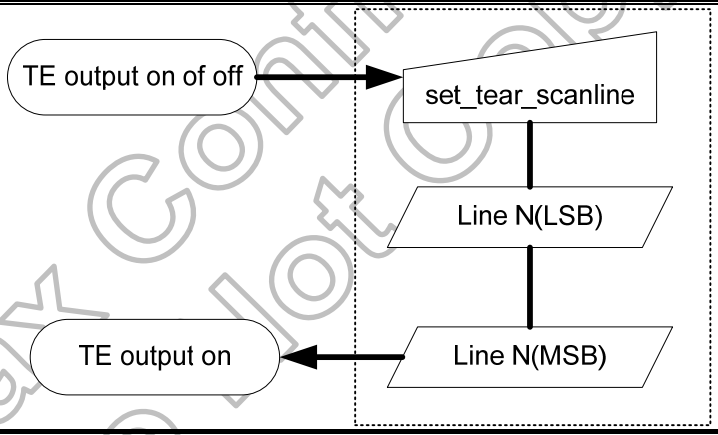
Default

Status	Default Value
Power On Sequence	Tearing Effect Off
S/W Reset	Tearing Effect Off
H/W Reset	Tearing Effect Off

Flow Chart



7.4.15 Set_tear_scanline (44h)

44H	Set_tear_scanline (Tear Effect Scan Lines)→TESL									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	1	0	0	0	1	0	0	44
1st parameter	H→D	N15	N14	N13	N12	N11	N10	N9	N8	00..FF
2nd parameter	H→D	N7	N6	N5	N4	N3	N2	N1	N0	00..FF
Description	This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reaches line N. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. The Tearing Effect Output line consists of V-Blanking information only:  **Note:** That N=0 is equivalent to set_tear_on with M=0.(default value of N is 0) The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.									
Restriction	The command has no effect when Tearing Effect output is already ON.									
Register Availability	**Status** / **Availability** Sleep Out / Yes Sleep In / Yes									
Default	**Status** / **Default Value** Power On Sequence / N[15:0]=0000h S/W Reset / N[15:0]=0000h H/W Reset / N[15:0]=0000h									
Flow Chart	 									

7.4.16 Soft_reset (01h)

01H	SWRESET (Software Reset)									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER									
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. **(See default tables in each command description.)** The display is blank immediately. **Note:** The frame memory contents are unaffected by this command.									
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5m sec. If SW Reset is applied during Sleep In mode, it will be necessary to wait 120m sec before sending Sleep Out command. SW Reset command cannot be sent during Sleep Out mode.									

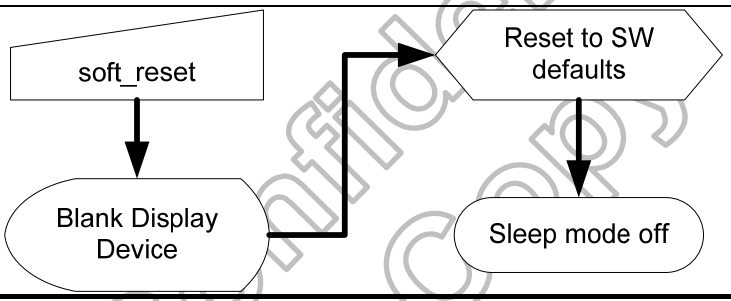
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



7.5 MIPI video input timing

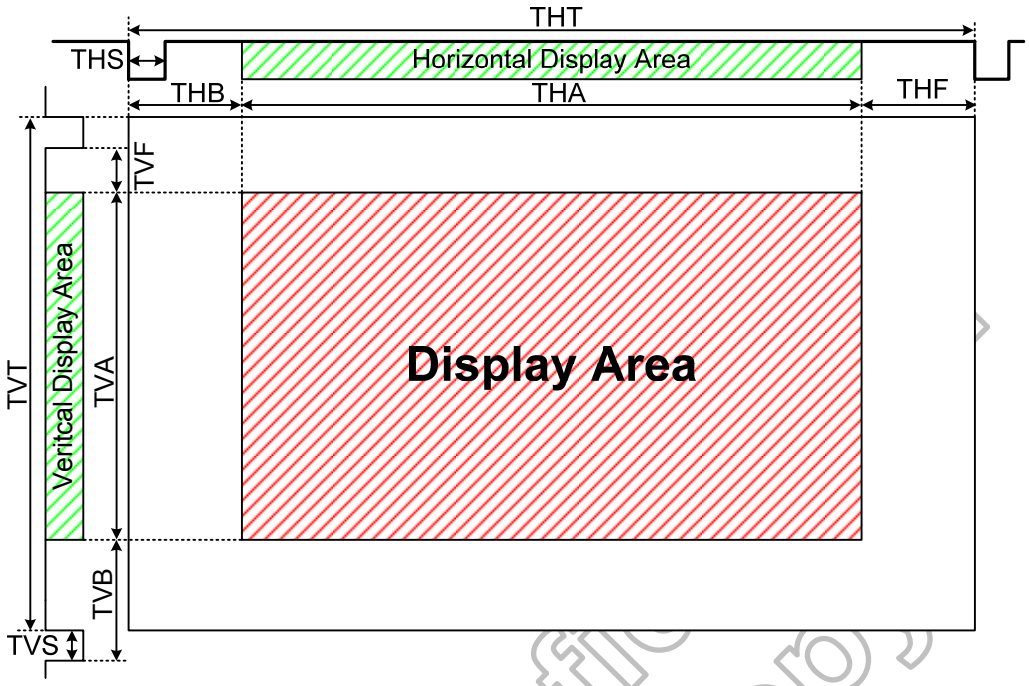
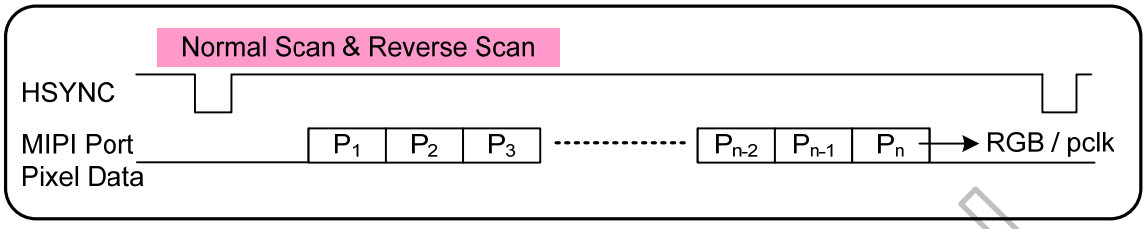


Figure 7.6: MIPI video input timing

7.5.1 Video input timing for Multi-Drop type

MIPI Multi-Drop type when normal or reverse scan.



Input Timing	Symbol	1200RGBx1920			1200RGBx1600			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
PCLK Frequency	-	-	156	-	-	131	-	MHz
Horizontal Total	THT	1270	1340	2047	1270	1340	2047	DCLK
Horizontal Synchronization	THS	10	24	-	10	24	-	DCLK
Horizontal Back Porch	THB(1)	50	80	-	50	80	-	DCLK
Horizontal Address	THA	-	1200	-	-	1200	-	DCLK
Horizontal Front Porch	THF	20	60	-	20	60	-	DCLK
Vertical Frequency	-	-	60	-	-	60	-	Hz
Vertical Total(2)	TVT	(3)	1944	2047	(3)	1624	1750	THT
Vertical Synchronization	TVS	(3)	2	-	(3)	2	-	THT
Vertical Back Porch	TVB	(3)	10	-	(3)	10	-	THT
Vertical Address	TVA	(3)	1920	-	(3)	1600	-	THT
Vertical Front Porch	TVF	(3)	14	-	(3)	14	-	THT

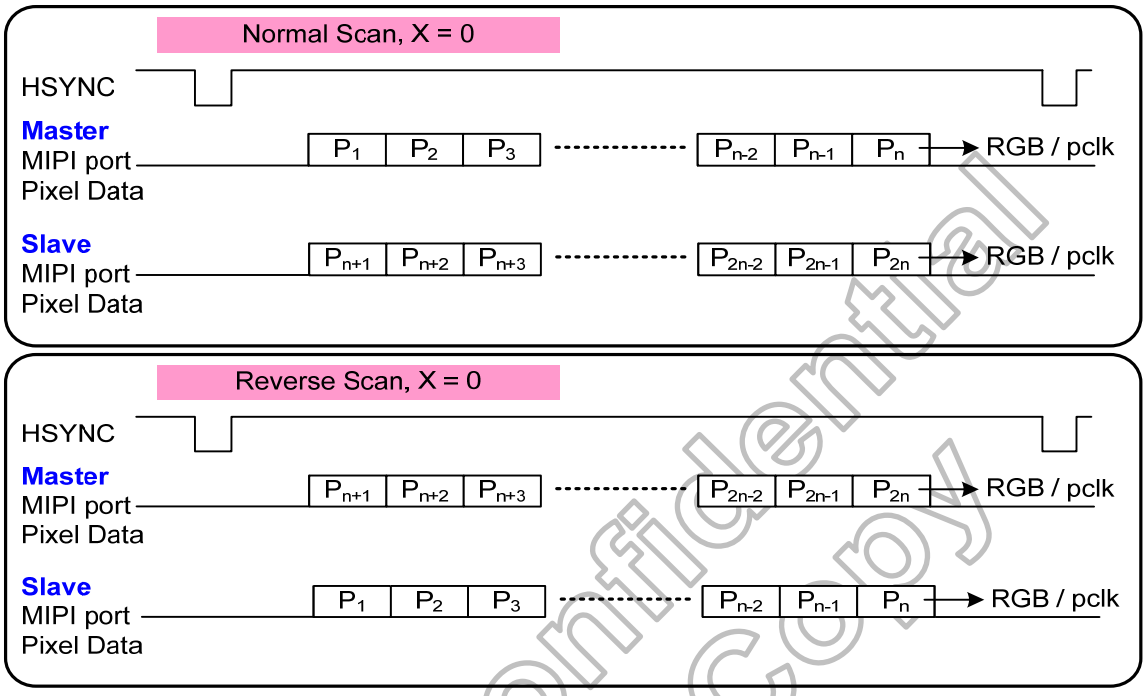
Input Timing	Symbol	1080RGBx1920			600RGBx1024			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
PCLK Frequency	-	-	142	-	-	48	-	MHz
Horizontal Total	THT	1150	1220	2047	670	760	1200	DCLK
Horizontal Synchronization	THS	10	24	-	10	24	-	DCLK
Horizontal Back Porch	THB(1)	50	80	-	50	80	-	DCLK
Horizontal Address	THA	-	1080	-	-	600	-	DCLK
Horizontal Front Porch	THF	20	60	-	20	80	-	DCLK
Vertical Frequency	-	-	60	-	-	60	-	Hz
Vertical Total(2)	TVT	(3)	1944	2047	(3)	1056	1176	THT
Vertical Synchronization	TVS	(3)	2	-	(3)	2	-	THT
Vertical Back Porch	TVB	(3)	10	-	(3)	10	-	THT
Vertical Address	TVA	(3)	1920	-	(3)	1024	-	THT
Vertical Front Porch	TVF	(3)	14	-	(3)	22	-	THT

Note: (1) THB includes THS.
(2) (Vertical frequency) x THTxTVTx24bits →total operation bandwidth.
(3) The min. value of Vertical porch is depending on GOA timing.Please refers to the AP. Note for the min value.

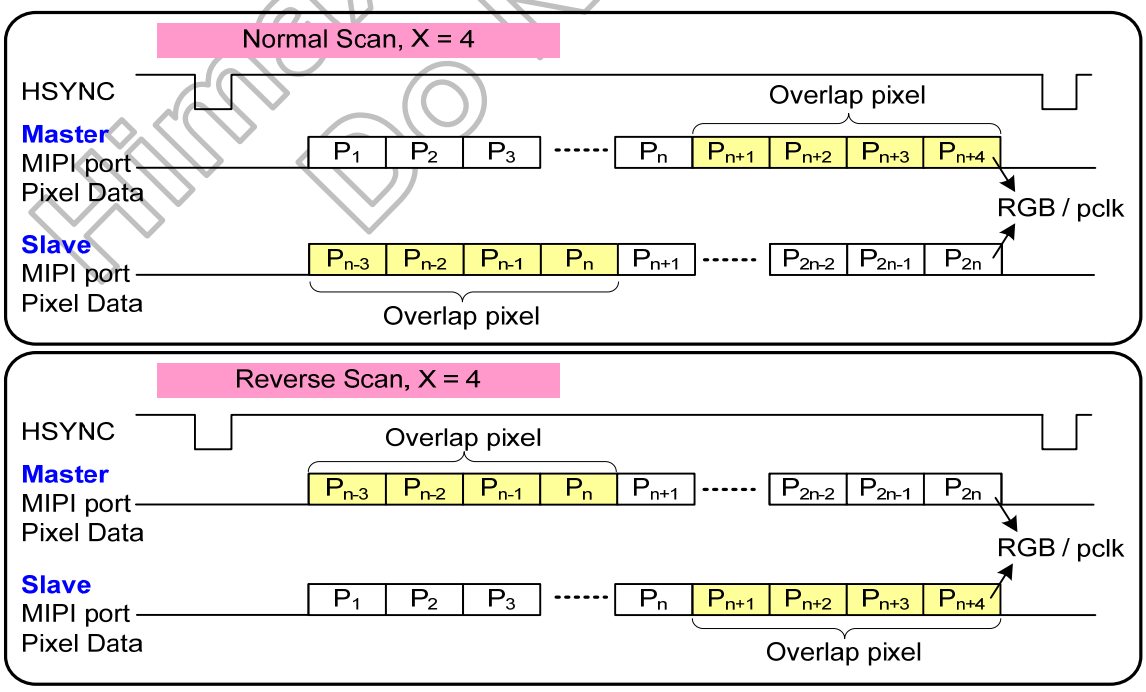
Table 7.3: MIPI input video timing for multi-drop type

7.5.2 Video input timing for RL type

MIPI R/L type timing when normal and reverse scan. Below figure is no overlap X=0 between left and right display data. The value of X can be setting by page0 0xB7[2:1].



At MIPI R/L type, it supports overlap X= 2,4 between left and right display data. Below figure is example for overlap X=4. The value of X can be setting by REG OVERLAP (page0 0xB7[2:1]). **The overlap pixel must be sent in the zigzag panel application.**



Input Timing	Symbol	1200RGBx1920			1200RGBx1600			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
PCLK Frequency	-	-	86	-	-	72	-	MHz
Horizontal Total	THT	670	740	1200	670	740	1200	DCLK
Horizontal Synchronization	THS	10	24	-	10	24	-	DCLK
Horizontal Back Porch	THB(1)	50	80	-	50	80	-	DCLK
Horizontal Address	THA	-	600	-	-	600	-	DCLK
Horizontal Front Porch	THF	20	60	-	20	60	-	DCLK
Vertical Frequency	-	-	60	-	-	60	-	Hz
Vertical Total(2)	TVT	(3)	1944	2047	(3)	1624	2047	THT
Vertical Synchronization	TVS	(3)	2	-	(3)	2	-	THT
Vertical Back Porch	TVB	(3)	10	-	(3)	10	-	THT
Vertical Address	TVA	(3)	1920	-	(3)	1600	-	THT
Vertical Front Porch	TVF	(3)	14	-	(3)	14	-	THT

Input Timing	Symbol	1080RGBx1920			Unit
		Min.	Typ.	Max.	
PCLK Frequency	-	-	77	-	MHz
Horizontal Total	THT	610	660	1080	DCLK
Horizontal Synchronization	THS	10	24	-	DCLK
Horizontal Back Porch	THB(1)	50	80	-	DCLK
Horizontal Address	THA	-	540	-	DCLK
Horizontal Front Porch	THF	20	60	-	DCLK
Vertical Frequency	-	-	60	-	Hz
Vertical Total(2)	TVT	(3)	1944	2047	THT
Vertical Synchronization	TVS	(3)	2	-	THT
Vertical Back Porch	TVB	(3)	10	-	THT
Vertical Address	TVA	(3)	1920	-	THT
Vertical Front Porch	TVF	(3)	14	-	THT

Note: (1) THB includes THS.
(2) (Vertical frequency) x THTxTVTx24bits →total operation bandwidth.
(3) The min. value of Vertical porch is depending on GOA timing.Please refers to the AP. Note for the min value.

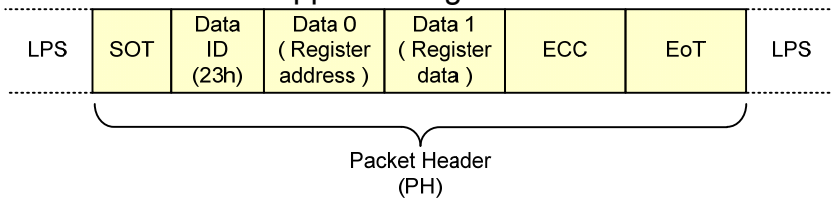
Table 7.4: MIPI input video timing for RL type

8. Register table

The HX8279-D01 can set internal register by MIPI or SPI.

8.1 MIPI control register

The HX8279-D01 supports the generic short write command to set internal register.



Note: (1) Data ID: Contain virtual channel identifier and data type.
(2) ECC **(Error Correction Code)**: The error correction code allows single-bit errors to be corrected and 2-bit errors to be detected in the short packet.

Figure 8.1: Support the DSI data short write

8.2 SPI control register

The HX8279-D01 supports the 4-wire serial peripheral interface **(SPI)** to set internal register. The basic operation of SPI interface is shown below. The Host asserts the CSB when it wants to initiate a read or write transaction. This is followed by the Host sending 16 pulses on the SPI clock **(SCK)**. The 8th bit of SCK pulses is the read/write command. **(0=Write, 1=Read)**. The Host de-asserts the CSB to indicate end of transfer.

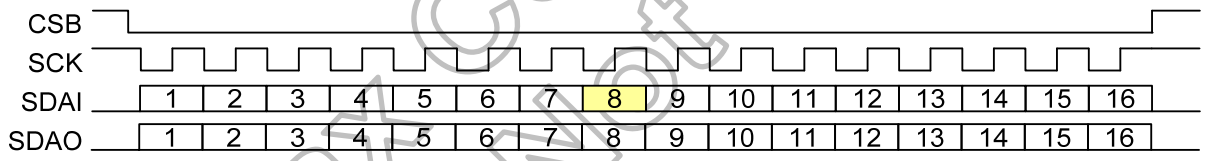


Figure 8.2: SPI basic operation

8.3 SPI read/write timing

The typical SPI writes operation is shows following figure.

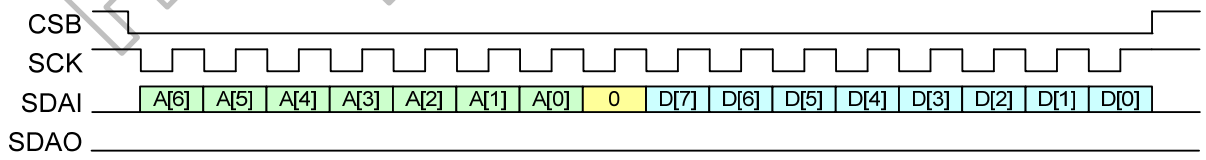


Figure 8.3: SPI write operation

The typical SPI reads operation is shows following figure.

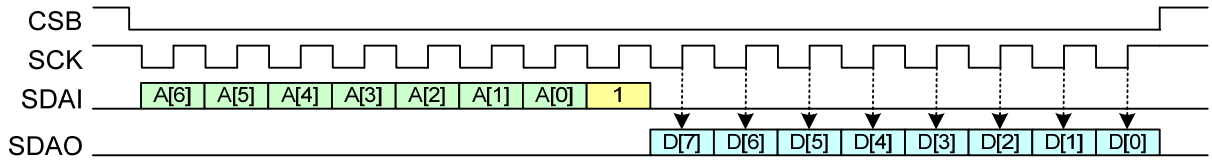


Figure 8.4: SPI read operation

8.4 Register table list

Register page selection

Addr[7:0]	Default[7:0]	OTP	Bit name	Data[7:0]								Description
				7	6	5	4	3	2	1	0	
0xB0	0Fh	-	Page_sel	-	-	-	-	1	1	1	1	Register page selection 0~12

The register page selection is set up individually by MIPI and SPI.

MSB bit [7] of address is only for MIPI interface. The SPI must be ignored its.

8.4.1 Register of page 0

MIPI Addr[7:0]	Default[7:0]	OTP	Bit name	Data[7:0]								Description
				7	6	5	4	3	2	1	0	
0xB1	00h	v	VENDER_ID[6:0]	-	0	0	0	0	0	0	0	driver ID and module ID
0xB2	40h	v	SLEEP	-	1	-	-	-	-	-	-	sleep mode control
		v	UPDNB	-	-	0	-	-	-	-	-	V-scan direction control
		v	LR	-	-	-	0	-	-	-	-	H-scan direction control
		v	ZIGZAG	-	-	-	-	0	-	-	-	panel type selection
		v	ZTYPE	-	-	-	-	-	0	-	-	Zigzag type selection
		v	NBW	-	-	-	-	-	-	0	-	panel normal white/black selection
		v	BISTB	-	-	-	-	-	-	-	0	BIST mode control
0xB3	08h	v	DISP_ON	0	-	-	-	-	-	-	-	display on/off control
		v	LPM_CTRL	-	0	0	-	-	-	-	-	low power mode selection
		v	PWRMD	-	-	-	0	-	-	-	-	power mode selection
		v	VRES_FIX	-	-	-	-	1	-	-	-	display vertical line decide by(1):RES[2:0] or (0) VRES
		v	LED_EN	-	-	-	-	-	0	-	-	LEDON pin output control
		v	RES[1:0]	-	-	-	-	-	-	0	0	resolution selection
0xB4	C0h	v	VRES[7:0]	1	1	0	0	0	0	0	0	vertical resolution selection
0xB5	00h	v	ZDATA[7:0]	0	0	0	0	0	0	0	0	ZigZag dummy data selection
0xB6	00h	v	RP1EN	-	0	-	-	-	-	-	-	odd repair OP on/off control.
		v	RP2EN	-	-	0	-	-	-	-	-	even repair OP on/off control.
		v	CABC_CTRL[1:0]	-	-	-	-	0	0	-	-	CABC-Mode selection
		v	DITHER_EN	-	-	-	-	-	-	0	-	dithering on/off control
		v	D_GAM_EN	-	-	-	-	-	-	-	0	digital gamma on/off control
0xB7	00h	v	OVERLAP	-	-	-	-	-	0	0	-	MIPI OVERLAP selection
		v	PCLK_SEL	-	-	-	-	-	-	-	0	TCON PCLK source
0xB8	00h	v	GOA_EN	0	-	-	-	-	-	-	-	GOA on/off control
		v	PNSW	-	-	0	-	-	-	-	-	MIPI pin polarity swap
		v	MIPI_TYPE	-	-	-	0	-	-	-	-	MIPI mode selection
		v	LNSW	-	-	-	-	0	0	-	-	MIPI lane swap
		v	MIPI_LAN	-	-	-	-	-	-	0	0	MIPI lane number selection
0xBA	8Fh	v	BLREV	1	0	-	-	-	-	-	-	source output at V-blanking
		v	BLREVONOFF	-	-	0	-	-	-	-	-	source output at power on off
		v	INV_SEL2	-	-	-	0	-	-	-	-	data inversion select
		v	SD_ISSEL[1:0]	-	-	-	-	1	1	-	-	source bias current select
		v	INV_SEL[1:0]	-	-	-	-	-	-	1	1	data inversion select
0xBD	71h	v	T_VCOMS[7:0]	0	1	1	1	0	0	0	1	VCOM voltage selection
0xBE	70h	v	LPM_VCOMS[7:0]	0	1	1	1	0	0	0	0	VCOM voltage selection in LPM
0xBF	19h	v	VGHS[4:0]	-	-	-	1	1	0	0	1	VGH voltage selection
0xC0	10h	v	VGLS[4:0]	-	-	-	1	0	0	0	0	VGL voltage selection
0xC1	1Fh	v	VGLXSP	-	-	-	1	-	-	-	-	VGH boosting multiple selection
		v	VGHXSP[1:0]	-	-	-	-	1	1	-	-	VGH boosting multiple selection

		v	CPCLKH [1:0]	-	-	-	-	-	-	1	1	VGH/VGL charge pump clock selection
0xC2	04h	v	VGPHS[4:0]	-	-	-	0	0	1	0	0	positive gamma_H selection
0xC3	02h	v	VGPLS[4:0]	-	-	-	0	0	0	1	0	positive gamma_L selection
0xC4	04h	v	VGNHS[4:0]	-	-	-	0	0	1	0	0	negative gamma_H selection
0xC5	02h	v	VGNLS[4:0]	-	-	-	0	0	0	1	0	negative gamma_L selection
0xC6	10h	v	STILLIMG_DET_NUM	-	0	0	1	0	0	0	0	still image detect frame number
0xC7	00h	v	REF_NUM[3:0]	-	-	-	-	0	0	0	0	define refresh frame number when still image time
0xC8	02h	v	NOREF_NUM[7:0]	0	0	0	0	0	0	1	0	define no refresh frame number when still image time
0xCC	08h	v	POCSD_CTL[1:0]	-	0	0	-	-	-	-	-	SD offset cancel method selection
		v	SD_EQW[4:0]	-	-	-	0	1	0	0	0	source eq0/eq1 width adjsutmention
0xCD	5Ch	-	VPP_EN	0	-	-	-	-	-	-	-	Internal VPP enable
0xF9	5Dh	v	GOA_GAS	-	-	-	-	1	-	-	-	GOA output selection when GAS enable
		v	GOA_POWERON	-	-	-	-	-	1	-	-	CLR1/CLR2 output selection when power on
		v	GOA_POWEROFF	-	-	-	-	-	-	0	-	GOA output selection when power off
		v	FLC2B_SEL	-	-	-	-	-	-	-	1	FLC2B output selection
0XFB	01h	-	GRB	-	-	-	-	-	-	-	1	SPI registers reset
0xFC	82h	-	PRODUCTID1	0	0	0	0	0	0	0	0	PRODUCTID1 (82)
0xFD	79h	-	PRODUCTID2	0	0	0	0	0	0	0	0	PRODUCTID2(79)
0xFE	0Dh	-	PRODUCTID3	0	0	0	0	0	0	0	0	PRODUCTID3(0D)
0xFF	06h	-	CHIPID	0	0	0	0	0	1	1	0	IC version ID 01 for version A (READ only)

8.4.2 Register of page 1 (OTP & GOA MUX)

Addr[7:0]	Default[7:0]	OTP	Bit name	Data[7:0]								Description
				7	6	5	4	3	2	1	0	
0xB1	00h	-	OTP Group	-	-	0	0	0	0	0	0	OTP trimming group select. The group range is from group0 to group35
0xB2	5ah	-	OTP pwd	0	1	0	1	1	0	1	0	set to 0xA5 to enable 0xB3 command.
0xB3	00h	-	OTP_BURST_WR	0	-	-	-	-	-	-	-	auto OTP program mode write command
		-	OTP_re_Load	-	-	-	-	-	0	-	-	OTP auto re-load command.
		-	OTP_WR	-	-	-	-	-	-	-	0	OTP burst write command
0xB9	00h	-	DISABLE_OTP	-	-	0	0	-	-	-	-	00: M/S OTP enable 01: Master OTP enable Slave OTP disable 11: M/S OTP disable 10: Master OTP disable Slave OTP enable
0xBB	0	-	bust_write_index[7:0]	0	0	0	0	0	0	0	0	burst program Group index(group0~7)
0xBC	0	-	bust_write_index[15:8]	0	0	0	0	0	0	0	0	burst program Group index(group8~15)
0xBD	0	-	bust_write_index[23:16]	0	0	0	0	0	0	0	0	burst program Group index(group16~23)
0xBE	0	-	bust_write_index[31:24]	0	0	0	0	0	0	0	0	burst program Group index(group24~31)
0xBF	0	-	bust_write_index[35:31]	-	-	-	-	0	0	0	0	burst program Group index(groupu32~35)
GOA MUX												
0xC0	09h	v	GOUTL_1_STB	0	0	-	-	-	-	-	-	GOUTL_1 level in standby mode
		v	GOUTL_1_SEL[5:0]	-	-	0	0	1	0	0	1	Mux goa signal to GINL1 ref GOUT SEL mapping table
0xC1	09h	v	GOUTL_2_STB	0	0	-	-	-	-	-	-	GOUTL_2 level in standby mode
		v	GOUTL_2_SEL[5:0]	-	-	0	0	1	0	0	1	Mux goa signal to GINL2 ref GOUT SEL mapping table
0xC2	07h	v	GOUTL_3_STB	0	0	-	-	-	-	-	-	GOUTL_3 level in standby mode
		v	GOUTL_3_SEL[5:0]	-	-	0	0	0	1	1	1	Mux goa signal to GINL3 ref GOUT SEL mapping table
0xC3	07h	v	GOUTL_4_STB	0	0	-	-	-	-	-	-	GOUTL_4 level in standby mode
		v	GOUTL_4_SEL[5:0]	-	-	0	0	0	1	1	1	Mux goa signal to GINL4 ref GOUT SEL mapping table
0xC4	05h	v	GOUTL_5_STB	0	0	-	-	-	-	-	-	GOUTL_5 level in standby mode
		v	GOUTL_5_SEL[5:0]	-	-	0	0	0	1	0	1	Mux goa signal to GINL5 ref GOUT SEL mapping table
0xC5	05h	v	GOUTL_6_STB	0	0	-	-	-	-	-	-	GOUTL_6 level in standby mode
		v	GOUTL_6_SEL[5:0]	-	-	0	0	0	1	0	1	Mux goa signal to GINL6 ref GOUT SEL mapping table
0xC6	16h	v	GOUTL_7_STB	0	0	-	-	-	-	-	-	GOUTL_7 level in standby mode
		v	GOUTL_7_SEL[5:0]	-	-	0	1	0	1	1	0	Mux goa signal to GINL7 ref GOUT SEL mapping table
0xC7	16h	v	GOUTL_8_STB	0	0	-	-	-	-	-	-	GOUTL_8 level in standby mode
		v	GOUTL_8_SEL[5:0]	-	-	0	1	0	1	1	0	Mux goa signal to GINL8 ref GOUT SEL mapping table
0xC8	10h	v	GOUTL_9_STB	0	0	-	-	-	-	-	-	GOUTL_9 level in standby mode
		v	GOUTL_9_SEL[5:0]	-	-	0	1	0	0	0	0	Mux goa signal to GINL9 ref GOUT SEL mapping table
0xC9	10h	v	GOUTL_10_STB	0	0	-	-	-	-	-	-	GOUTL_10 level in standby mode
		v	GOUTL_10_SEL[5:0]	-	-	0	1	0	0	0	0	Mux goa signal to GINL10 ref GOUT SEL mapping table
0xCA	0Bh	v	GOUTL_11_STB	0	0	-	-	-	-	-	-	GOUTL_11 level in standby mode
		v	GOUTL_11_SEL[5:0]	-	-	0	0	1	0	1	1	Mux goa signal to GINL11 ref GOUT SEL mapping table
0xCB	0Bh	v	GOUTL_12_STB	0	0	-	-	-	-	-	-	GOUTL_12 level in standby mode
		v	GOUTL_12_SEL[5:0]	-	-	0	0	1	0	1	1	Mux goa signal to GINL12 ref GOUT SEL mapping table
0xCC	0Fh	v	GOUTL_13_STB	0	0	-	-	-	-	-	-	GOUTL_13 level in standby mode
		v	GOUTL_13_SEL[5:0]	-	-	0	0	1	1	1	1	Mux goa signal to GINL13 ref GOUT SEL mapping table
0xCD	0Fh	v	GOUTL_14_STB	0	0	-	-	-	-	-	-	GOUTL_14 level in standby mode
		v	GOUTL_14_SEL[5:0]	-	-	0	0	1	1	1	1	Mux goa signal to GINL14 ref GOUT SEL mapping table
0xCE	15h	v	GOUTL_15_STB	0	0	-	-	-	-	-	-	GOUTL_15 level in standby mode
		v	GOUTL_15_SEL[50]	-	-	0	1	0	1	0	1	Mux goa signal to GINL15 ref GOUT SEL mapping table
0xCF	15h	v	GOUTL_16_STB	0	0	-	-	-	-	-	-	GOUTL_16 level in standby mode
		v	GOUTL_16_SEL[5:0]	-	-	0	1	0	1	0	1	Mux goa signal to GINL16 ref GOUT SEL mapping table
0xD0	01h	v	GOUTL_17_STB	0	0	-	-	-	-	-	-	GOUTL_17 level in standby mode
		v	GOUTL_17_SEL[5:0]	-	-	0	0	0	0	0	1	Mux goa signal to GINL17 ref GOUT SEL mapping table
0xD1	01h	v	GOUTL_18_STB	0	0	-	-	-	-	-	-	GOUTL_18 level in standby mode
		v	GOUTL_18_SEL[5:0]	-	-	0	0	0	0	0	1	Mux goa signal to GINL18 ref GOUT SEL mapping table

0xD2	03h	v	GOUTL_19_STB	0	0	-	-	-	-	-	-	GOUTL_19 level in standby mode
		v	GOUTL_19_SEL[5:0]	-	-	0	0	0	0	1	1	Mux goa signal to GINL19 ref GOUT SEL mapping table
0xD3	03h	v	GOUTL_20_STB	0	0	-	-	-	-	-	-	GOUTL_20 level in standby mode
		v	GOUTL_20_SEL[5:0]	-	-	0	0	0	0	1	1	Mux goa signal to GINL20 ref GOUT SEL mapping table
0xD4	0Ah	v	GOUTR_1_STB	0	0	-	-	-	-	-	-	GOUTR_1 level in standby mode
		v	GOUTR_1_SEL[5:0]	-	-	0	0	1	0	1	0	Mux goa signal to GINR1 ref GOUT SEL mapping table
0xD5	0Ah	v	GOUTR_2_STB	0	0	-	-	-	-	-	-	GOUTR_2 level in standby mode
		v	GOUTR_2_SEL[5:0]	-	-	0	0	1	0	1	0	Mux goa signal to GINR2 ref GOUT SEL mapping table
0xD6	08h	v	GOUTR_3_STB	0	0	-	-	-	-	-	-	GOUTR_3 level in standby mode
		v	GOUTR_3_SEL[5:0]	-	-	0	0	1	0	0	0	Mux goa signal to GINR3 ref GOUT SEL mapping table
0xD7	08h	v	GOUTR_4_STB	0	0	-	-	-	-	-	-	GOUTR_4 level in standby mode
		v	GOUTR_4_SEL[5:0]	-	-	0	0	1	0	0	0	Mux goa signal to GINR4 ref GOUT SEL mapping table
0xD8	06h	v	GOUTR_5_STB	0	0	-	-	-	-	-	-	GOUTR_5 level in standby mode
		v	GOUTR_5_SEL[5:0]	-	-	0	0	0	1	1	0	Mux goa signal to GINR5 ref GOUT SEL mapping table
0xD9	06h	v	GOUTR_6_STB	0	0	-	-	-	-	-	-	GOUTR_6 level in standby mode
		v	GOUTR_6_SEL[5:0]	-	-	0	0	0	1	1	0	Mux goa signal to GINR6 ref GOUT SEL mapping table
0xDA	16h	v	GOUTR_7_STB	0	0	-	-	-	-	-	-	GOUTR_7 level in standby mode
		v	GOUTR_7_SEL[5:0]	-	-	0	1	0	1	1	0	Mux goa signal to GINR7 ref GOUT SEL mapping table
0xDB	16h	v	GOUTR_8_STB	0	0	-	-	-	-	-	-	GOUTR_8 level in standby mode
		v	GOUTR_8_SEL[5:0]	-	-	0	1	0	1	1	0	Mux goa signal to GINR8 ref GOUT SEL mapping table
0xDC	10h	v	GOUTR_9_STB	0	0	-	-	-	-	-	-	GOUTR_9 level in standby mode
		v	GOUTR_9_SEL[5:0]	-	-	0	1	0	0	0	0	Mux goa signal to GINR9 ref GOUT SEL mapping table
0xDD	10h	v	GOUTR_10_STB	0	0	-	-	-	-	-	-	GOUTR_10 level in standby mode
		v	GOUTR_10_SEL[5:0]	-	-	0	1	0	0	0	0	Mux goa signal to GINR10 ref GOUT SEL mapping table
0xDE	0Ch	v	GOUTR_11_STB	0	0	-	-	-	-	-	-	GOUTR_11 level in standby mode
		v	GOUTR_11_SEL[5:0]	-	-	0	0	1	1	0	0	Mux goa signal to GINR11 ref GOUT SEL mapping table
0xDF	0Ch	v	GOUTR_12_STB	0	0	-	-	-	-	-	-	GOUTR_12 level in standby mode
		v	GOUTR_12_SEL[5:0]	-	-	0	0	1	1	0	0	Mux goa signal to GINR12 ref GOUT SEL mapping table
0xE0	0Fh	v	GOUTR_13_STB	0	0	-	-	-	-	-	-	GOUTR_13 level in standby mode
		v	GOUTR_13_SEL[5:0]	-	-	0	0	1	1	1	1	Mux goa signal to GINR13 ref GOUT SEL mapping table
0xE1	0Fh	v	GOUTR_14_STB	0	0	-	-	-	-	-	-	GOUTR_14 level in standby mode
		v	GOUTR_14_SEL[5:0]	-	-	0	0	1	1	1	1	Mux goa signal to GINR14 ref GOUT SEL mapping table
0xE2	15h	v	GOUTR_15_STB	0	0	-	-	-	-	-	-	GOUTR_15 level in standby mode
		v	GOUTR_15_SEL[5:0]	-	-	0	1	0	1	0	1	Mux goa signal to GINR15 ref GOUT SEL mapping table
0xE3	15h	v	GOUTR_16_STB	0	0	-	-	-	-	-	-	GOUTR_16 level in standby mode
		v	GOUTR_16_SEL[5:0]	-	-	0	1	0	1	0	1	Mux goa signal to GINR16 ref GOUT SEL mapping table
0xE4	02h	v	GOUTR_17_STB	0	0	-	-	-	-	-	-	GOUTR_17 level in standby mode
		v	GOUTR_17_SEL[5:0]	-	-	0	0	0	0	1	0	Mux goa signal to GINR17 ref GOUT SEL mapping table
0xE5	02h	v	GOUTR_18_STB	0	0	-	-	-	-	-	-	GOUTR_18 level in standby mode
		v	GOUTR_18_SEL[5:0]	-	-	0	0	0	0	1	0	Mux goa signal to GINR18 ref GOUT SEL mapping table
0xE6	04h	v	GOUTR_19_STB	0	0	-	-	-	-	-	-	GOUTR_19 level in standby mode
		v	GOUTR_19_SEL[5:0]	-	-	0	0	0	1	0	0	Mux goa signal to GINR19 ref GOUT SEL mapping table
0xE7	04h	v	GOUTR_20_STB	0	0	-	-	-	-	-	-	GOUTR_20 level in standby mode
		v	GOUTR_20_SEL[5:0]	-	-	0	0	0	1	0	0	Mux goa signal to GINR20 ref GOUT SEL mapping table

8.4.3 Register of page 2 (analog gamma)

Addr[7:0]	Default[7:0]	OTP	Bit name	Data[7:0]								Description
				7	6	5	4	3	2	1	0	
0xC0	00h	v	T_PVP0[2:0]	-	-	-	-	-	0	0	0	V0 positive gamma op's input voltage.
0xC1	07h	v	T_PVP1[5:0]	-	-	0	0	0	1	1	1	V4 positive gamma op's input voltage.
0xC2	10h	v	T_PVP2[5:0]	-	-	0	1	0	0	0	0	V8 positive gamma op's input voltage.
0xC3	1Fh	v	T_PVP3[5:0]	-	-	0	1	1	1	1	1	V16 positive gamma op's input voltage.
0xC4	1Fh	v	T_PVP4[5:0]	-	-	0	1	1	1	1	1	V28 positive gamma op's input voltage.
0xC5	1Fh	v	T_PVP5[5:0]	-	-	0	1	1	1	1	1	V40 positive gamma op's input voltage.
0xC6	1Fh	v	T_PVP6[5:0]	-	-	0	1	1	1	1	1	V56 positive gamma op's input voltage.
0xC7	1Fh	v	T_PVP7[5:0]	-	-	0	1	1	1	1	1	V80 positive gamma op's input voltage.
0xC8	1Fh	v	T_PVP8[5:0]	-	-	0	1	1	1	1	1	V128 positive gamma op's input voltage.
0xC9	1Fh	v	T_PVP9[5:0]	-	-	0	1	1	1	1	1	V176 positive gamma op's input voltage.
0xCA	1Fh	v	T_PVP10[5:0]	-	-	0	1	1	1	1	1	V200 positive gamma op's input voltage.
0xCB	1Fh	v	T_PVP11[5:0]	-	-	0	1	1	1	1	1	V216 positive gamma op's input voltage.
0xCC	1Fh	v	T_PVP12[5:0]	-	-	0	1	1	1	1	1	V228 positive gamma op's input voltage.
0xCD	1Fh	v	T_PVP13[5:0]	-	-	0	1	1	1	1	1	V240 positive gamma op's input voltage.
0XCE	1Fh	v	T_PVP14[5:0]	-	-	0	1	1	1	1	1	V248 positive gamma op's input voltage.
0xCF	20h	v	T_PVP15[5:0]	-	-	1	0	0	0	0	0	V252 positive gamma op's input voltage.
0xD0	07h	v	T_PVP16[2:0]	-	-	-	-	-	1	1	1	V255 positive gamma op's input voltage.
0xD2	00h	v	T_PVN0[2:0]	-	-	-	-	-	0	0	0	V0 negative gamma op's input voltage.
0xD3	07h	v	T_PVN1[5:0]	-	-	0	0	0	1	1	1	V4 negative gamma op's input voltage.
0xD4	10h	v	T_PVN2[5:0]	-	-	0	1	0	0	0	0	V8 negative gamma op's input voltage.
0xD5	1Fh	v	T_PVN3[5:0]	-	-	0	1	1	1	1	1	V16 negative gamma op's input voltage.
0xD6	1Fh	v	T_PVN4[5:0]	-	-	0	1	1	1	1	1	V28 negative gamma op's input voltage.
0xD7	1Fh	v	T_PVN5[5:0]	-	-	0	1	1	1	1	1	V40 negative gamma op's input voltage.
0xD8	1Fh	v	T_PVN6[5:0]	-	-	0	1	1	1	1	1	V56 negative gamma op's input voltage.
0xD9	1Fh	v	T_PVN7[5:0]	-	-	0	1	1	1	1	1	V80 negative gamma op's input voltage.
0xDA	1Fh	v	T_PVN8[5:0]	-	-	0	1	1	1	1	1	V128 negative gamma op's input voltage.
0xDB	1Fh	v	T_PVN9[5:0]	-	-	0	1	1	1	1	1	V176 negative gamma op's input voltage.
0xDC	1Fh	v	T_PVN10[5:0]	-	-	0	1	1	1	1	1	V200 negative gamma op's input voltage.
0xDD	1Fh	v	T_PVN11[5:0]	-	-	0	1	1	1	1	1	V216 negative gamma op's input voltage.
0xDE	1Fh	v	T_PVN12[5:0]	-	-	0	1	1	1	1	1	V228 negative gamma op's input voltage.
0xDF	1Fh	v	T_PVN13[5:0]	-	-	0	1	1	1	1	1	V240 negative gamma op's input voltage.
0xE0	1Fh	v	T_PVN14[5:0]	-	-	0	1	1	1	1	1	V248 negative gamma op's input voltage.
0xE1	20h	v	T_PVN15[5:0]	-	-	1	0	0	0	0	0	V252 negative gamma op's input voltage.
0xE2	07h	v	T_PVN16[2:0]	-	-	-	-	-	1	1	1	V255 negative gamma op's input voltage.

8.4.4 Register of page 3 (GOA)

MIPI Addr[7:0]	Default[7:0]	OTP	Bit name	Data[7:0]								Description
				7	6	5	4	3	2	1	0	
0xB9	00	-	Reserved	0	-	-	-	-	-	-	-	Reserved
		v	FLC_SEL	-	0	-	-	-	-	-	-	FLC output selection
		-	Reserved	-	-	0	0	0	0	0	0	Reserved
0xBB	00h	-	Reserved	0	0	0	0	0	-	-	-	Reserved
		v	STV_PREC[3:0]	-	-	-	-	-	0	0	0	STV pre-charge width adjustment
0xBC	00h	v	CKV_FALL_PREC[7:0]	0	0	0	0	0	0	0	0	CKV falling pre-charge width adjustment.
0xBE	01h	-	Reserved	0	0	-	-	-	-	-	-	Reserved
		v	GOA_UD	-	-	0	-	-	-	-	-	GOA scan direction selection
		-	Reserved	-	-	-	0	-	-	-	-	Reserved
		v	CKV_BLANKON	-	-	-	-	0	-	-	-	Blanking all on enable.
		v	GOA_PHASE[2:0]	-	-	-	-	-	0	0	1	GOA phase selection.
0xBF	10h	-	Reserved	0	0	-	-	-	-	-	-	Reserved
		v	GOA_Tn_FACTOR	-	-	0	1	-	-	-	-	GOA Timing (T0~T5) adjustment factor selection.
		-	Reserved	-	-	-	-	0	0	0	0	Reserved
0xC2	00h	v	GOA_T0[7:0]	0	0	0	0	0	0	0	0	Odd STV falling position adjustment.
0xC3	3Ah	v	GOA_T1[7:0]	0	0	0	0	0	0	0	1	Odd STV rising position adjustment.
0xC4	00h	v	GOA_T2[7:0]	0	0	0	0	0	0	0	0	Odd CKV falling position adjustment.
0xC5	2Ch	v	GOA_T3[7:0]	0	0	1	0	1	1	0	0	Odd CKV rising position adjustment.
0xC6	00h	v	GOA_T4[7:0]	0	0	0	0	0	0	0	0	Odd GCK falling position adjustment.
0xC7	01h	v	GOA_T5[7:0]	0	0	0	0	0	0	0	1	Odd GCK rising position adjustment.
0xC8	0Dh	-	Reserved	0	0	0	-	-	-	-	-	Reserved
		v	STV_LEAD[4:0]	-	-	-	0	0	1	0	1	GOA STV leads time setting.
0xC9	0Bh	v	Reserved	0	0	0	-	-	-	-	-	Reserved
		v	CKV_LEAD[4:0]	-	-	-	0	0	0	1	1	GOA CKV leads time setting.
0xCA	42h	v	CKV_NONOVERLAP	0	-	-	-	-	-	-	-	CKV non-overlap control
		-	Reserved	-	1	-	-	-	-	-	-	Reserved
		v	CKV_DUMMY[5:0]	-	-	0	0	0	0	1	0	GOA CKV dummy number in V-blanking
0xCB	00h	v	CKV_RISE_PREC[7:0]	0	0	0	0	0	0	0	0	CKV rising pre-charge width adjustment.
0xCC	44h	v	STV_WIDTH[3:0]	0	1	0	0	-	-	-	-	GOA STV width setting.
		v	CKV_WIDTH[3:0]	-	-	-	-	0	1	0	0	GOA CKV width setting.
0xCD	07h	v	GOA_FLC[7:0]	0	0	0	0	0	1	1	1	GOA FLC toggle frame setting.
0xCE	03h	-	Reserved	0	-	-	-	-	-	-	-	Reserved
		v	GOA_FLCA_LEAD[6:0]	-	0	0	0	0	0	1	1	FLCA lead 1st DE toggle number.
0xCF	68h	v	FLC_sync	0	-	-	-	-	-	-	-	FLC sync selection
		-	Reserved	-	0	0	0	-	-	-	-	Reserved
		v	CLR_adjsel	-	-	-	-	1	-	-	-	CLR adjustment selection
		v	CLR_WD[10:8]	-	-	-	-	-	0	0	0	CLR width adjustment
0xD0	05h	v	CKV_BLANK_SHIFT[7:0]	0	0	0	0	0	1	0	1	Blank CKV shift from the last DE.
0xD1	06h	v	CKV_BLANK_WIDTH[7:0]	0	0	0	0	0	1	1	0	Blank CKV width adjustment.
0xD2	06h	v	CLR1_WD[7:0]	0	0	0	0	0	1	1	0	GOA CLR1 width adjustment
0xD3	06h	v	CLR234_WD[7:0]	0	0	0	0	0	1	1	0	GOA CLR2/3/4 width adjustment
0xD4	88h	v	CLR1_POL	1	-	-	-	-	-	-	-	CLR1 polarity setting.
		v	CLR1_START[6:0]	-	0	0	0	1	0	0	0	CLR1 start position.
0xD5	09h	v	CLR2_POL	0	-	-	-	-	-	-	-	CLR2 polarity setting.
		v	CLR2_START[6:0]	-	0	0	0	1	0	0	1	CLR2 start position.
0xD6	88h	v	CLR3_POL	1	-	-	-	-	-	-	-	CLR3 polarity setting.
		v	CLR3_START[6:0]	-	0	0	0	1	0	1	1	CLR3 start position.
0xD7	08h	v	CLR4_POL	0	-	-	-	-	-	-	-	CLR4 polarity setting.
		v	CLR4_START[6:0]	-	0	0	0	1	0	0	0	CLR4 start position.
0xD8	00h	v	CLR2/3/4_START_MSB[3:0]	0	0	0	0	-	-	-	-	MSB[10:7] of CLR2/3/4 start position.
		v	CLR1_START_MSB[3:0]	-	-	-	-	0	0	0	0	MSB[10:7] of CLR1 start position.
0xD9	00h	-	Reserved	0	0	0	0	0	-	-	-	Reserved
		v	CLR4_LEAD	-	-	-	-	-	0	-	-	GOA CLR4 offset direction setting.
		v	CLR3_LEAD	-	-	-	-	-	-	0	-	GOA CLR3 offset direction setting.

		v	CLR2_LEAD	-	-	-	-	-	-	-	0	GOA CLR2 offset direction setting.
0xDB	00h	-	Reserved	0	0	0	0	0	-	-	-	Reserved
		v	FLC_NONOVLAP[1:0]	-	-	-	-	-	0	0	-	FLC overlap setting.
		v	CLR1_LEAD	-	-	-	-	-	-	-	0	GOA CLR1 offset direction setting.
0xDD	01h	v	GOA_T2B[7:0]	0	0	0	0	0	0	0	1	Tune even CKV falling time.
0xDE	2Ch	v	GOA_T3B[7:0]	0	0	1	0	1	1	0	0	Tune even CKV rising time.
0xE6	00h	v	GOA_T0B[7:0]	0	0	0	0	0	0	0	0	Tune even STV falling time.
0xE7	3Ah	v	GOA_T1B[7:0]	0	0	0	0	0	0	0	0	Tune even STV rising time.

8.4.5 Register of page 5 (MIPI)

Address (M) is for master, Address(S) is for slave, Address (M/S) is for master and slave

Addr[7:0]	Default[7:0]	OTP	Bit name	Data[7:0]								Description
				7	6	5	4	3	2	1	0	
0xB1(M/S)	E5h	v	Reserved	1	1	1	0	-	-	-	-	Reserved
		v	R_EoTpEN	-	-	-	-	0	-	-	-	Decode EoTp packet enable
		v	Reserved	-	-	-	-	-	1	0	1	Reserved
0xB3(M/S)	32h	v	Ths_settle	0	0	1	-	-	-	-	-	Ths_settle adjustment
		v	Lhs_settle	-	-	-	1	-	-	-	-	Ths_settle time latch by OSC25 edge selection.
		v	T_TLPX	-	-	-	-	0	0	1	0	TLPX time of BTA adjustment
0xC0(M) 0xD9(S)	05h	v	TR_EN[7:6]	0	0	-	-	-	-	-	-	Terminal resistor enable
		v	TRC_VAL[2:0]	-	-	-	-	-	1	0	1	Terminal resistor of CLK lane value adjustment
0xC2(M) 0xDB(S)	15h	v	Reserved	-	0	0	1	-	-	-	-	Reserved
		v	TRD_VAL[2:0]	-	-	-	-	-	1	0	1	Terminal resistor of data lane value adjustment
0xC5(M/S)	18h	v	TUNEC	-	0	0	1	-	-	-	-	CLK lane skew adjustment
		v	Reserved	-	-	-	-	1	-	-	-	Reserved
0xC6(M) 0xDC(S)	00h	v	TUNED1	-	0	0	0	-	-	-	-	Data lane1 skew adjustment
		v	TUNED0	-	-	-	-	-	0	0	0	Data lane0 skew adjustment
0xC7(M) 0xDD(S)	00h	v	TUNED3	-	0	0	0	-	-	-	-	Data lane3 skew adjustment
		v	TUNED2	-	-	-	-	-	0	0	0	Data lane2 skew adjustment

8.4.6 Register of page 6 (Engineer)

Addr[7:0]	Default[7:0]	OTP	Bit name	Data[7:0]								Description
				7	6	5	4	3	2	1	0	
0xB8	5Ah	-	Engineer_PWD	0	1	0	1	1	0	1	0	Engineer_PWD=A5h to enable engineer register
0xBC	00h	v	POCGM_CTL	-	0	0	0	-	-	-	-	Gamma chopper control
		v	POCGMD_CTL	-	-	-	-	-	0	0	0	Gamma buffer chopper control
0xC0	5Ah	-	Function_EN	0	1	0	1	0	1	0	1	Function_EN=A5h to enable in-house function
0xC7	0Ah	v	VCCIFS	-	-	-	-	1	0	-	-	VCCIF adjustment.
		v	VCCS	-	-	-	-	-	-	1	0	VCC adjustment
0xD5	26h	v	GOE_WD	0	1	0	0	0	1	1	0	Source delay time adjustment(CKV falling to Source off)

8.4.7 Register of digital gamma

Page 7/10: Red positive/negative gamma
Page 8/11: Green positive/negative gamma
Page 9/12: Blue positive/negative gamma

Page 7/8/9/10/11/12 register table

Addr[7:0]	Default[7:0]	OTP	Bit name	Data[7:0]								Description
				7	6	5	4	3	2	1	0	
0xB1	00h	v	DGMA1[7:0]	0	0	0	0	0	0	0	0	Digital gamma V0 Reference
0xB2	04h	v	DGMA2[7:0]	0	0	0	0	0	1	0	0	Digital gamma V1 Reference
0xB3	0Ch	v	DGMA3[7:0]	0	0	0	0	1	1	0	0	Digital gamma V3 Reference
0xB4	1Ch	v	DGMA4[7:0]	0	0	0	1	1	1	0	0	Digital gamma V7 Reference
0xB5	2Ch	v	DGMA5[7:0]	0	0	1	0	1	1	0	0	Digital gamma V11 Reference
0xB6	3Ch	v	DGMA6[7:0]	0	0	1	1	1	1	0	0	Digital gamma V15 Reference
0xB7	5Ch	v	DGMA7[7:0]	0	1	0	1	1	1	0	0	Digital gamma V23 Reference
0xB8	7Ch	v	DGMA8[7:0]	0	1	1	1	1	1	0	0	Digital gamma V31 Reference
0xB9	BCh	v	DGMA9[7:0]	1	0	1	1	1	1	0	0	Digital gamma V47 Reference
0xBA	FCh	v	DGMA10[7:0]	1	1	1	1	1	1	0	0	Digital gamma V63 Reference
0xBB	7Ch	v	DGMA11[7:0]	0	1	1	1	1	1	0	0	Digital gamma V95 Reference
0xBC	FCh	v	DGMA12[7:0]	1	1	1	1	1	1	0	0	Digital gamma V127 Reference
0xBD	00h	v	DGMA13[7:0]	0	0	0	0	0	0	0	0	Digital gamma V128 Reference
0xBE	80h	v	DGMA14[7:0]	1	0	0	0	0	0	0	0	Digital gamma V160 Reference
0xBF	00h	v	DGMA15[7:0]	0	0	0	0	0	0	0	0	Digital gamma V192 Reference
0xC0	40h	v	DGMA16[7:0]	0	1	0	0	0	0	0	0	Digital gamma V208 Reference
0xC1	80h	v	DGMA17[7:0]	1	0	0	0	0	0	0	0	Digital gamma V224 Reference
0xC2	A0h	v	DGMA18[7:0]	1	0	1	0	0	0	0	0	Digital gamma V232 Reference
0xC3	C0h	v	DGMA19[7:0]	1	1	0	0	0	0	0	0	Digital gamma V240 Reference
0xC4	D0h	v	DGMA20[7:0]	1	1	0	1	0	0	0	0	Digital gamma V244 Reference
0xC5	E0h	v	DGMA21[7:0]	1	1	1	0	0	0	0	0	Digital gamma V248 Reference
0xC6	F0h	v	DGMA22[7:0]	1	1	1	1	0	0	0	0	Digital gamma V252 Reference
0xC7	F8h	v	DGMA23[7:0]	1	1	1	1	1	0	0	0	Digital gamma V254 Reference
0xC8	FCh	v	DGMA24[7:0]	1	1	1	1	1	1	0	0	Digital gamma V255 Reference
0xC9	00h	v	DGMA1[9:8]	0	0	-	-	-	-	-	-	Digital gamma V0 Reference
		v	DGMA2[9:8]	-	-	0	0	-	-	-	-	Digital gamma V1 Reference
		v	DGMA3[9:8]	-	-	-	-	0	0	-	-	Digital gamma V3 Reference
		v	DGMA4[9:8]	-	-	-	-	-	-	0	0	Digital gamma V7 Reference
0xCA	00h	v	DGMA5[9:8]	0	0	-	-	-	-	-	-	Digital gamma V11 Reference
		v	DGMA6[9:8]	-	-	0	0	-	-	-	-	Digital gamma V15 Reference
		v	DGMA7[9:8]	-	-	-	-	0	0	-	-	Digital gamma V23 Reference
		v	DGMA8[9:8]	-	-	-	-	-	-	0	0	Digital gamma V31 Reference
0xCB	05h	v	DGMA9[9:8]	0	0	-	-	-	-	-	-	Digital gamma V47 Reference
		v	DGMA10[9:8]	-	-	0	0	-	-	-	-	Digital gamma V63 Reference
		v	DGMA11[9:8]	-	-	-	-	0	1	-	-	Digital gamma V95 Reference
		v	DGMA12[9:8]	-	-	-	-	-	-	0	1	Digital gamma V127 Reference
0xCC	AFh	v	DGMA13[9:8]	1	0	-	-	-	-	-	-	Digital gamma V128 Reference
		v	DGMA14[9:8]	-	-	1	0	-	-	-	-	Digital gamma V160 Reference

		v	DGMA15[9:8]	-	-	-	-	1	1	-	-	Digital gamma V192 Reference
		v	DGMA16[9:8]	-	-	-	-	-	-	1	1	Digital gamma V208 Reference
0xCD	FFh	v	DGMA17[9:8]	1	1	-	-	-	-	-	-	Digital gamma V224 Reference
		v	DGMA18[9:8]	-	-	1	1	-	-	-	-	Digital gamma V232 Reference
		v	DGMA19[9:8]	-	-	-	-	1	1	-	-	Digital gamma V240 Reference
		v	DGMA20[9:8]	-	-	-	-	-	-	1	1	Digital gamma V244 Reference
0xCE	FFh	v	DGMA21[9:8]	1	1	-	-	-	-	-	-	Digital gamma V248 Reference
		v	DGMA22[9:8]	-	-	1	1	-	-	-	-	Digital gamma V252 Reference
		v	DGMA23[9:8]	-	-	-	-	1	1	-	-	Digital gamma V254 Reference
		v	DGMA24[9:8]	-	-	-	-	-	-	1	1	Digital gamma V255 Reference

9. Register Description

9.1 Register of page 0

Address [7:0]	Data [7:0] (Default) 7	6	5	4	3	2	1	0	Name	Description	OTP
0xB1	0	0	0	0	0	0	0	0	VENDER_ID[6:0]	The register is defines vender id for customer.	v
0xB2	-	-	-	-	-	-	-	0	BISTB	TCON BIST mode control.	v
	-	-	-	-	-	-	0	-	NBW	Normal Black and Normal white panel selection.	v
	-	-	-	-	-	0	-	-	ZTYPE	When zigzag function is enabled that selection type of Zigzag.	v
	-	-	-	-	0	-	-	-	ZIGZAG	Panel driving method selection.	v
	-	-	-	0	-	-	-	-	LR	Horizontal direction control. MIPI DCS 0x36 set_address_mode [2] command and SPI register do XOR operation.	v
	-	-	0	-	-	-	-	-	UPDNB	Vertical direction control. MIPI DCS 0x36 set_address_mode [1] command and SPI register do XOR operation.	v
	-	1	-	-	-	-	-	-	SLEEP	TCON sleep mode control. MIPI DCS 0x10 enter_sleep_mode is sleep mode, and 0x11 exit_sleep_mode is normal mode. MIPI DCS command does AND with SPI register.	v

Combination Logic	Truth table PIN/MIPI	REG	To TCON	To TCON
BIST_EN (pin), BISTB (reg) → XOR → To TCON BIST	0	0	0	0: BIST mode. 1: Normal mode.
	0	1	1	
	1	0	1	
	1	1	0	
NBW (pin), NBW (reg) → XOR → To TCON NBW	0	0	0	0: Normal white panel. 1: Normal black panel.
	0	1	1	
	1	0	1	
	1	1	0	
ZTYPE (pin), ZTYPE (reg) → XOR → To TCON ZTYPE	0	0	0	0: Zigzag type 0 1: Zigzag type 1
	0	1	1	
	1	0	1	
	1	1	0	
ZIGZAG (pin), ZIGZAG (reg) → XOR → To TCON ZIGZAG	0	0	0	0: Stripe driving method. 1: Zigzag driving method.
	0	1	1	
	1	0	1	
	1	1	0	
MIPI DCS 0x36[6], LR (SPI) → XOR → To TCON LR	0	0	0	0: Left to right. 1: Right to left.
	0	1	1	
	1	0	1	
	1	1	0	
MIPI DCS 0x36[7], UPDNB (SPI) → XOR → To TCON UPDNB	0	0	0	0: Bottom to top. 1: Top to Bottom.
	0	1	1	
	1	0	1	
	1	1	0	
MIPI DCS 0x10,0x11, Sleep (SPI) → AND → To TCON Sleep	0 **(0x10)**	0	0	0: Sleep mode. 1: Normal mode.
	0 **(0x10)**	1	0	
	1 **(0x11)**	0	0	
	1 **(0x11)**	1	1	

Table 9.1: TCON configuration 1-truth table

Address [7:0]	Data [7:0] (Default) 7	6	5	4	3	2	1	0	Name	Description	OTP
0xB3	-	-	-	-	-	-	0	0	RES[1:0]	Resolution selection	v
	-	-	-	-	-	0	-	-	LED_EN	LEDON pin output control. 0:disable 1: enable	v
	-	-	-	-	1	-	-	-	VRES_FIX	Display vertical line decides by RES [1:0] or VRES [7:0]. This function is for TEST. 0: Vertical line decides by VRES [7:0].(page0 0xB4) 1: Vertical line decides by RES [1:0].(page0 0xB3	v
	-	-	-	0	-	-	-	-	PWRMD	Power mode control. 0: internal VGH/VGL 1:external VGH/VGL	v
	-	0	0	-	-	-	-	-	LPM_CTRL	LPM mode control. 00:normal mode 01:LPM01 mode MIPI TX manu control display frame rate 1x:LPM10 mode driver auto detect still image and control display frame rate by register(page0 0xC6,0xC7,0xC8)	v
	0	-	-	-	-	-	-	-	DISP_ON	MIPI DCS 0x29 displays on and DCS 0x28 display off command. This DCS command does XOR with SPI.	v

Combination Logic	Truth table PIN/MIPI	REG	To TCON	To TCON
RES0 (pin), RES0 (reg) → XOR → To TCON RES0	0	0	0	00b:1200RGBx1600 01b:108RGBx1920 10b: 600RGBx1024 11b: 1200RGBx1920
	0	1	1	
	1	0	1	
	1	1	0	
RES1 (pin), RES1 (reg) → XOR → To TCON RES1	0	0	0	
	0	1	1	
	1	0	1	
	1	1	0	
LED_EN (pin), LED_EN (reg) → XOR → To TCON LED_EN	0	0	0	0:LEDON pin output disable 1:LEDON pin output enable.
	0	1	1	
	1	0	1	
	1	1	0	
PWRMD (pin), PWRMD (reg) → XOR → To TCON PWRMD	0	0	0	0:Internal VGH/VGL 1:External VGH/VGL
	0	1	1	
	1	0	1	
	1	1	0	
MIPI DCS 0x28, 0x29, DISP_ON (SPI) → XOR → To TCON DISP	0 **(0x28)**	0	0	0: Display off. 1: Display on.
	0 **(0x28)**	1	1	
	1 **(0x29)**	0	1	
	1 **(0x29)**	1	0	

Table 9.2: TCON configuration 2-truth table

Address [7:0]	Data [7:0] (Default) 7	6	5	4	3	2	1	0	Name	Description	OTP
0xB4	1	1	0	0	0	0	0	0	VRES[7:0]	When VRES_FIX is set enable, the vertical display line decide by this register. The VRES range is 80 ~ 255 and step is 8H. The max vertical display line must be less than V-display. e.g. RES[1:0] is set 1200RGBx1920, VRES[7:0] < 0xF0	v
0xB5	0	0	0	0	0	0	0	0	ZDATA[7:0]	Zigzag panel dummy data set. When Zigzag driving method is enable. This data will be dummy line of source output.	v
0xB6	-	-	-	-	-	-	-	0	D_GAM_EN	Digital gamma function enables. 0: Disable. 1: Enable.	v
	-	-	-	-	-	-	0	-	DITHER_EN	Dithering function enables. If D_GAM_EN set to disable, the dithering function will be disable even set enable. 0: Disable. 1: Enable.	v
	-	-	-	-	0	0	-	-	CABC_CTRL[1:0]	CABC mode selection. 00b:Bypass mode. 01b:UI mode. 10b:Still mode 11b: Moving mode.	v
	-	-	0	-	-	-	-	-	RP2EN	2nd repair OP enable/disable control(XOR pin) 0: Disable. 1: Enable.	v
	-	0	-	-	-	-	-	-	RP1EN	1st repair OP enalbe/disable control(XOR pin) 0: Disable. 1: Enable.	v
0xB7	-	-	-	-	-	-	-	0	PCLK_SEL	TCON PCLK source path selection. 0: From OSC IP. 1:From EXT_CLK.	v
	-	-	-	-	-	0	0	-	OVERLAP[1:0]	Overlap select for MIPI RL type mode. 0: no pixel overlap 1: 2 pixel overlap 2: 4 pixel overlap 3: reserve	v
0xB8	-	-	-	-	-	-	0	0	MIPI_LAN	MIPI lane number selection(XOR pin MIPI_LAN) 00: reserve 01: 2 lans 10: reserve 11: 4 lans	v
	-	-	-	-	0	0	-	-	LNSW	MIPI lane swap(XOR pin LNSW) Please see chapter 4.4.	v
	-	-	-	0	-	-	-	-	MIPI_TYPE	MIPI mode selection(XOR pin MIPI_TYPE) 0: multi drop mode 1: RL mode	v
	-	-	0	-	-	-	-	-	PNSW	MIPI pin polarity swap(XOR pin PNSW) 0: P/N not swap 1: P/N swap	v
	0	-	-	-	-	-	-	-	GOA_EN	GOA on/off control(XOR pin GOA_EN) 0: GOA off 1: GOA on	v
0xBA	-	-	-	-	-	-	1	1	INV_SEL[1:0]	POL inversion selection. This function isn't support in BIST mode and Free mode.For ZIGZAG panel only has column inversion. For strip panel 00b: 1line 1dot inversion. 01b: 1+2line 1dot inversion. 10b: 2line 1dot inversion. 11b: Column inversion.	v
	-	-	-	-	1	1	-	-	SD_ISEL[1:0]	Source bias selection. 00:83% 01:125% 10:167% 11:100%	v
	-	-	-	0	-	-	-	-	INV_SEL2	INV_SEL[1 :0]=01 selection 0: 1+2line 1dot inversion 1: 4line 1dot inversion	v
	-	-	0	-	-	-	-	-	BLREVONOFF	Source output at power on/off 0: Hi-z. 1: GND.	v
	1	0	-	-	-	-	-	-	BLREV[1:0]	Source output selection at V-blanking. 00b: Keep output the last line. 01b: Hi-z. 1xb: GND.	v

<table>
<tr><th rowspan="2">Address [7:0]</th><th colspan="8">Data [7:0] (Default)</th><th rowspan="2">Name</th><th rowspan="2">Description</th><th rowspan="2">OTP</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0xBD</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>T_VCOMS[7:0]</td><td>VCOM voltage selection.
VCOM=-0.2-0.01xT_VCOMS[7:0].
<table><tr><th>T_VCOMS[7:0]</th><th>Output VCOM(V)</th></tr><tr><td>0x00</td><td>-0.20</td></tr><tr><td>0x01</td><td>-0.21</td></tr><tr><td>0x02</td><td>-0.22</td></tr><tr><td>0x03</td><td>-0.23</td></tr><tr><td colspan="2">:</td></tr><tr><td>0x7F</td><td>-1.47</td></tr><tr><td>0x80</td><td>-1.48</td></tr><tr><td>0x81</td><td>-1.49</td></tr><tr><td colspan="2">:</td></tr><tr><td>0xFD</td><td>-2.73</td></tr><tr><td>0xFE</td><td>-2.74</td></tr><tr><td>0xFF</td><td>-2.75</td></tr></table></td><td>v</td></tr>
<tr><td>0xBE</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>LPM_VCOMS[7:0]</td><td>VCOM voltage selection in LPM mode. Range refer to T_VCOMS table</td><td>v</td></tr>
<tr><td>0xBF</td><td>-</td><td>-</td><td>-</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>VGHS[4:0]</td><td>VGH voltage selection. Range is from 8.7V to 18V. Step=0.3V. (Default=16.2V)
<table><tr><th>VGHS[4:0]</th><th>Output VGH(V)</th></tr><tr><td>0</td><td>8.7</td></tr><tr><td>1</td><td>9.0</td></tr><tr><td>2</td><td>9.3</td></tr><tr><td>3</td><td>9.6</td></tr><tr><td colspan="2">:</td></tr><tr><td>29</td><td>17.4</td></tr><tr><td>30</td><td>17.7</td></tr><tr><td>31</td><td>18.0</td></tr></table></td><td>v</td></tr>
<tr><td>0xC0</td><td>-</td><td>-</td><td>-</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>VGLS[4:0]</td><td>VGL voltage selection. Range is from -6.7V to -16V. Step=0.3V. (Default=-11.5V)
<table><tr><th>VGLS[4:0]</th><th>Output VGL(V)</th></tr><tr><td>0</td><td>-6.7V</td></tr><tr><td>1</td><td>-7.0V</td></tr><tr><td>2</td><td>-7.3V</td></tr><tr><td>3</td><td>-7.6V</td></tr><tr><td colspan="2">:</td></tr><tr><td>29</td><td>-15.4V</td></tr><tr><td>30</td><td>-15.7V</td></tr><tr><td>31</td><td>-16.0V</td></tr></table></td><td>v</td></tr>
<tr><td rowspan="3">0xC1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>1</td><td>1</td><td>CPCLKH [1:0]</td><td>VGH/VGL charge pump clock cycle.
00b:4H 01b:2H 10b:1H 11b:0.5H</td><td>v</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>1</td><td>1</td><td>-</td><td>-</td><td>VGHXSP[1:0]</td><td>VGH boosting multiple selection
00: 2X
01: 3X
10: 4X
11: 4X</td><td>v</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>VGLXSP</td><td>VGL boosting multiple selection
0: -2X
1: -3X</td><td>v</td></tr>
<tr><td>0xC2</td><td>-</td><td>-</td><td>-</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>VGPHS[4:0]</td><td>Positive gamma high voltage selection . Range is from 4V ~ 5.5V. (Default=4.2V) Step=0.05V.
<table><tr><th>VPHS[4:0]</th><th>Output VGPH(V)</th></tr><tr><td>0x00</td><td>4.00V</td></tr><tr><td>0x01</td><td>4.05V</td></tr><tr><td>0x02</td><td>4.10V</td></tr><tr><td>0x03</td><td>4.15V</td></tr><tr><td colspan="2">:</td></tr><tr><td>0x1D</td><td>5.45V</td></tr><tr><td>0x1E</td><td>5.50V</td></tr><tr><td>0x1F</td><td>5.50V</td></tr></table></td><td>v</td></tr>
</table>

<table>
<tr><th rowspan="2">Address [7:0]</th><th colspan="8">Data [7:0] (Default)</th><th rowspan="2">Name</th><th rowspan="2">Description</th><th rowspan="2">OTP</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0xC3</td><td>-</td><td>-</td><td>-</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>VGPLS[4:0]</td><td>Positive gamma low voltage selection.
Range is from 0.1V ~ 1.6V. (Default=0.2V)
Step=0.05V.
<table><tr><th>VPLS[4:0]</th><th>Output VGPL(V)</th></tr><tr><td>0x00</td><td>0.10V</td></tr><tr><td>0x01</td><td>0.15V</td></tr><tr><td>0x02</td><td>0.20V</td></tr><tr><td>0x03</td><td>0.25V</td></tr><tr><td colspan="2">:</td></tr><tr><td>0x1D</td><td>1.55V</td></tr><tr><td>0x1E</td><td>1.60V</td></tr><tr><td>0x1F</td><td>1.60V</td></tr></table></td><td>v</td></tr>
<tr><td>0xC4</td><td>-</td><td>-</td><td>-</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>VGNHS[4:0]</td><td>Negative gamma high voltage selection. Range is from -4V ~ -5.5V. (Default=-4.2V). Step=0.05V.
<table><tr><th>VNHS[4:0]</th><th>Output VGNH(V)</th></tr><tr><td>0x00</td><td>-4.00V</td></tr><tr><td>0x01</td><td>-4.05V</td></tr><tr><td>0x02</td><td>-4.10V</td></tr><tr><td>0x03</td><td>-4.15V</td></tr><tr><td colspan="2">:</td></tr><tr><td>0x1D</td><td>-5.45V</td></tr><tr><td>0x1E</td><td>-5.50V</td></tr><tr><td>0x1F</td><td>-5.50V</td></tr></table></td><td>v</td></tr>
<tr><td>0xC5</td><td>-</td><td>-</td><td>-</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>VGNLS[4:0]</td><td>Negative gamma low voltage selection. Range is from -0.1V ~ -1.6V. (Default=-0.2V)
Step=0.05V.
<table><tr><th>VNLS[4:0]</th><th>Output VGNL(V)</th></tr><tr><td>0x00</td><td>-0.10V</td></tr><tr><td>0x01</td><td>-0.15V</td></tr><tr><td>0x02</td><td>-0.20V</td></tr><tr><td>0x03</td><td>-0.25V</td></tr><tr><td colspan="2">:</td></tr><tr><td>0x1D</td><td>-1.55V</td></tr><tr><td>0x1E</td><td>-1.60V</td></tr><tr><td>0x1F</td><td>-1.60V</td></tr></table></td><td>v</td></tr>
<tr><td>0xC6</td><td>-</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>STILLIMG_DET_NUM</td><td>Still image detect frame number.
Detect still image input to enter LPM10 mode.2n frames/step(value 0 can’t use)</td><td>v</td></tr>
<tr><td>0xC7</td><td>-</td><td>-</td><td>-</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>RER_NUM</td><td>Refresh frame number in LPM10 mode.
2n+1 frames/step</td><td>v</td></tr>
<tr><td>0xC8</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>NOREF_NUM</td><td>No refresh frame number in LPM10 mode
2n+1 frames/step</td><td>v</td></tr>
<tr><td rowspan="2">0xCC</td><td>-</td><td>-</td><td>-</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>EQ0/1W[4:0](1)</td><td>Source EQ0/1 time setting. EQ0/1W is N.
T_{EQ0}=4N*40ns(EQ0/1W=0 N=0,EQ0/1W<4 N=3)</td><td>v</td></tr>
<tr><td>-</td><td>0</td><td>0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>POCSD_CTL[1:0]</td><td>Source output offset cancel method selection.
00:1+2line 01:2line 10:1line 11:off</td><td>v</td></tr>
<tr><td>0xCD</td><td>0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>VPP_EN</td><td>1:internal VPP enable 0:internal VPP disable</td><td></td></tr>
<tr><td rowspan="5">0xF9</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>1</td><td>FLC2B_SEL</td><td>FLC2B signal output selection.
1: VGL output 0:FLC2B output</td><td>v</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>0</td><td>-</td><td>GOA_POWEROFF</td><td>1:GOA keeps VGH 0:GOA keeps active</td><td>v</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>1</td><td>-</td><td>-</td><td>GOA_POWERON</td><td>CLR1/2 output selection when power on
1:CLR1 keeps VGL,CLR2 keeps VGH
0:CLR1 keeps VGH,CLR2 keeps VGL</td><td>v</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>1</td><td>-</td><td>-</td><td>-</td><td>GOA_GAS</td><td>GOA output when GAS enable
1:VGH 0:VGL</td><td>v</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Reserved</td><td>Reserved</td><td>-</td></tr>
<tr><td>0xFB</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>1</td><td>GRB</td><td>All spi register reset 1: normal 0: reset register</td><td>-</td></tr>
<tr><td>0xFC</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>PRODUCTID1</td><td>Read only. The value is 0x82</td><td>-</td></tr>
<tr><td>0xFD</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>PRODUCTID2</td><td>Read only. The value is 0x79</td><td>-</td></tr>
<tr><td>0xFE</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>PRODUCTID3</td><td>Read only. The value is 0x0D</td><td>-</td></tr>
<tr><td>0xFF</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>CHIPID</td><td>Read only.</td><td>-</td></tr>
<tr><td colspan="11">Note: (1)EQ0: SOUT pre charge to GND when SOUT polarization change.
EQ1:SOUT charges sharing by odd CHs short and even CHs short when n line and n+1 line datas are different up to 1/2.</td></tr>
</table>

9.2 Register of page 1 (OTP & GOA MUX)

Address [7:0]	Data [7:0] (Default) 7	6	5	4	3	2	1	0	Name	Description	OTP
0xB1	-	-	0	0	0	0	0	0	OTP_GROUP[4:0]	OTP trimming group select. The group range is from group0 to group35	-
0xB2	0	1	0	1	1	0	1	0	OTP_PWD[7:0]	Set to 0xA5 to enable 0xB3 command.	-
0xB3	-	-	-	-	-	-	-	0	OTP_WR(1)	Auto OTP program mode write command	-
	-	-	-	-	-	0	-	-	OTP_RE_LOAD	OTP auto re-load command.	-
	0	-	-	-	-	-	-	-	OTP_BURST_WR(2)	OTP burst write command	-
0xB9	-	-	0	0	-	-	-	-	DISABLE_OTP[1:0]	OTP function disables.	-

DISABLE_OTP	Master OTP function	Slave OTP function
00b	Enable	Enable
01b	Enable	Disable
10b	Disable	Enable
11b	Disable	Disable

0xBB	0	0	0	0	0	0	0	0	OTP_BURST_INDEX[7:0]	Burst program group index(group0~7)	-
0xBC	0	0	0	0	0	0	0	0	OTP_BURST_INDEX[15:8]	Burst program group index(group8~15)	-
0xBD	0	0	0	0	0	0	0	0	OTP_BURST_INDEX[23:16]	Burst program group index(group16~23)	-
0xBE	0	0	0	0	0	0	0	0	OTP_BURST_INDEX[31:24]	Burst program group index(group24~31)	-
0xBF	-	-	-	-	0	0	0	0	OTP_BURST_INDEX[35:32]	Burst program group index(group32~35)	-

Note:
(1) OTP auto program mode (program by group) sequence：
Write OTP setting value→write OTP group N(0xB1=N)→write 0xB2=0xA5→write 0xB3[0]=1
(2) OTP burst write mode(program by group index) sequence：
Write OTP setting value→write group index(0xBB[n]=1,n mean OTP group)→ write 0xB2=0xA5→write 0xB3[7]=1
EX. Program OTP group 5,10,,20,30,35
Write OTP setting value→
write 0xBB[5]=1(group5),0xBC[3]=1(group10),0xBD[4]=1(group20),0xBE[6]=1(group30),0xBF[3]=1(group35)
→ write 0xB2=0xA5→write 0xB3[7]=1

0xC0~0xD3	-	-	0	0	0	0	0	0	GOUTL_[20:1]_SEL	Mux GOA signal to GOUTL pin.	v
	0	0	-	-	-	-	-	-	GOUTL_[20:1]_STB	GOUTR_20 level in standby mode 00:VGL 01:VGH 10:GND 11:reserve	v
0xD4~0xE7	-	-	0	0	0	0	0	0	GOUTR_[20:1]_SEL	Mux GOA signal to GOUTR pin.	v
	0	0	-	-	-	-	-	-	GOUTR_[20:1]_STB	GOUTR_20 level in standby mode 00:VGL 01:VGH 10:GND 11:reserve	v

SEL[5:0]	GOA Output
0x00	VGL
0x01	STV1
0x02	STV2
0x03	STV3
0x04	STV4
0x05	CKV1
0x06	CKV2
0x07	CKV3
0x08	CKV4
0x09	CKV5

SEL[5:0]	GOA Output
0x0A	CKV6
0x0B	CKV7
0x0C	CKV8
0x0D	CLR1
0x0E	CLR2
0x0F	CLR3
0x10	CLR4
0x11	FLC1
0x12	FLC2
0x13	GCKA

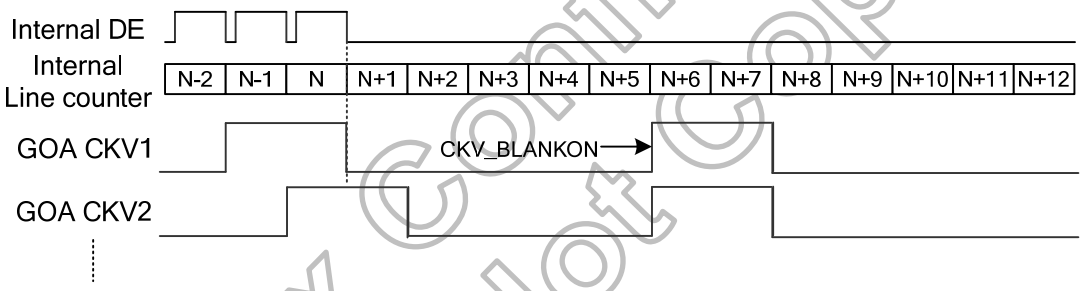
SEL[5:0]	GOA Output
0x14	GCKB
0x15	DIR
0x16	DIRB
0x17	STV5
0x18	STV6
0x19	STV7
0x1A	STV8
0x1B	CKV9
0x1C	CKV10
0x1D	CKV11

SEL[5:0]	GOA Output
0x1E	CKV12
0x1F	CKV13
0x20	CKV14
0x21	CKV15
0x22	CKV16
0x23	FLC1B
0x24	FLC2B
0x26	VGH

9.3 Register of page 3 (GOA)

Address [7:0]	Data [7:0] (Default) 7	6	5	4	3	2	1	0	Name	Description	OTP
0xB9	-	-	0	0	0	0	0	0	Reserved	Reserved	-
	-	0	-	-	-	-	-	-	FLC_SEL	FLC output selection 1:for CPT signal output 0:for FLC output	v
	0	-	-	-	-	-	-	-	Reserved	Reserved	-
0xBB	-	-	-	-	-	0	0	0	STV_PREC[2:0]	STV pre-charge width adjustment 1 OSC25M/step	v
	0	0	0	0	-	-	-	-	Reserved	Reserved	-
0xBC	0	0	0	0	0	0	0	0	CKV_FALL_PREC[7:0]	CKV falling pre-charge width adjustment. 1 OSC25M/step	v
0xBE	-	-	-	-	-	0	0	1	GOA_PHASE[2:0]	GOA phase selection. 000b:4 phase. 001b:8 phase. 010b:6 phase. 011b:12phase. 100b:16 phase. others: Reserve.	v
	-	-	-	-	0	-	-	-	CKV_BLANKON	CKV blanking on enable. 0:Disable. 1:Enable.	v
	-	-	-	0	-	-	-	-	Reserved	Reserved	-
	-	-	0	-	-	-	-	-	GOA_UD	GOA scan direction selection.XOR page0 0xB2[5]	v
	0	0	-	-	-	-	-	-	Reserved	Reserved	-

Note: (1)



0xBF	-	-	-	-	0	0	0	0	Reserved	Reserved	-
	-	-	0	1	-	-	-	-	GOA_Tn_FACTOR	GOA Timing (T0~T5) adjustment factor selection. 00: Tnx1 01: Tnx2. 10: Tnx4 11: Tnx8	v
	0	0	-	-	-	-	-	-	Reserved	Reserved	-
0xC2	0	0	0	0	0	0	0	0	GOA_T0[7:0]	Odd STV falling position adjustment. T0=GOA_T0[7:0] x GOA_Tn_FACTOR.	v
0xC3	0	0	1	1	1	0	1	0	GOA_T1[7:0]	Odd STV rising position adjustment. T1=GOA_T1[7:0] x GOA_Tn_FACTOR.	v
0xC4	0	0	0	0	0	0	0	0	GOA_T2[7:0]	Odd CKV falling position adjustment. T2=GOA_T2[7:0] x GOA_Tn_FACTOR.	v
0xC5	0	0	1	0	1	1	0	0	GOA_T3[7:0]	Odd CKV rising position adjustment. T3=GOA_T3[7:0] x GOA_Tn_FACTOR.	v
0xC6	0	0	0	0	0	0	0	0	GOA_T4[7:0]	Odd GCK falling position adjustment. T4=GOA_T4[7:0] x GOA_Tn_FACTOR.	v
0xC7	0	0	0	0	0	0	0	1	GOA_T5[7:0]	Odd GCK rising position adjustment. T5=GOA_T5[7:0] x GOA_Tn_FACTOR.	v

Note: (2) Unit is OSC25M.

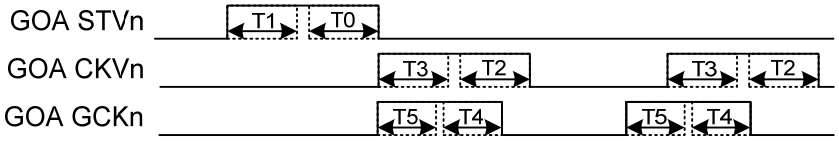


Figure 9.1: GOA timing tune

Address [7:0]	Data [7:0] (Default) 7	6	5	4	3	2	1	0	Name	Description	OTP
0xC8	-	-	-	0	1	1	0	1	STV_LEAD[4:0]	GOA STV leads time adjustment.	v
	0	0	0	-	-	-	-	-	Reserved	Reserved	-
0xC9	-	-	-	0	1	0	1	1	CKV_LEAD[4:0]	GOA CKV leads time adjustment.	v
	0	0	0	-	-	-	-	-	Reserved	Reserved	-

Note: (3) a. Unit is H.
b. VT is meats V-total.

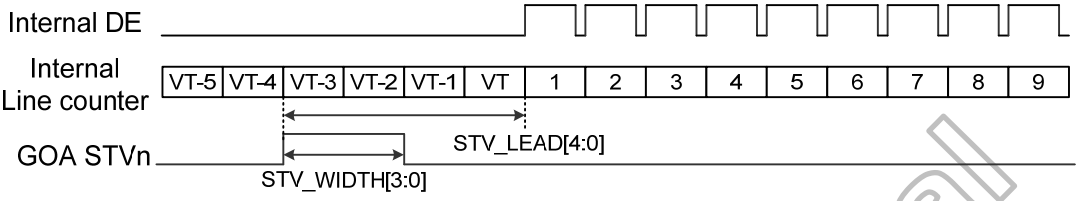


Figure 9.2: GOA STV time chart

(4)a. Unit is H.
b. VT is meats V-total.

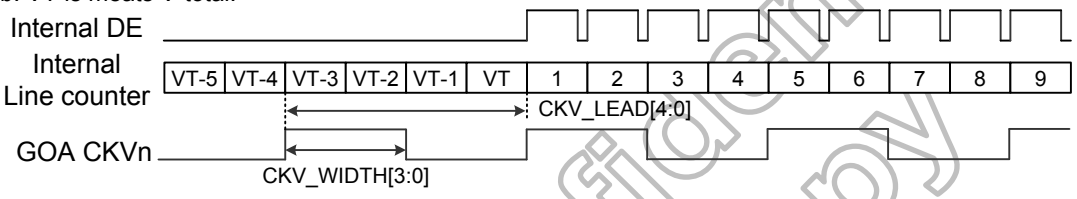


Figure 9.3: GOA CKV time chart

0xCA	-	-	0	0	0	0	1	0	CKV_DUMMY[5:0]	GOA CKV dummy number in V-blanking. The total number is CKV_DUMMY[5:0]xGOA Phase,	v
	-	1	-	-	-	-	-	-	Reserved	Reserved	-
	0	-	-	-	-	-	-	-	CKV_NONOVERLAP	CKV non-overlap control 0: Non-overlap 1: overlap	v

Note: (5) a. N is meats V-Active lines.
b. DUMMY must be less than V-front porch.

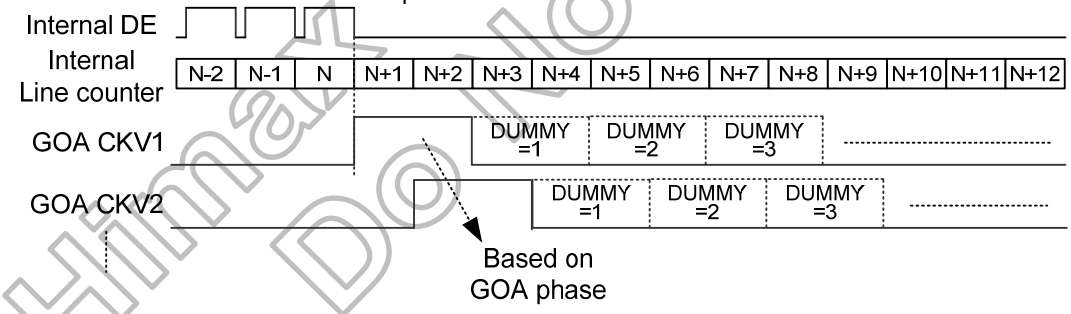


Figure 9.4: GOA CKV dummy chart

0xCB	0	0	0	0	0	0	0	0	CKV_RISE_PREC[7:0]	CKV rising pre-charge width adjustment. 1 OSC25M/step	v

Note: (6)

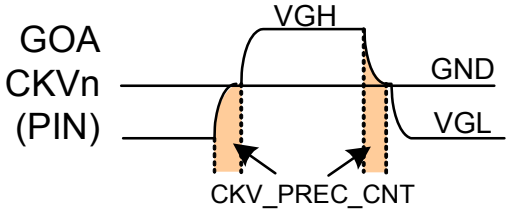


Figure 9.5: GOA precharge time chart

Address [7:0]	Data [7:0] (Default) 7	6	5	4	3	2	1	0	Name	Description	OTP
0xCC	-	-	-	-	0	1	0	0	CKV_WIDTH[3:0]	GOA CKV width adjustment.	v
	0	1	0	0	-	-	-	-	STV_WIDTH[3:0]	GOA STV width adjustment.	v
0xCD	0	0	0	0	0	1	1	1	GOA_FLC[7:0]	GOA FLC toggle frame adjustment. The toggle frame range is 1 ~ 127 frames.	v

Note: (7)

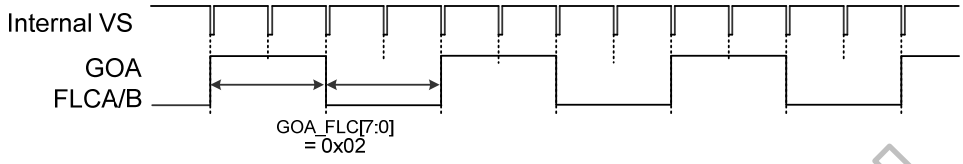


Figure 9.6: GOA FLC time chart

0xCE	-	0	1	0	0	0	0	0	GOA_FLC_LEAD[6:0]	FLC toggle point adjustment	v
	0	-	-	-	-	-	-	-	Reserved	Reserved	-
0xCF	-	-	-	-	-	0	0	0	CLR_WD[10:8]	CLR width adjustment bits[10:8]	v
	-	-	-	-	1	-	-	-	CLR_adjsel	CLR adjustment selection 1:rising adjust 0:width adjust	v
	-	1	1	0	-	-	-	-	Reserved	Reserved	-
	0	-	-	-	-	-	-	-	FLC_sync	FLC sync selection 1:Sync with 1st STV 0:Sync with last DE	v
0xD0	0	0	0	0	0	1	0	1	CKV_BLANK_SHIFT[7:0]	Blank CKV shift from the last DE. H/step	v
0xD1	0	0	0	0	0	1	1	0	CKV_BLANK_WIDTH[7:0]	Blank CKV width adjustment. H/step	v
0xD2	0	0	0	0	0	1	1	0	CLR1_WD[7:0]	GOA CLR1 width adjustment CLR1_WIDTH[10:0]=CLR1234_WD_MSB[2:0]x256 + CLR1_WD[7:0]	v
0xD3	0	0	0	0	0	1	1	0	CLR234_WD[7:0]	GOA CLR234 width adjustment. CLR234_WIDTH[10:0]=CLR1234_WD_MSB[2:0]x256+CLR234_WD[7:0]	v

Note: (8) a. Unit is H.
b. The total value must be less than V-front porch.

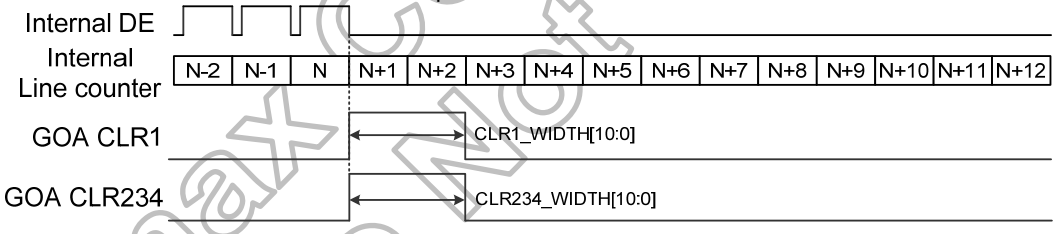


Figure 9.7: CLR width time chart

0xD4	-	0	0	0	1	0	0	0	CLR1_START[6:0]	CLR1 start position. CLR1_ST[10:0]=CLR1_START_MSB[3:0]x128+CLR1_START[6:0]	v
	1	-	-	-	-	-	-	-	CLR1_POL	CLR1 polarity setting. 0: Non-inversion. 1: Inversion.	v
0xD5	-	0	0	0	1	0	0	1	CLR2_START[6:0]	CLR2 start position. CLR2_ST[10:0]=CLR234_START_MSB[3:0]x128+CLR2_START[6:0]	v
	0	-	-	-	-	-	-	-	CLR2_POL	CLR2 polarity setting. 0: Non-inversion. 1: Inversion.	v
0xD6	-	0	0	0	1	0	0	0	CLR3_START[6:0]	CLR3 start position. CLR3_ST[10:0]=CLR234_START_MSB[3:0]x128+CLR3_START[6:0]	v
	1	-	-	-	-	-	-	-	CLR3_POL	CLR3 polarity setting. 0: Non-inversion. 1: Inversion.	v
0xD7	-	0	0	0	1	0	0	0	CLR4_START[6:0]	CLR4 start position. CLR4_ST[10:0]=CLR234_START_MSB[3:0]x128+CLR4_START[6:0]	v
	0	-	-	-	-	-	-	-	CLR4_POL	CLR4 polarity setting. 0: Non-inversion. 1: Inversion.	v

Address [7:0]	Data [7:0] (Default) 7	6	5	4	3	2	1	0	Name	Description	OTP
0xD8	-	-	-	-	0	0	0	0	CLR1_START_MSB[3:0]	MSB[10:7] of CLR1 start position.	v
	0	0	0	0	-	-	-	-	CLR2/3/4_START_MSB[3:0]	MSB[10:7] of CLR2/3/4 start position.	v

Note: (9) a. Unit is H-total.
b. The total value must be less than V-total

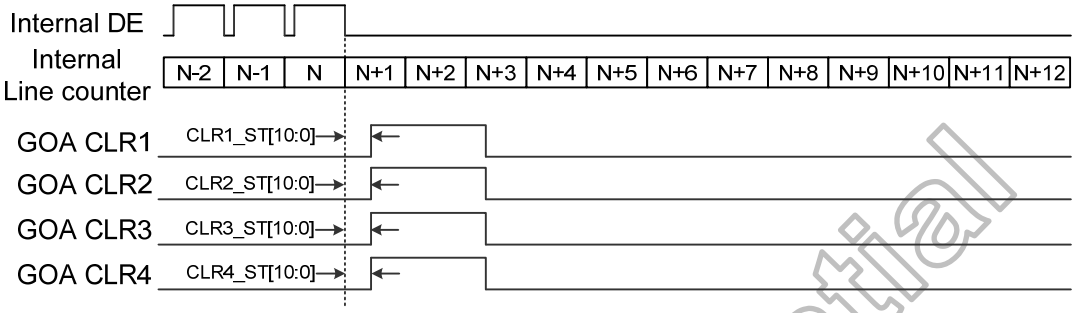


Figure 9.8: CLR start position time chart

0xD9	-	-	-	-	-	-	-	0	CLR2_LEAD	GOA CLR2 offset direction setting.	v
	-	-	-	-	-	-	0	-	CLR3_LEAD	GOA CLR3 offset direction setting.	v
	-	-	-	-	-	0	-	-	CLR4_LEAD	GOA CLR4 offset direction setting.	v
	0	0	0	0	0	-	-	-	Reserved	Reserved	-
0xDB	-	-	-	-	-	-	-	0	CLR1_LEAD	GOA CLR1 offset direction setting.	v
	-	-	-	-	0	0	0	-	FLC_NONOVLAP[1:0]	FLC overlap setting. 00b:0H x1b:1H 10b:2H	v
	0	0	0	0	-	-	-	-	Reserved	Reserved	-
0xDD	0	0	0	0	0	0	0	1	GOA_T2B[7:0]	Even CKV falling position adjustment. T0=GOA_T2B[7:0] x GOA_Tn_FACTOR.	v
0xDE	0	0	1	0	1	1	0	0	GOA_T3B[7:0]	Even CKV rising position adjustment. T0=GOA_T3B[7:0] x GOA_Tn_FACTOR.	v
0xE6	0	0	0	0	0	0	0	0	GOA_T0B[7:0]	Even STV falling position adjustment. T0=GOA_T0B[7:0] x GOA_Tn_FACTOR.	v
0xE7	0	0	1	1	1	0	1	0	GOA_T1B[7:0]	Even STV rising position adjustment. T0=GOA_T1B[7:0] x GOA_Tn_FACTOR.	v

9.4 Register of page 5 (MIPI)

Address(M) is for master, Address(S) is for slave, Address(M/S) is for master and slave

Address [7:0]	Data [7:0] (Default) 7	6	5	4	3	2	1	0	Name	Description	OTP
0xB1	-	-	-	-	-	1	0	1	Reserved	Reserved	v
	-	-	-	-	0	-	-	-	R_EoTpEN	Decode EoTp packet enable. 0:disable 1:enable	v
	1	1	1	0	-	-	-	-	Reserved	Reserved	v
0xB3	-	-	-	-	0	0	1	0	T_TLPX	TLPX time of BTA adjustment TLPX time=T_TLPX*40ns	v
	-	-	-	1	-	-	-	-	Lhs_settle	Ths_settle time latch by OSC25 edge selection. 1:rising 0:falling	v
	0	0	1	-	-	-	-	-	Ths_settle	Ths_settle adjustment Ths_settle time=(Ths_settle+1)*40ns	v
0xC0(M) 0xD9(S)	-	-	-	-	-	1	0	1	TRC_VAL	Terminal resistor of CLK lane value adjustment TR_ADJ[2:0] / TR(ohm) 000 / 255 001 / 192 010 / 153 011 / 128 100 / 118 101 / 102 110 / 90 111 / 81	v
	0	0	-	-	-	-	-	-	TR_EN	Terminal resistor enable 00: turn on TR 10: turn off TR	v
0xC2(M) 0xDB(S)	-	-	-	-	-	1	0	1	TRD_VAL	Terminal resistor of data lane value adjustment TR_ADJ[2:0] / TR(ohm) 000 / 255 001 / 192 010 / 153 011 / 128 100 / 118 101 / 102 110 / 90 111 / 81	v
		1	0	1					Reserved	Reserved	v
0xC5(M/S)	-	-	-	-	1	-	-	-	Reserved	Reserved	v
	-	0	0	1	-	-	-	-	TUNEC	CLK lane skew adjustment	v
0xC6(M)	-	-	-	-	-	0	0	0	TUNED0	Data lane0 skew adjustment	v
0xDC(S)	-	0	0	0	-	-	-	-	TUNED1	Data lane1 skew adjustment	v
0xC7(M)	-	-	-	-	-	0	0	0	TUNED2	Data lane2 skew adjustment	v
0xDD(S)	-	0	0	0	-	-	-	-	TUNED3	Data lane3 skew adjustment	v

9.5 Register of page 6 (Engineer)

<table>
<tr><th rowspan="2">Address [7:0]</th><th colspan="8">Data [7:0] (Default)</th><th rowspan="2">Name</th><th rowspan="2">Description</th><th rowspan="2">OTP</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0xB8</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Engineer_PWD</td><td>Engineer_PWD = A5h to enable engineer register</td><td>v</td></tr>
<tr><td rowspan="2">0xBC</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>0</td><td>0</td><td>0</td><td>POCGMD_CTL</td><td>Gamma buffer chopper control
<table><tr><th>Value</th><th>POCGMD_CTL</th></tr><tr><td>0</td><td>1 line</td></tr><tr><td>1</td><td>2 line</td></tr><tr><td>2</td><td>4 line</td></tr><tr><td>3</td><td>1 frame</td></tr><tr><td>4</td><td>2 frame</td></tr><tr><td>5</td><td>4 frame</td></tr><tr><td>6</td><td>8 frame</td></tr><tr><td>7</td><td>Non toggle</td></tr></table></td><td>v</td></tr>
<tr><td>-</td><td>0</td><td>0</td><td>0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>POCGM_CTL</td><td>Gamma chopper control
<table><tr><th>Value</th><th>POCGM_CTL</th></tr><tr><td>0</td><td>1 line</td></tr><tr><td>1</td><td>2 line</td></tr><tr><td>2</td><td>4 line</td></tr><tr><td>3</td><td>1 frame</td></tr><tr><td>4</td><td>2 frame</td></tr><tr><td>5</td><td>4 frame</td></tr><tr><td>6</td><td>8 frame</td></tr><tr><td>7</td><td>Non toggle</td></tr></table></td><td>v</td></tr>
<tr><td>0xC0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Function_EN</td><td>Function_EN=A5h to enable in-house function</td><td>v</td></tr>
<tr><td rowspan="2">0xC7</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>1</td><td>0</td><td>VCCS</td><td>VCC adjustment
00:1,45mV,01:1.5mV,10:1.55mV,11:1.6mV</td><td>v</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>1</td><td>0</td><td>-</td><td>-</td><td>VCCIFS</td><td>VCCIF adjustment.
00:1,45mV,01:1.5mV,10:1.55mV,11:1.6mV</td><td>v</td></tr>
<tr><td>0xD5</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>GOE_WD</td><td>Source delay time adjustment(CKV falling to Source off)
Source delay time=GOE_WD*40ns</td><td>v</td></tr>
</table>

10. Function Description

10.1 BIST function

When BIST_ENB is trigger to low, then HX8279-D01 will leave normal operation mode and starts to generate the BIST pattern to LCD panel without MIPI input signals.

10.1.1 BIST output timing

BIST mode	H-active	H-total	V-total	Frame rate(Hz)	osc_freq(MHz)
1200RGBx1920	600	690	1940	60	80
1200RGBx1600	600	696	1620	60	68
1080RGBx1920	540	632	1940	60	74
600RGBx1024	300	345	1044	60	21

Note: (1) BIST mode is 2-pixel/dclk.

Table 10.1: BIST mode with multi drop type

BIST mode	H-active	H-total	V-total	Frame rate(Hz)	osc_freq(MHz)
1200RGBx1920	300	420	1940	56	46
1200RGBx1600	300	420	1620	57	39
1080RGBx1920	270	380	1940	56	42
600RGBx1024	300	430	1044	55	25

Note: (1) BIST mode is 4-pixel/dclk.

Table 10.2: BIST mode with RL type

10.1.2 BIST pattern

The BIST pattern is illustrated as below figure. Each pattern will display about 127 frames.

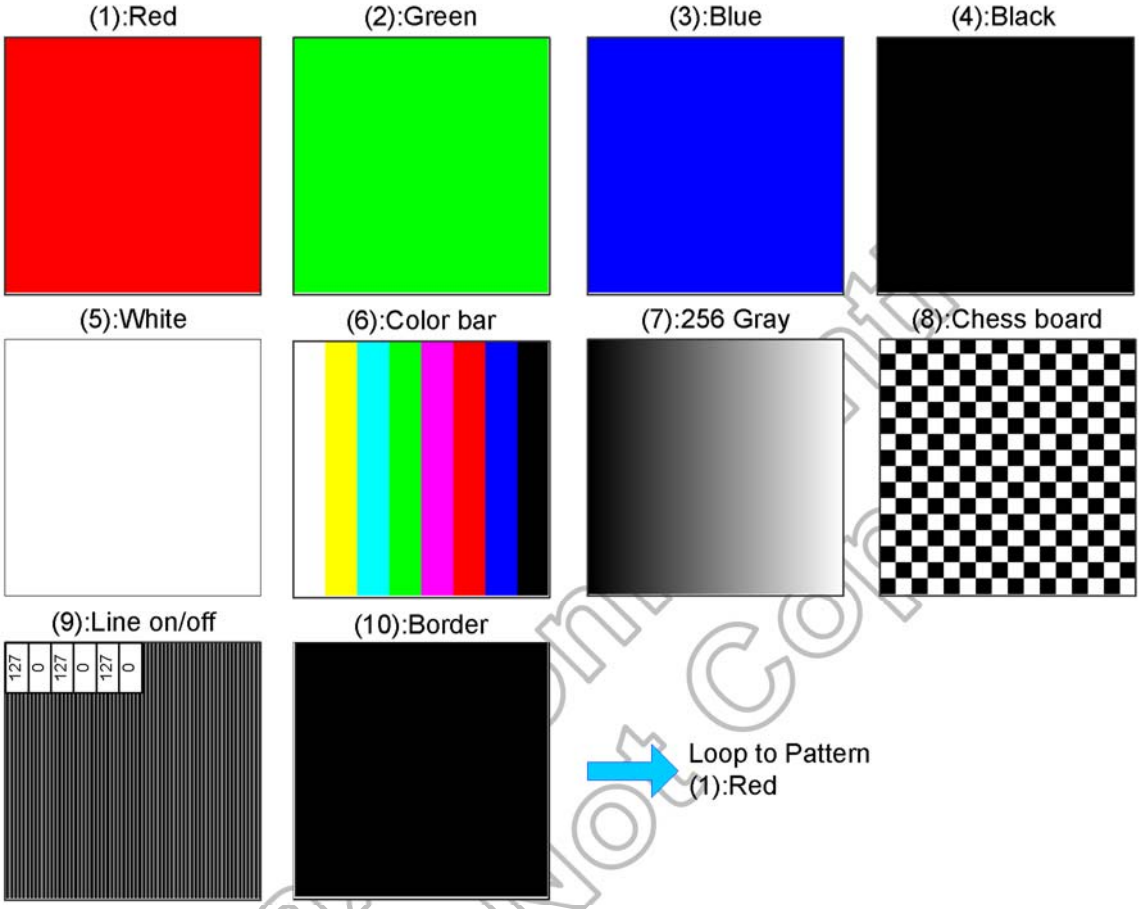


Figure 10.1: BIST pattern loop

10.2 OTP function

10.2.1 OTP programming by internal VPP and OTP time check flow

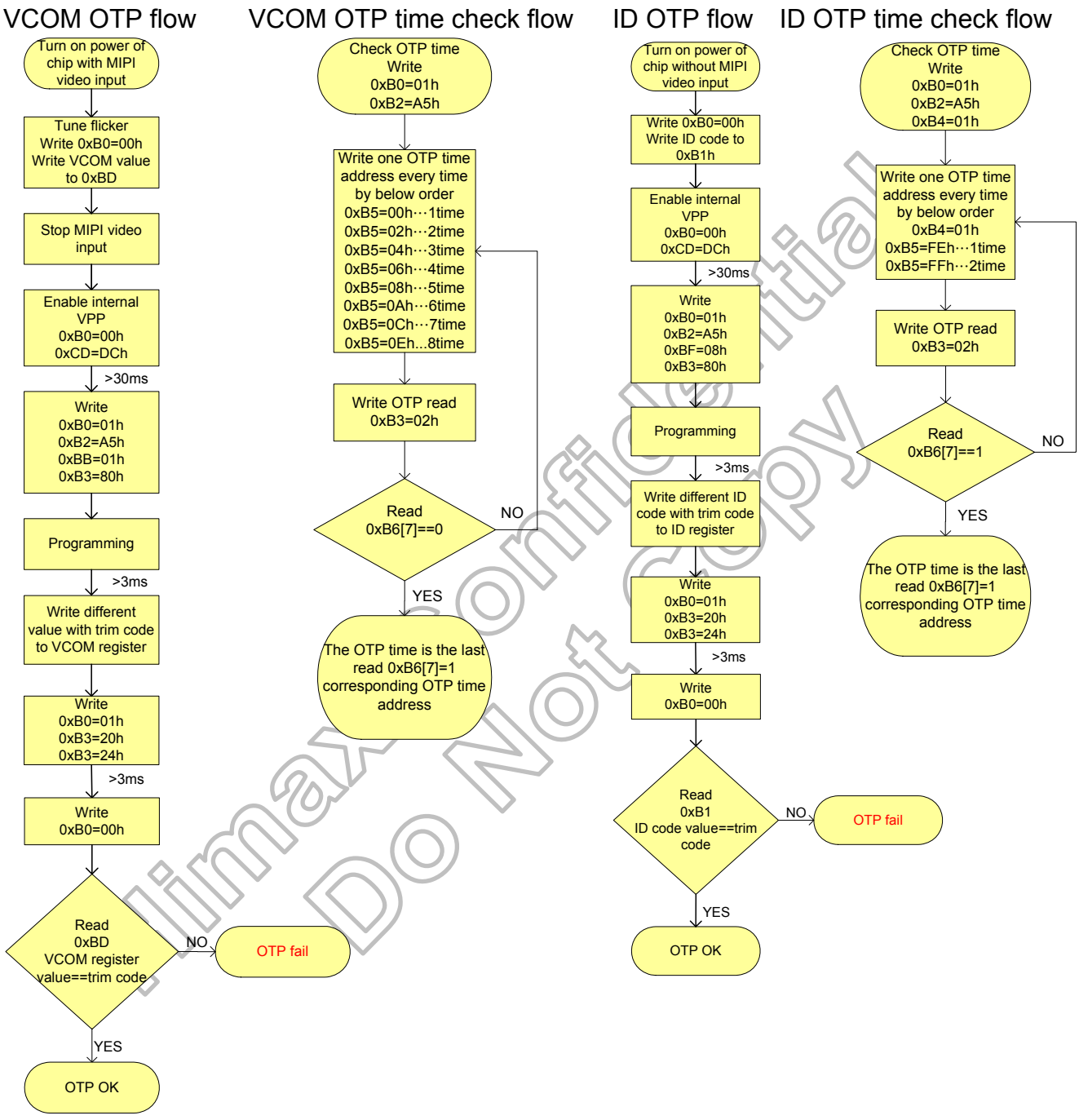


Figure 10.2: OTP of VCOM and ID programming flow

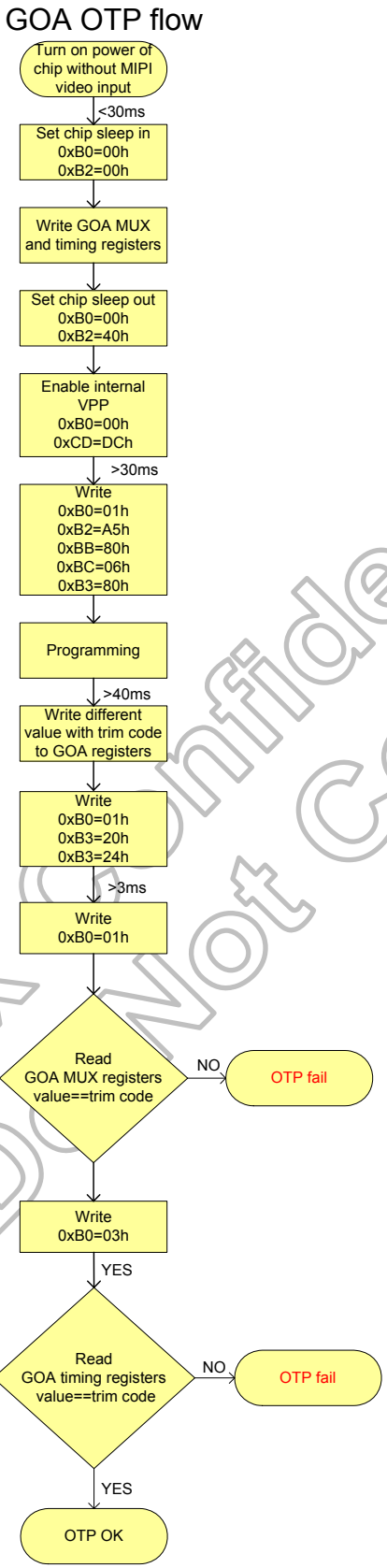


Figure 10.3: OTP of GOA programming flow

10.2.2 OTP group table

OTP_index	D7	D6	D5	D4	D3	D2	D1	D0	Group	SPI page	SPI address
0	W1	-	-	-	-		-		GROUP0	page0	-
1	T_VCOMS[7:0]										3D
2	W2	-	-	-	-		-				-
3	T_VCOMS[7:0]										3D
4	W3	-	-	-	-		-				-
5	T_VCOMS[7:0]										3D
6	W4	-	-	-	-		-				-
7	T_VCOMS[7:0]										3D
8	W5	-	-	-	-		-				-
9	T_VCOMS[7:0]										3D
10	W6	-	-	-	-		-				-
11	T_VCOMS[7:0]										3D
12	W7	-	-	-	-		-				-
13	T_VCOMS[7:0]										3D
14	W8	-	-	-	-		-				-
15	T_VCOMS[7:0]										3D
16	W1	-	-	-	-		-		GROUP1		-
17	LPM_VCOMS[7:0]										3E
18	W1	-	UPDNB	LR	ZIGZAG	ZTYPE	NBW	BISTB	GROUP2		32
19	DISP_ON	LPM_CTRL[1:0]		PWRMD	VRES_FIX	LED_EN	RES[1:0]				33
20	VRES[7:0]										34
21	ZDATA[7:0]										35
22	-	RP1EN	RP2EN	-	CABC_CTRL[1:0]		DITHER_EN	D_GAM_EN			36
23	-	-	-	OVERLAP[3:0]				PCLK_SEL			37
24	GOA_EN	VCOM_EN	PNSW	MIPI_TYPE	LNSW[1:0]		MIPI_LAN[1:0]				38
26	BLREV[1:0]		BLREVONFF	INV_SEL2	SD_ISSEL[1:0]		INV_SEL[1:0]				3a
27	W1	-	-	VGHS[4:0]					GROUP3		3f
28	-	-	-	VGLS[4:0]							40
29	-	-	-	VGLXSP[1:0]	VGHXSP[1:0]		CPCLKH [1:0]				41
30	-	-	-	VPHS[4:0]							42
31	-	-	-	VPLS[4:0]							43
32	-	-	-	VNHS[4:0]							44
33	-	-	-	VNLS[4:0]							45
34	W1	STILLIMG_DET_NUM[6:0]							GROUP4		46
35	-	-	-	-	REF_NUM[3:0]						47
36	NOREF_NUM[7:0]										48
40	W1	POCSD_CTL[1:0]		SD_EQW[4:0]					GROUP5		4c
44	W1	-	-	-	-	-	-	-	GROUP7	page1	-
45	GOUTL_1_STB[1:0]	GOUTL_1_SEL[5:0]									40
46	GOUTL_2_STB[1:0]	GOUTL_2_SEL[5:0]									41
47	GOUTL_3_STB[1:0]	GOUTL_3_SEL[5:0]									42
48	GOUTL_4_STB[1:0]	GOUTL_4_SEL[5:0]									43
49	GOUTL_5_STB[1:0]	GOUTL_5_SEL[5:0]									44
50	GOUTL_6_STB[1:0]	GOUTL_6_SEL[5:0]									45
51	GOUTL_7_STB[1:0]	GOUTL_7_SEL[5:0]									46
52	GOUTL_8_STB[1:0]	GOUTL_8_SEL[5:0]									47

53	GOUTL_9_STB[1:0]	GOUTL_9_SEL[5:0]							48
54	GOUTL_10_STB[1:0]	GOUTL_10_SEL[5:0]							49
55	GOUTL_11_STB[1:0]	GOUTL_11_SEL[5:0]							4a
56	GOUTL_12_STB[1:0]	GOUTL_12_SEL[5:0]							4b
57	GOUTL_13_STB[1:0]	GOUTL_13_SEL[5:0]							4c
58	GOUTL_14_STB[1:0]	GOUTL_14_SEL[5:0]							4d
59	GOUTL_15_STB[1:0]	GOUTL_15_SEL[5:0]							4e
60	GOUTL_16_STB[1:0]	GOUTL_16_SEL[5:0]							4f
61	GOUTL_17_STB[1:0]	GOUTL_17_SEL[5:0]							50
62	GOUTL_18_STB[1:0]	GOUTL_18_SEL[5:0]							51
63	GOUTL_19_STB[1:0]	GOUTL_19_SEL[5:0]							52
64	GOUTL_20_STB[1:0]	GOUTL_20_SEL[5:0]							53
65	GOUTR_1_STB[1:0]	GOUTR_1_SEL[5:0]							54
66	GOUTR_2_STB[1:0]	GOUTR_2_SEL[5:0]							55
67	GOUTR_3_STB[1:0]	GOUTR_3_SEL[5:0]							56
68	GOUTR_4_STB[1:0]	GOUTR_4_SEL[5:0]							57
69	GOUTR_5_STB[1:0]	GOUTR_5_SEL[5:0]							58
70	GOUTR_6_STB[1:0]	GOUTR_6_SEL[5:0]							59
71	GOUTR_7_STB[1:0]	GOUTR_7_SEL[5:0]							5a
72	GOUTR_8_STB[1:0]	GOUTR_8_SEL[5:0]							5b
73	GOUTR_9_STB[1:0]	GOUTR_9_SEL[5:0]							5c
74	GOUTR_10_STB[1:0]	GOUTR_10_SEL[5:0]							5d
75	GOUTR_11_STB[1:0]	GOUTR_11_SEL[5:0]							5e
76	GOUTR_12_STB[1:0]	GOUTR_12_SEL[5:0]							5f
77	GOUTR_13_STB[1:0]	GOUTR_13_SEL[5:0]							60
78	GOUTR_14_STB[1:0]	GOUTR_14_SEL[5:0]							61
79	GOUTR_15_STB[1:0]	GOUTR_15_SEL[5:0]							62
80	GOUTR_16_STB[1:0]	GOUTR_16_SEL[5:0]							63
81	GOUTR_17_STB[1:0]	GOUTR_17_SEL[5:0]							64
82	GOUTR_18_STB[1:0]	GOUTR_18_SEL[5:0]							65
83	GOUTR_19_STB[1:0]	GOUTR_19_SEL[5:0]							66
84	GOUTR_20_STB[1:0]	GOUTR_20_SEL[5:0]							67
85	W1	-	-	-	-	T_PVP_0[2:0]			40
86	-	-	T_PVP_1[5:0]						41
87	-	-	T_PVP_2[5:0]						42
88	-	-	T_PVP_3[5:0]						43
89	-	-	T_PVP_4[5:0]						44
90	-	-	T_PVP_5[5:0]						45
91	-	-	T_PVP_6[5:0]						46
92	-	-	T_PVP_7[5:0]						47
93	-	-	T_PVP_8[5:0]				GROUP8	page2	48
94	-	-	T_PVP_9[5:0]						49
95	-	-	T_PVP_10[5:0]						4a
96	-	-	T_PVP_11[5:0]						4b
97	-	-	T_PVP_12[5:0]						4c
98	-	-	T_PVP_13[5:0]						4d
99	-	-	T_PVP_14[5:0]						4e
100	-	-	T_PVP_15[5:0]						4f
101	-	-	-	-	-	T_PVP_16[2:0]			50

103	-	-	-	-	-	T_PVN_0[2:0]					52
104	-	-	T_PVN_1[5:0]								53
105	-	-	T_PVN_2[5:0]								54
106	-	-	T_PVN_3[5:0]								55
107	-	-	T_PVN_4[5:0]								56
108	-	-	T_PVN_5[5:0]								57
109	-	-	T_PVN_6[5:0]								58
110	-	-	T_PVN_7[5:0]								59
111	-	-	T_PVN_8[5:0]								5a
112	-	-	T_PVN_9[5:0]								5b
113	-	-	T_PVN_10[5:0]								5c
114	-	-	T_PVN_11[5:0]								5d
115	-	-	T_PVN_12[5:0]								5e
116	-	-	T_PVN_13[5:0]								5f
117	-	-	T_PVN_14[5:0]								60
118	-	-	T_PVN_15[5:0]								61
119	-	-	-	-	-	T_PVN_16[2:0]					62
120	W1	-	-	-	-	-	-	-	Group9	page3	-
122	-	-	-	-	STV_PREC[3:0]						3b
123	CKV_FALL_PREC[7:0]										3c
124	spi_goa_ckv_prec_cnt_1stFrame[7:0]										3d
125	-	-	-	-	CKV_BLANKON	GOA_PHASE[2:0]					3e
126	-	-	GOA_Tn_FACTOR[1:0]		-	-	-	-			3f
127	W1	-	-	-	-	-	-	-	GROUP10		-
128	GOA_T0[7:0]										42
129	GOA_T1[7:0]										43
130	GOA_T2[7:0]										44
131	GOA_T3[7:0]										45
132	GOA_T4[7:0]										46
133	GOA_T5[7:0]										47
134	-	-	-	STV_LEAD[4:0]							48
135	-	-	-	CKV_LEAD[4:0]							49
136	CKV_NONOVERLAP	-	CKV_DUMMY[5:0]								4a
137	CKV_RISE_PREC[7:0]										4b
138	STV_WIDTH[3:0]				CKV_WIDTH[3:0]						4c
139	GOA_FLC[7:0]										4d
140	-	GOA)FLCA_LEAD[6:0]									4e
142	CKV_BLANK_SHIFT[7:0]										50
143	CKV_BLANK_WIDTH[7:0]										51
144	CLR1_WD[7:0]										52
145	CLR234_WD[7:0]										53
146	CLR1_POL	CLR1_START[6:0]									54
147	CLR2_POL	CLR2_START[6:0]									55
148	CLR3_POL	CLR3_START[6:0]									56
149	CLR4_POL	CLR4_START[6:0]									57
150	CLR2/3/4_START_MSB[3:0]				CLR1_START_MSB[3:0]						58
151	-	-	-	-	-	CLR4_LEAD	CLR3_LEAD	CLR2_LEAD			59
153	-	-	-	-	-	FLC_NONOVLAP[1:0]		CLR1_LEAD			5b
155	GOA_T2B[7:0]										5d
156	GOA_T3B[7:0]										5e

164	GOA_T0B[7:0]											66
165	GOA_T1B[7:0]											67
166	W2	-	-	-	-	-	-	-				-
167	GOA_T0[7:0]											42
168	GOA_T1[7:0]											43
169	GOA_T2[7:0]											44
170	GOA_T3[7:0]											45
171	GOA_T4[7:0]											46
172	GOA_T5[7:0]											47
173	-	-	-	STV_LEAD[4:0]								48
174	-	-	-	CKV_LEAD[4:0]								49
175	CKV_NONOVERLAP	-	CKV_DUMMY[5:0]									4a
176	CKV_RISE_PREC[7:0]											4b
177	STV_WIDTH[3:0]				CKV_WIDTH[3:0]							4c
178	GOA_FLC[7:0]											4d
179	-	GOA)FLCA_LEAD[6:0]										4e
181	CKV_BLANK_SHIFT[7:0]											50
182	CKV_BLANK_WIDTH[7:0]											51
183	CLR1_WD[7:0]											52
184	CLR234_WD[7:0]											53
185	CLR1_POL	CLR1_START[6:0]										54
186	CLR2_POL	CLR2_START[6:0]										55
187	CLR3_POL	CLR3_START[6:0]										56
188	CLR4_POL	CLR4_START[6:0]										57
189	CLR2/3/4_START_MSB[3:0]				CLR1_START_MSB[3:0]							58
190	-	-	-	-	-	CLR4_LEAD	CLR3_LEAD	CLR2_LEAD				59
192	-	-	-	-	-	FLC_NONOVLAP[1:0]		CLR1_LEAD				5b
194	GOA_T2B[7:0]											5d
195	GOA_T3B[7:0]											5e
203	GOA_T0B[7:0]											66
204	GOA_T1B[7:0]											67
324	W1	-	-	-	-	-	-	-				-
325	PGMA1R[7:0]											31
326	PGMA2R[7:0]											32
327	PGMA3R[7:0]											33
328	PGMA4R[7:0]											34
329	PGMA5R[7:0]											35
330	PGMA6R[7:0]											36
331	PGMA7R[7:0]											37
332	PGMA8R[7:0]											38
333	PGMA9R[7:0]											39
334	PGMA10R[7:0]										GROUP29	page7	3a
335	PGMA11R[7:0]											3b
336	PGMA12R[7:0]											3c
337	PGMA13R[7:0]											3d
338	PGMA14R[7:0]											3e
339	PGMA15R[7:0]											3f
340	PGMA16R[7:0]											40
341	PGMA17R[7:0]											41
342	PGMA18R[7:0]											42
343	PGMA19R[7:0]											43
344	PGMA20R[7:0]											44

345	PGMA21R[7:0]										45
346	PGMA22R[7:0]										46
347	PGMA23R[7:0]										47
348	PGMA24R[7:0]										48
349	PGMA1R[9:8]		PGMA2R[9:8]		PGMA3R[9:8]		PGMA4R[9:8]				49
350	PGMA5R[9:8]		PGMA6R[9:8]		PGMA7R[9:8]		PGMA8R[9:8]				4a
351	PGMA9R[9:8]		PGMA10R[9:8]		PGMA11R[9:8]		PGMA12R[9:8]				4b
352	PGMA13R[9:8]		PGMA14R[9:8]		PGMA15R[9:8]		PGMA16R[9:8]				4c
353	PGMA17R[9:8]		PGMA18R[9:8]		PGMA19R[9:8]		PGMA20R[9:8]				4d
354	PGMA21R[9:8]		PGMA22R[9:8]		PGMA23R[9:8]		PGMA24R[9:8]				4e
355	W1	-	-	-	-	-	-	-			-
356	PGMA1G[7:0]										31
357	PGMA2G[7:0]										32
358	PGMA3G[7:0]										33
359	PGMA4G[7:0]										34
360	PGMA5G[7:0]										35
361	PGMA6G[7:0]										36
362	PGMA7G[7:0]										37
363	PGMA8G[7:0]										38
364	PGMA9G[7:0]										39
365	PGMA10G[7:0]										3a
366	PGMA11G[7:0]										3b
367	PGMA12G[7:0]										3c
368	PGMA13G[7:0]										3d
369	PGMA14G[7:0]										3e
370	PGMA15G[7:0]									GROUP30	page8 3f
371	PGMA16G[7:0]										40
372	PGMA17G[7:0]										41
373	PGMA18G[7:0]										42
374	PGMA19G[7:0]										43
375	PGMA20G[7:0]										44
376	PGMA21G[7:0]										45
377	PGMA22G[7:0]										46
378	PGMA23G[7:0]										47
379	PGMA24G[7:0]										48
380	PGMA1G[9:8]		PGMA2G[9:8]		PGMA3G[9:8]		PGMA4G[9:8]				49
381	PGMA5G[9:8]		PGMA6G[9:8]		PGMA7G[9:8]		PGMA8G[9:8]				4a
382	PGMA9G[9:8]		PGMA10G[9:8]		PGMA11G[9:8]		PGMA12G[9:8]				4b
383	PGMA13G[9:8]		PGMA14G[9:8]		PGMA15G[9:8]		PGMA16G[9:8]				4c
384	PGMA17G[9:8]		PGMA18G[9:8]		PGMA19G[9:8]		PGMA20G[9:8]				4d
385	PGMA21G[9:8]		PGMA22G[9:8]		PGMA23G[9:8]		PGMA24G[9:8]				4e
386	W1	-	-	-	-	-	-	-			-
387	PGMA1B[7:0]										31
388	PGMA2B[7:0]										32
389	PGMA3B[7:0]										33
390	PGMA4B[7:0]										34
391	PGMA5B[7:0]									GROUP31	page9 35
392	PGMA6B[7:0]										36
393	PGMA7B[7:0]										37
394	PGMA8B[7:0]										38
395	PGMA9B[7:0]										39

396	PGMA10B[7:0]											3a
397	PGMA11B[7:0]											3b
398	PGMA12B[7:0]											3c
399	PGMA13B[7:0]											3d
400	PGMA14B[7:0]											3e
401	PGMA15B[7:0]											3f
402	PGMA16B[7:0]											40
403	PGMA17B[7:0]											41
404	PGMA18B[7:0]											42
405	PGMA19B[7:0]											43
406	PGMA20B[7:0]											44
407	PGMA21B[7:0]											45
408	PGMA22B[7:0]											46
409	PGMA23B[7:0]											47
410	PGMA24B[7:0]											48
411	PGMA1B[9:8]		PGMA2B[9:8]		PGMA3B[9:8]		PGMA4B[9:8]					49
412	PGMA5B[9:8]		PGMA6B[9:8]		PGMA7B[9:8]		PGMA8B[9:8]					4a
413	PGMA9B[9:8]		PGMA10B[9:8]		PGMA11B[9:8]		PGMA12B[9:8]					4b
414	PGMA13B[9:8]		PGMA14B[9:8]		PGMA15B[9:8]		PGMA16B[9:8]					4c
415	PGMA17B[9:8]		PGMA18B[9:8]		PGMA19B[9:8]		PGMA20B[9:8]					4d
416	PGMA21B[9:8]		PGMA22B[9:8]		PGMA23B[9:8]		PGMA24B[9:8]					4e
417	W1	-	-	-	-	-	-	-				-
418	NGMA1R[7:0]											31
419	NGMA2R[7:0]											32
420	NGMA3R[7:0]											33
421	NGMA4R[7:0]											34
422	NGMA5R[7:0]											35
423	NGMA6R[7:0]											36
424	NGMA7R[7:0]											37
425	NGMA8R[7:0]											38
426	NGMA9R[7:0]											39
427	NGMA10R[7:0]											3a
428	NGMA11R[7:0]											3b
429	NGMA12R[7:0]										GROUP32	page10	3c
430	NGMA13R[7:0]											3d
431	NGMA14R[7:0]											3e
432	NGMA15R[7:0]											3f
433	NGMA16R[7:0]											40
434	NGMA17R[7:0]											41
435	NGMA18R[7:0]											42
436	NGMA19R[7:0]											43
437	NGMA20R[7:0]											44
438	NGMA21R[7:0]											45
439	NGMA22R[7:0]											46
440	NGMA23R[7:0]											47
441	NGMA24R[7:0]											48

442	NGMA1R[9:8]		NGMA2R[9:8]		NGMA3R[9:8]		NGMA4R[9:8]					49
443	NGMA5R[9:8]		NGMA6R[9:8]		NGMA7R[9:8]		NGMA8R[9:8]					4a
444	NGMA9R[9:8]		NGMA10R[9:8]		NGMA11R[9:8]		NGMA12R[9:8]					4b
445	NGMA13R[9:8]		NGMA14R[9:8]		NGMA15R[9:8]		NGMA16R[9:8]					4c
446	NGMA17R[9:8]		NGMA18R[9:8]		NGMA19R[9:8]		NGMA20R[9:8]					4d
447	NGMA21R[9:8]		NGMA22R[9:8]		NGMA23R[9:8]		NGMA24R[9:8]					4e
448	W1	-	-	-	-	-	-	-				-
449	NGMA1G[7:0]											31
450	NGMA2G[7:0]											32
451	NGMA3G[7:0]											33
452	NGMA4G[7:0]											34
453	NGMA5G[7:0]											35
454	NGMA6G[7:0]											36
455	NGMA7G[7:0]											37
456	NGMA8G[7:0]											38
457	NGMA9G[7:0]											39
458	NGMA10G[7:0]											3a
459	NGMA11G[7:0]											3b
460	NGMA12G[7:0]											3c
461	NGMA13G[7:0]											3d
462	NGMA14G[7:0]											3e
463	NGMA15G[7:0]										GROUP33	page11	3f
464	NGMA16G[7:0]											40
465	NGMA17G[7:0]											41
466	NGMA18G[7:0]											42
467	NGMA19G[7:0]											43
468	NGMA20G[7:0]											44
469	NGMA21G[7:0]											45
470	NGMA22G[7:0]											46
471	NGMA23G[7:0]											47
472	NGMA24G[7:0]											48
473	NGMA1G[9:8]		NGMA2G[9:8]		NGMA3G[9:8]		NGMA4G[9:8]					49
474	NGMA5G[9:8]		NGMA6G[9:8]		NGMA7G[9:8]		NGMA8G[9:8]					4a
475	NGMA9G[9:8]		NGMA10G[9:8]		NGMA11G[9:8]		NGMA12G[9:8]					4b
476	NGMA13G[9:8]		NGMA14G[9:8]		NGMA15G[9:8]		NGMA16G[9:8]					4c
477	NGMA17G[9:8]		NGMA18G[9:8]		NGMA19G[9:8]		NGMA20G[9:8]					4d
478	NGMA21G[9:8]		NGMA22G[9:8]		NGMA23G[9:8]		NGMA24G[9:8]					4e
479	W1	-	-	-	-	-	-	-				-
480	NGMA1B[7:0]											31
481	NGMA2B[7:0]											32
482	NGMA3B[7:0]										GROUP34	page12	33
483	NGMA4B[7:0]											34
484	NGMA5B[7:0]											35
485	NGMA6B[7:0]											36

486	NGMA7B[7:0]						37
487	NGMA8B[7:0]						38
488	NGMA9B[7:0]						39
489	NGMA10B[7:0]						3a
490	NGMA11B[7:0]						3b
491	NGMA12B[7:0]						3c
492	NGMA13B[7:0]						3d
493	NGMA14B[7:0]						3e
494	NGMA15B[7:0]						3f
495	NGMA16B[7:0]						40
496	NGMA17B[7:0]						41
497	NGMA18B[7:0]						42
498	NGMA19B[7:0]						43
499	NGMA20B[7:0]						44
500	NGMA21B[7:0]						45
501	NGMA22B[7:0]						46
502	NGMA23B[7:0]						47
503	NGMA24B[7:0]						48
504	NGMA1B[9:8]	NGMA2B[9:8]	NGMA3B[9:8]	NGMA4B[9:8]			49
505	NGMA5B[9:8]	NGMA6B[9:8]	NGMA7B[9:8]	NGMA8B[9:8]			4a
506	NGMA9B[9:8]	NGMA10B[9:8]	NGMA11B[9:8]	NGMA12B[9:8]			4b
507	NGMA13B[9:8]	NGMA14B[9:8]	NGMA15B[9:8]	NGMA16B[9:8]			4c
508	NGMA17B[9:8]	NGMA18B[9:8]	NGMA19B[9:8]	NGMA20B[9:8]			4d
509	NGMA21B[9:8]	NGMA22B[9:8]	NGMA23B[9:8]	NGMA24B[9:8]			4e
510	W1	VENDER_ID[6:0]			GROUP35	page0	31
511	W2	VENDER_ID[6:0]				page0	31

11. Gamma Adjustment Function

11.1 Gamma voltage generator for source driver

The HX8279-D01 incorporates digital gamma adjustment function. Gamma adjustment operation is implemented by deciding the 10bit levels firstly in digital gamma adjustment control registers then dithering 8bit data to match the LCD panel. These registers are available for both polarities per RGB.

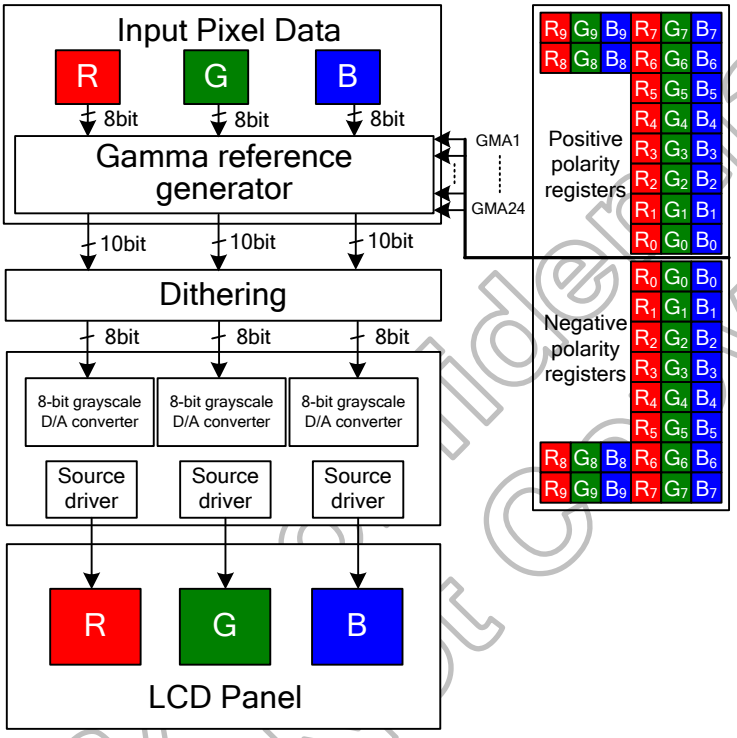
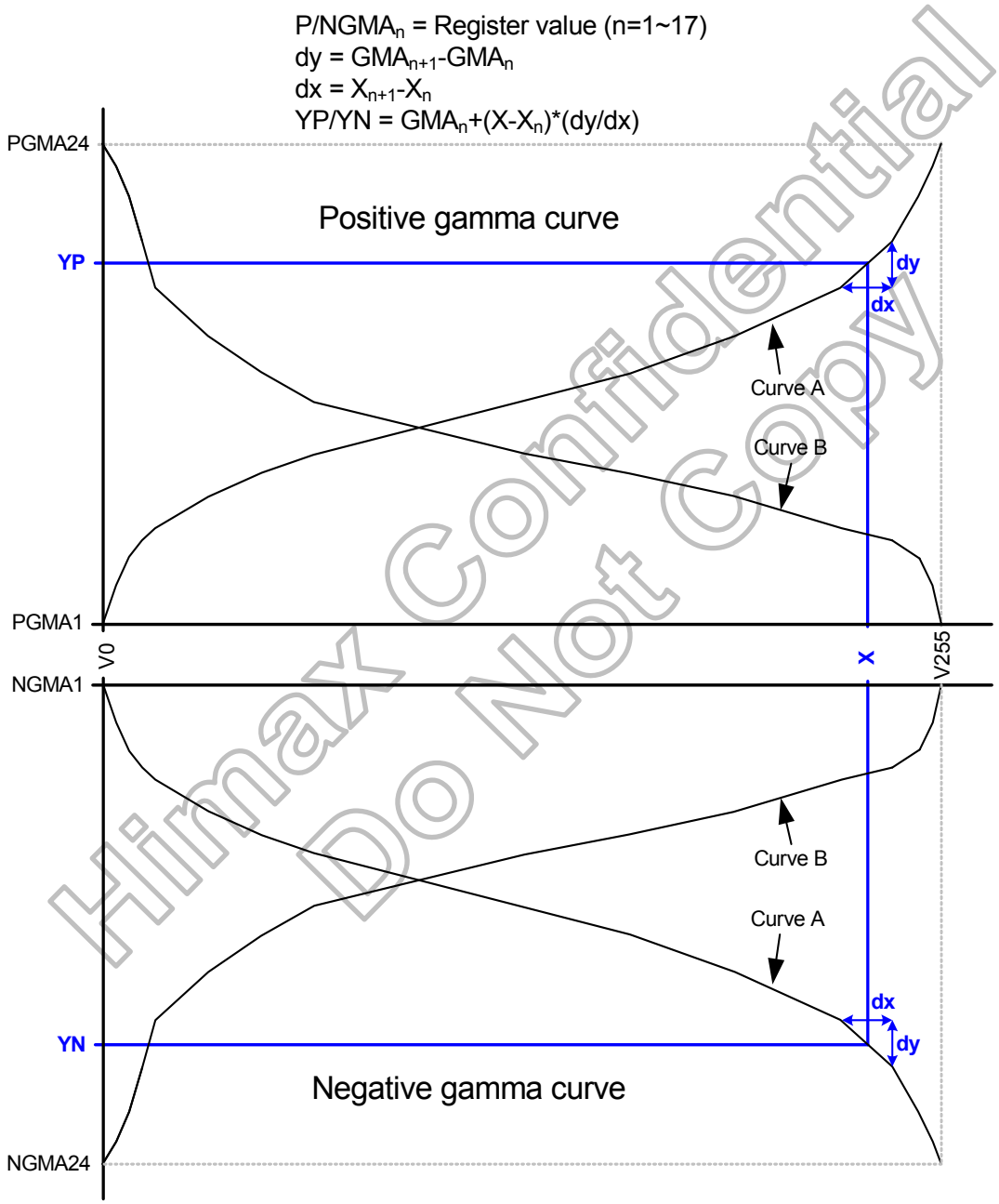


Figure 11.1: Grayscale control

11.2 Digital gamma curve adjustment

The gamma correction are done by 24-segment piecewise linear interpolation. The 24 segments are defined with 24 register values for level 0, 1, 3, 7, 11, 15, 23, 31, 47, 63, 95, 127, 128, 160, 192, 208, 224, 232, 240, 244, 248, 252, 254 and 255. These 24 register values defined the positive and negative gamma curve and RGB data. The gamma correction output data is then fed to 10-bit data to TCON dithering IP then generates 8-bit DAC and OP to drive the source lines on the panel.



Note: (1) Curve A is for normal black panel. Curve B is for normal white panel.

Figure 11.2: Digital gamma curve adjustment

11.3 Gamma reference voltage generator

The block consists of two gamma resister streams, one is for positive polarity and the other is for negative polarity. Gamma high/low voltage can be adjusted by VGPH, VGPL, VGNH, and VGNL.The gamma correction is done by 17 reference voltages. The 17 reference voltages are defined with 17 register values for level 0, 4, 8, 16, 28, 40, 56, 80, 128, 176, 200, 216, 228, 240, 248, 252 and 255.

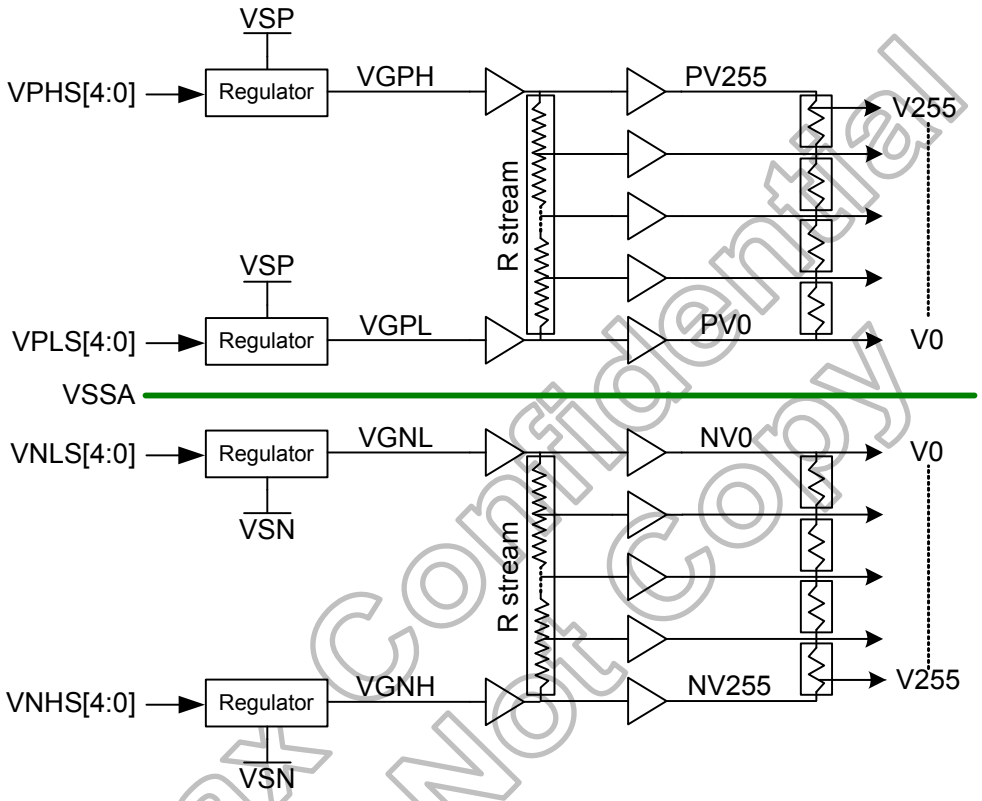


Figure 11.3: Gamma reference voltage generator diagram

11.4 Gamma table

Positive/Negative gamma resistor rate (Ω)															
R1	1.25	R33	2	R65	1.25	R97	1.1	R129	1.05	R161	1.25	R193	1.625	R225	2.75
R2	4.75	R34	2	R66	1.25	R98	1.1	R130	1.05	R162	1.25	R194	1.625	R226	3
R3	4.75	R35	2	R67	1.25	R99	1.1	R131	1.05	R163	1.25	R195	1.625	R227	3
R4	4.75	R36	2	R68	1.25	R100	1.1	R132	1.05	R164	1.25	R196	1.625	R228	3
R5	4.75	R37	2	R69	1.208	R101	1.05	R133	1.1	R165	1.333	R197	1.75	R229	3
R6	7.75	R38	2	R70	1.208	R102	1.05	R134	1.1	R166	1.333	R198	1.75	R230	3
R7	7.75	R39	2	R71	1.208	R103	1.05	R135	1.1	R167	1.333	R199	1.75	R231	3
R8	6.5	R40	2	R72	1.208	R104	1.05	R136	1.1	R168	1.333	R200	1.75	R232	3
R9	6.5	R41	1.833	R73	1.208	R105	1	R137	1.1875	R169	1.333	R201	1.75	R233	3.5
R10	4.25	R42	1.833	R74	1.208	R106	1	R138	1.1875	R170	1.333	R202	1.75	R234	3.5
R11	4.25	R43	1.833	R75	1.208	R107	1	R139	1.1875	R171	1.333	R203	1.75	R235	3.5
R12	5.5	R44	1.833	R76	1.208	R108	1	R140	1.1875	R172	1.333	R204	1.75	R236	3.5
R13	5.5	R45	1.75	R77	1.208	R109	1	R141	1.208	R173	1.375	R205	1.8333	R237	3.5
R14	4.25	R46	1.75	R78	1.208	R110	1	R142	1.208	R174	1.375	R206	1.8333	R238	3.5
R15	4	R47	1.75	R79	1.208	R111	1	R143	1.208	R175	1.375	R207	1.8333	R239	3.5
R16	3.25	R48	1.75	R80	1.208	R112	1	R144	1.208	R176	1.375	R208	1.8333	R240	4
R17	3.25	R49	1.625	R81	1.208	R113	1	R145	1.208	R177	1.5	R209	2	R241	4.75
R18	3.25	R50	1.625	R82	1.208	R114	1	R146	1.208	R178	1.5	R210	2	R242	4.75
R19	3.25	R51	1.625	R83	1.208	R115	1	R147	1.208	R179	1.5	R211	2	R243	4.2
R20	3.25	R52	1.625	R84	1.208	R116	1	R148	1.208	R180	1.5	R212	2	R244	4.25
R21	3.25	R53	1.5	R85	1.208	R117	1	R149	1.208	R181	1.5	R213	2.125	R245	6
R22	3.25	R54	1.5	R86	1.208	R118	1	R150	1.208	R182	1.5	R214	2.125	R246	6
R23	3.25	R55	1.5	R87	1.208	R119	1	R151	1.208	R183	1.5	R215	2.125	R247	6
R24	2.75	R56	1.5	R88	1.208	R120	1	R152	1.208	R184	1.5	R216	2.125	R248	6
R25	2.75	R57	1.375	R89	1.125	R121	1	R153	1.208	R185	1.5	R217	2.25	R249	7
R26	2.75	R58	1.375	R90	1.125	R122	1	R154	1.208	R186	1.5	R218	2.25	R250	7
R27	2.75	R59	1.375	R91	1.125	R123	1	R155	1.208	R187	1.5	R219	2.25	R251	9
R28	2.75	R60	1.375	R92	1.125	R124	1	R156	1.208	R188	1.5	R220	2.25	R252	9
R29	2.75	R61	1.333	R93	1.125	R125	1	R157	1.25	R189	1.5	R221	2.333	R253	15.5
R30	2.5	R62	1.333	R94	1.125	R126	1	R158	1.25	R190	1.5	R222	2.333	R254	15.5
R31	2.5	R63	1.333	R95	1.125	R127	1	R159	1.25	R191	1.5	R223	2.333	R255	38.25
R32	2.25	R64	1.333	R96	1.125	R128	1	R160	1.25	R192	1.5	R224	2.333		

Note: (1) 8.5Ω/unit.

12. DC Characteristics

12.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply power voltage	VDD	-0.30	-	2.1	V
VSP voltage	VSP	-0.30	-	6.60	V
VSN voltage	VSN	-6.60	-	0.30	V
VPP **(OTP power)**	VPP	-	-	9.0	V
VGH voltage	VGH	-0.30	-	VGL+32V	V
VGL voltage	VGL	VGH-32V	-	0.30	V
Operating Temperature	T_{OPR}	-20	-	+85	℃
Storage temperature	T_{STG}	-55	-	125	℃

12.2 Typical operating condition

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply power voltage	VDD	1.7	1.8	2.0	V
VSP voltage	VSP	4.5	-	6.0	V
VSN voltage	VSN	-4.5	-	-6.0	V
VGH voltage(external VGH)	VGH_EXT	8.7	-	20	V
VGL voltage(external VGL)	VGL_EXT	-18	-	-6.7	V
VGH voltage(internal VGH)	VGH_INT	8.7	-	18	V
VGL voltage(internal VGL)	VGL_INT	-16	-	-6.7	V
VPP **(OTP power)**	VPP	8.0	8.25	8.5	V

12.3 DC electrical characteristics

(Test condition: VDD=1.7~2.0V, T_{OPR} =-20℃~+85℃,VSS=VSSA=VSS_IF=0V)

Parameter		Symbol	Spec.			Unit	Note
			Min.	Typ.	Max.		
VDD input high level voltage		VIH1	0.8 x VDD	-	VDD	V	-
VDD input low level voltage		VIL1	VSS	-	0.2 x VDD	V	-
VCC input high level voltage		VIH2	0.8 x VCC	-	VCC	V	-
VCC input low level voltage		VIL2	VSS	-	0.2 x VCC	V	-
Input leakage current		IL1	-1	-	+1	μA	-
SDAO output high level voltage		VOH	0.8 x VDD	-	VDD	V	-
SDAO output low level voltage		VOL	VSS	-	0.2 x VDD	V	-
VLPH output voltage		VLPH	1.1	1.2	1.4	V	$I_{(VLPH)}$<10mA
VCL output voltage		VCL	-2.1	-2.4	-3.00	V	$I_{(VCORE)}$<60mA
VGH output voltage		VGH	8.7	-	18	V	$I_{(VGH)}$<5mA
VGL output voltage		VGL	-16	-	-6.7	V	$I_{(VGL)}$<5mA
VGPH output voltage		VGPH	4.0	4.5	5.5	V	-
VGPL output voltage		VGPL	0.1	0.2	1.6	V	-
VGNH output voltage		VGNH	-5.5	-4.5	-4.0	V	-
VGNL output voltage		VGNL	-1.6	-0.2	-0.1	V	-
Driving current of GOUT outputs		IGOS	1	-	-	mA	GOUT1~20 VO=15V vs 14.7V VGH=15V,VGL=-13V
Sinking current of GOUT outputs		IGOD	1	-	-	mA	GOUT1~20 VO=-13V vs -12.7V VGH=15V,VGL=-13V
VCOM output voltage		VCOM	-2.75	-	-0.20	V	-
Input terminal pull-high resistance		RPU	-	300	-	KΩ	VDD=1.8V
Input terminal pull-low resistance		RPD	-	300	-	KΩ	
Source output level deviation	Gray code= 0 ~ 14 Gray code= 241 ~ 255	-	-	-	40	mV	-
	Gray code= 15 ~ 31 Gray code= 208 ~ 240	-	-	-	30	mV	
	Gray code= 32 ~ 207	-	-	-	20	mV	
Source output offset deviation	Gray code= 0 ~ 14 Gray code= 241 ~ 255	-	-	-	50	mV	-
	Gray code= 15 ~ 31 Gray code= 208 ~ 240	-	-	-	40	mV	
	Gray code= 32 ~ 207	-	-	-	30	mV	
Withstanding current capability	IVDD capability	-	-	-	40	mA	-
	IVSP capability	-	-	-	50		
	IVSN capability	-	-	-	-50		
VSP current consumption	Standby mode	Ivsps	-	-	1.2	mA	Note(2)
	ULPS mode	Ivspu	-	-	6	μA	Note(3)
VSN current consumption	Standby mode	Ivsns	-	-	-0.15	mA	Note(2)
	ULPS mode	Ivsnu	-	-	-12	μA	Note(3)
VDD current consumption	Normal mode	Ivdd	-	-	30	mA	Note(1)
	Standby mode	Ivdds	-	-	1.1	mA	Note(2)
	ULPS mode	Ivddu	-	-	150	μA	Note(3)
VPP operation current		I_{VPP}	-	-	8	mA	-

Note: (1) Condition: one chip current ,VDD=1.8V, 25℃,1200RGBx1920 resolution ,MIPI frequency 950mbps,frame rate 60Hz, all setting are default.

(2) Condition: one chip current, VDD=1.8V,25℃,all function and MIPI input stop. And let MIPI input state keep ULPS to reduce more current consumption in standby mode.

(3) Conditon: one chip current,VDD=1.8V,VSP=5.5V,VSN=-5.5V 25℃

12.4 MIPI DC characteristics

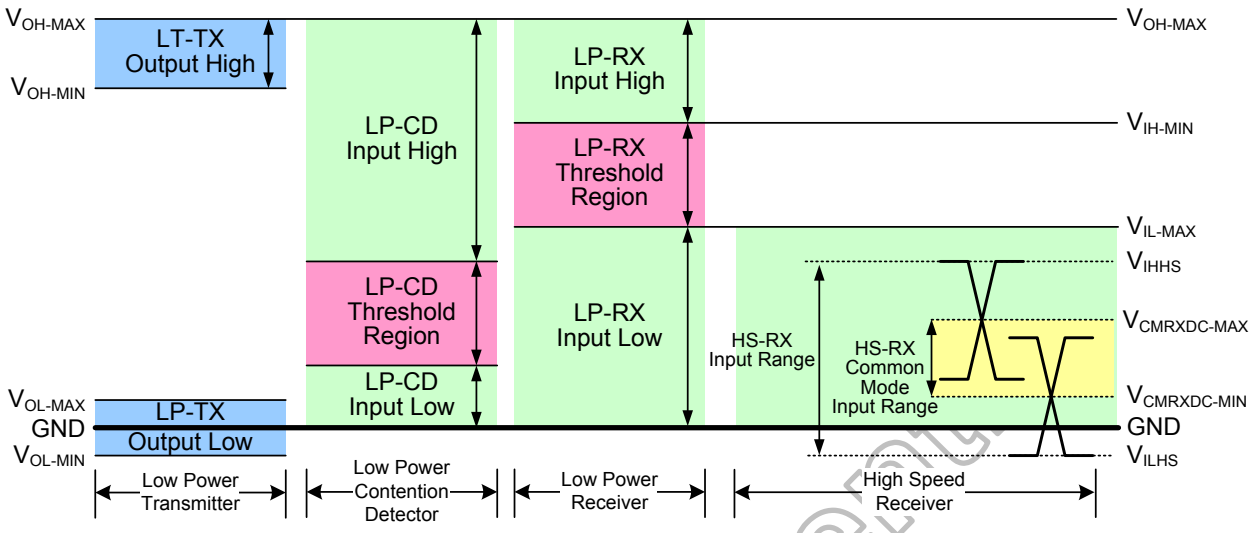


Figure 12.1: MIPI signaling and contention voltage levels

DC characteristics for MIPI LP mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic 1 input voltage	V_{IH}	880	-	-	mV
Logic 0 input voltage	V_{IL}	0	-	550	mV
Logic 1 output voltage	V_{OH}	1.1	1.2	1.3	V
Logic 0 output voltage	V_{OL}	-50	-	50	mV

DC characteristics for MIPI HS mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Common-mode voltage HS Receive mode	V_{CMRXDC}	70	-	330	mV
Differential input high threshold(1)	V_{IDTH}	-	-	70	mV
Differential input low threshold(1)	V_{IDTL}	-70	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Differential input impedance	Z_{ID}	80	100	125	Ω
HS transmit differential voltage **(VDP-VDN)**	|VOD|	140	200	270	mV

Note: (1) V_{IDTH} and V_{IDTL} only for reference, related to power and ground noise, this spec need to check on panel performance to fine tune

13. AC Characteristics

13.1 MIPI AC characteristics

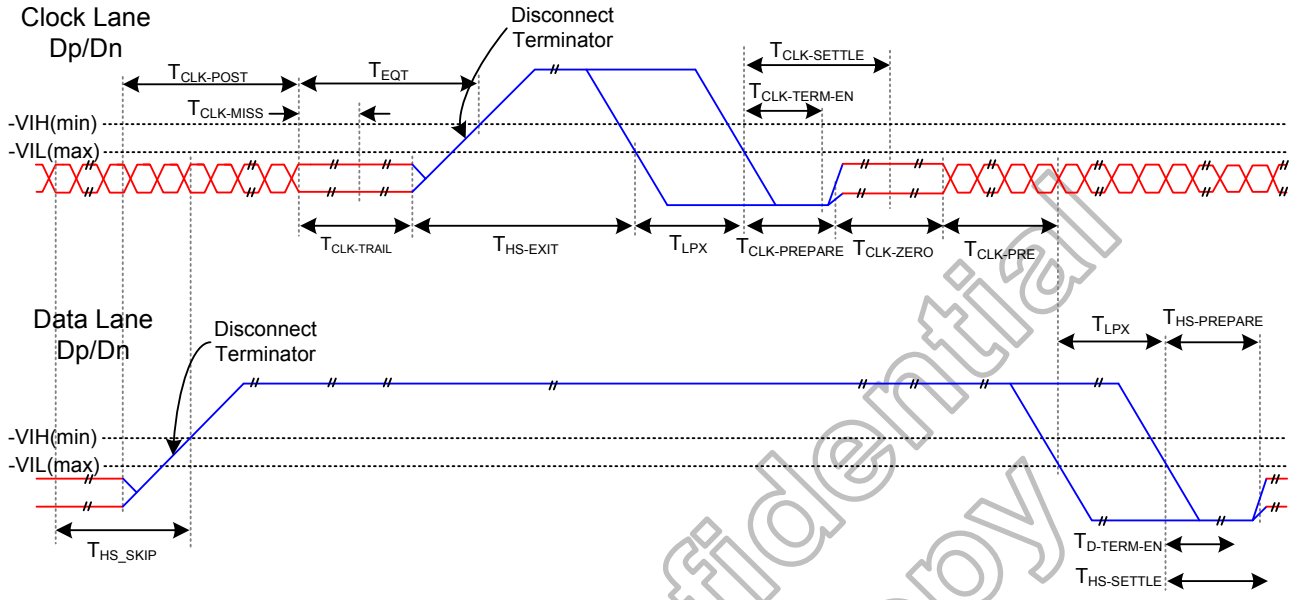


Figure 13.1: Switching the clock lane between clock transmission and low-power mode

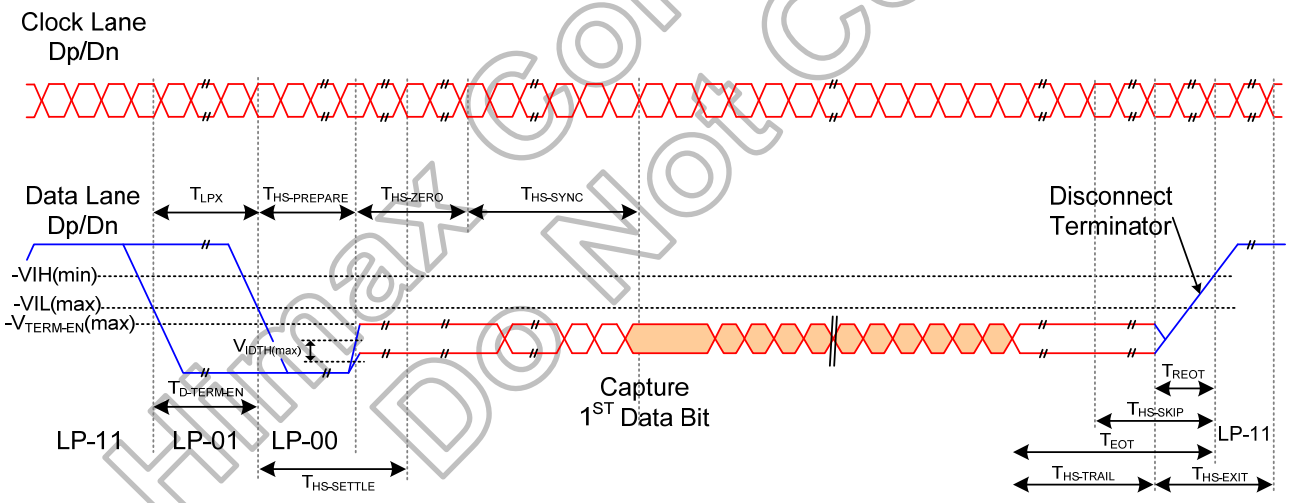


Figure 13.2: Timing of high-speed data transmission in bursts

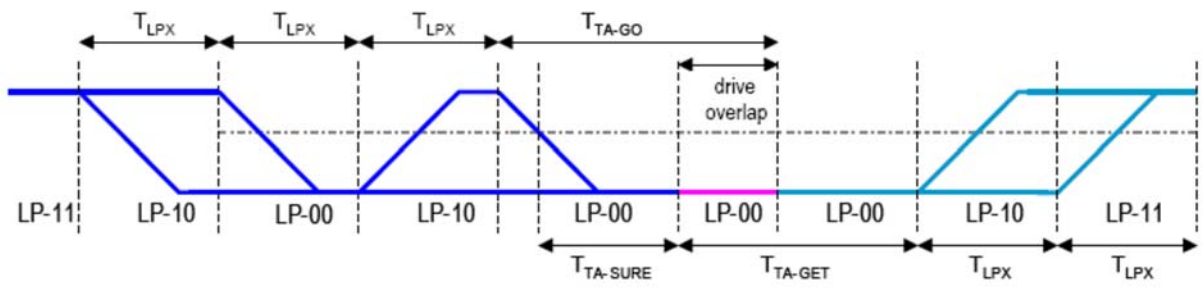


Figure 13.3: Turnaround Procedure

MIPI AC Characteristics

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI **(For DCS)**	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI		145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$(1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}$/$T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	5*T_{LPX}			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	4*T_{LPX}			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	2*T_{LPX}	ns

Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

13.2 MIPI data-clock timing specification

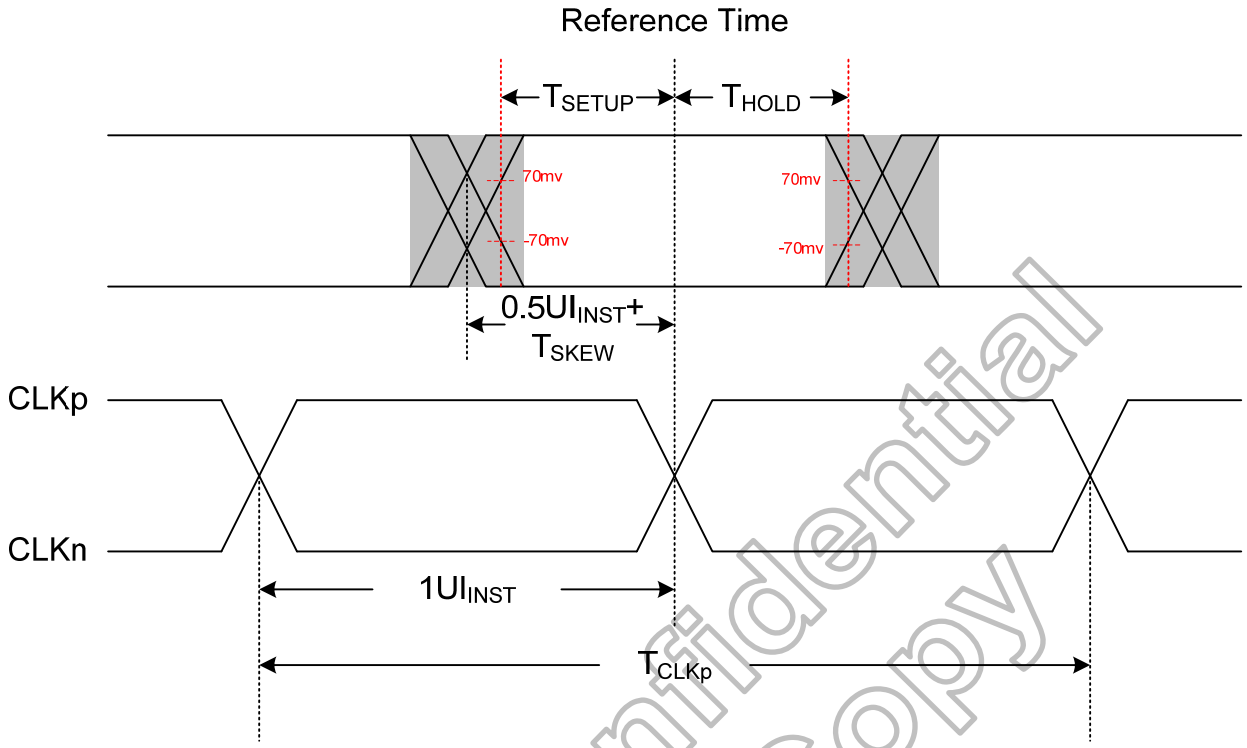
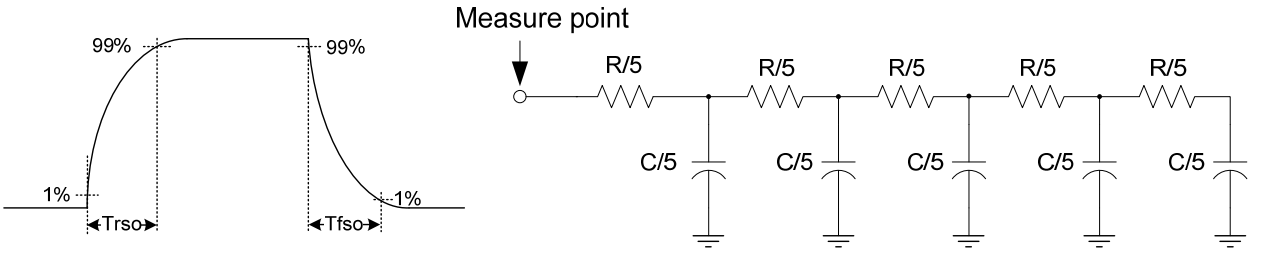


Figure 13.4: Data to clock timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
UI instantaneous	UI_{INST}	1.0	-	12.5(1)	ns
Data to clock setup time	T_{SETUP}	0.15	-	-	UI_{INST}
Data to clock hold time	T_{HOLD}	0.15	-	-	UI_{INST}

Note: (1) This value corresponds to a minimum 80 Mbps data rate.

13.3 Source output timing

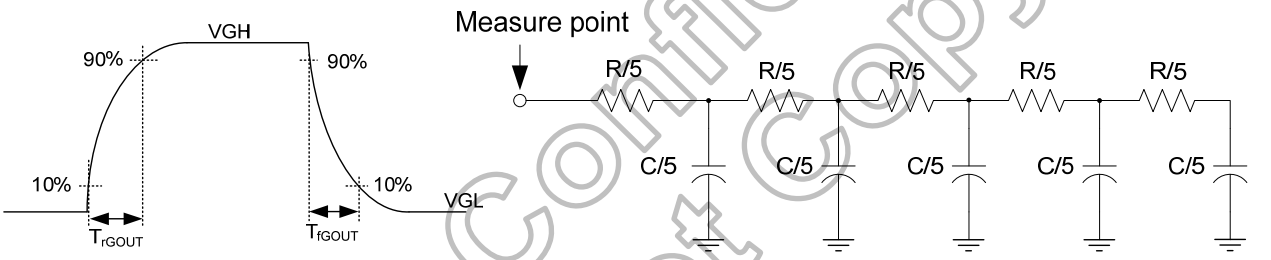


Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Source driver rising time	trSO	Load R=7.94KΩ, Load C = 85.84pF, Voltage: -5V←→5V VSN=-5.1V, VSP=5.1V	-	-	6.0	μs
Source driver falling time	tfSO		-	-	6.0	μs

Note: (1) Himax can support simulation for customer design.

Table 13.1: Source output timing

Panel control signal output 1 **(GOUT1_L~GOUT20_L, GOUT1_R~GOUT20_R)**

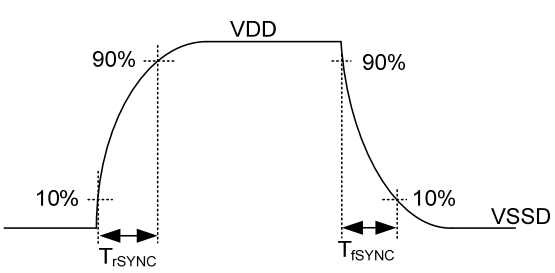


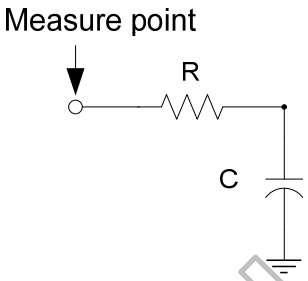
Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Panel control signal rising time	T_{rGOUT}	LOAD R=1780Ω LOAD C=1273pF VGH=+16V, VGL=-16.0V	-	-	5	μs
Panel control signal falling time	T_{fGOUT}		-	-	5	μs

Note: (1) Himax can support simulation for customer design.

Table 13.2: GOA output timing

Panel control signal output 2 **(SYNC1_L~ SYNC8_L, SYNC1_R~ SYNC8_R)**





Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Panel synchronization signal rising time	T_{rSYNC}	LOAD R = 1KΩ	-	-	60	ns
Panel synchronization signal falling time	T_{fSYNC}	LOAD C = 40pF	-	-	60	ns

Note: (1) Himax can support simulation for customer design.

Table 13.3: Synchronization signals output timing

13.4 Serial interface characteristics

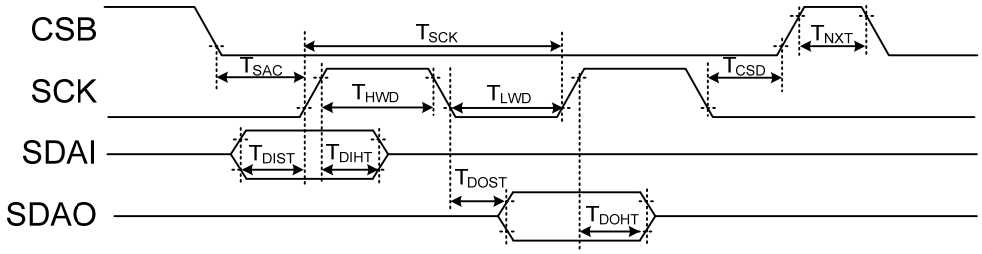


Figure 13.5: Serial interface characteristics

(VSS=0V, VDD=1.7~2.0V, T_{OPR} =-20 to 85℃)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
CSB assertion to first clock edge	T_{SAC}	-	120	-	-	ns
CSB reassertion from last clock edge	T_{CSD}	-	120	-	-	ns
CSB next control enable	T_E	-	200	-	-	ns
SCK period time	T_{SCK}	-	200	-	-	ns
SCK high period time	T_{HWD}	-	100	-	-	ns
SCK low period time	T_{LWD}	-	100	-	-	ns
SDAI input data setup time	T_{DIST}	-	50	-	-	ns
SDAI input data hold time	T_{DIHT}	-	50	-	-	ns
SDAO output data setup time	T_{DOST}	-	60	-	100	ns
SDAO output data hold time	T_{DOHT}	-	60	-	100	ns

Table 13.4: AC characteristic of SPI interface

13.5 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of low can be shown as the following.

(VDD=1.7V~2.0V, VSS=0V, T_{OPR} =-20℃~+85℃)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Reset low pulse width	Trst	-	20	-	-	μs

Table 13.5: Reset timing

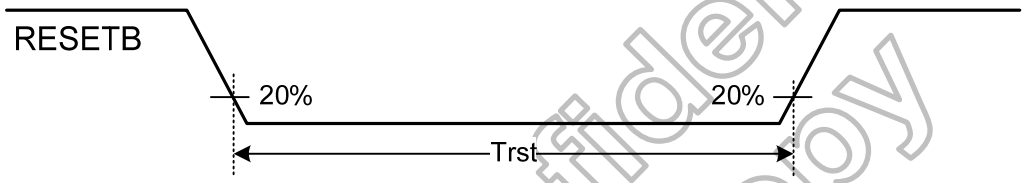
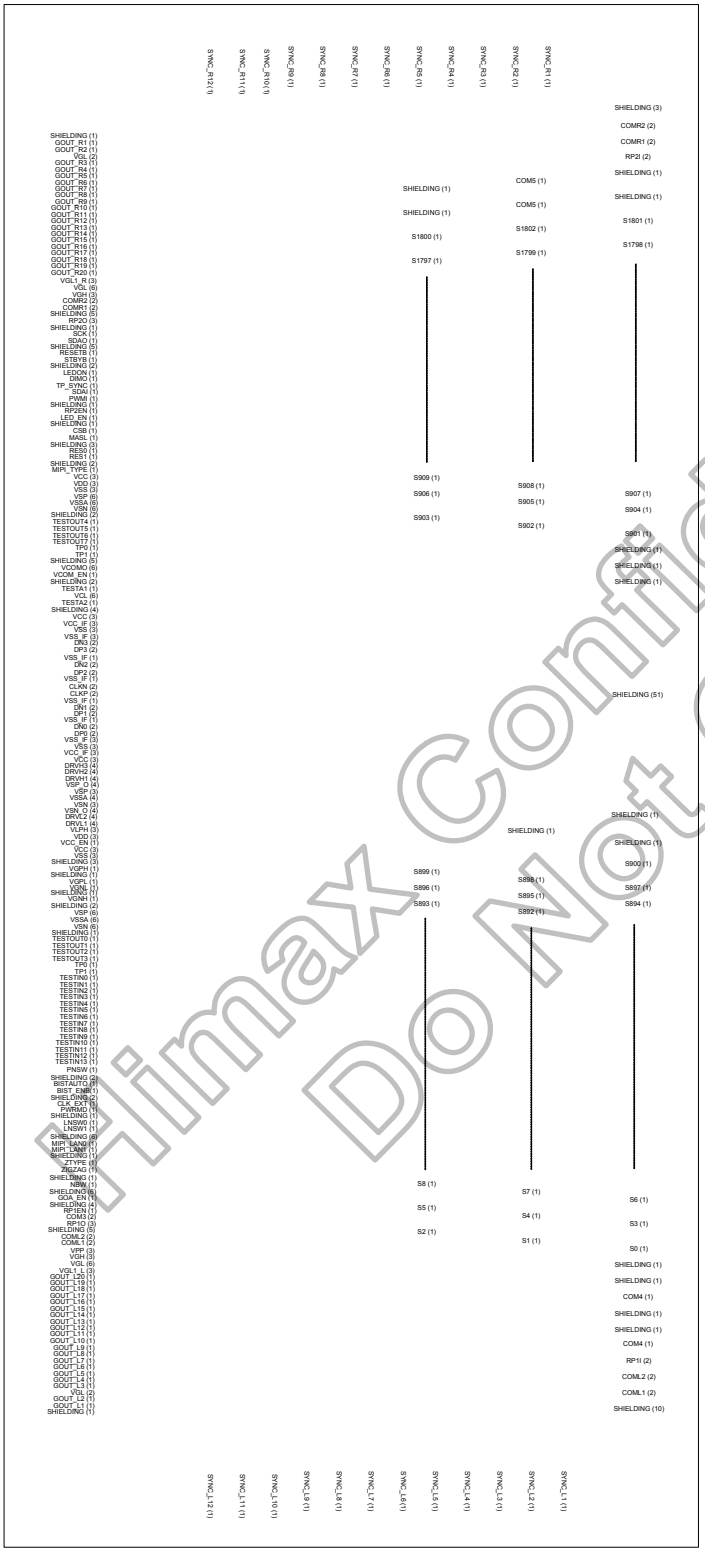


Figure 13.6: Reset timing

14. Pin Assignment (IC Face View)

14.1 Pad sequence



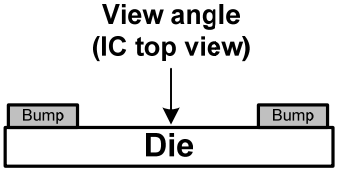
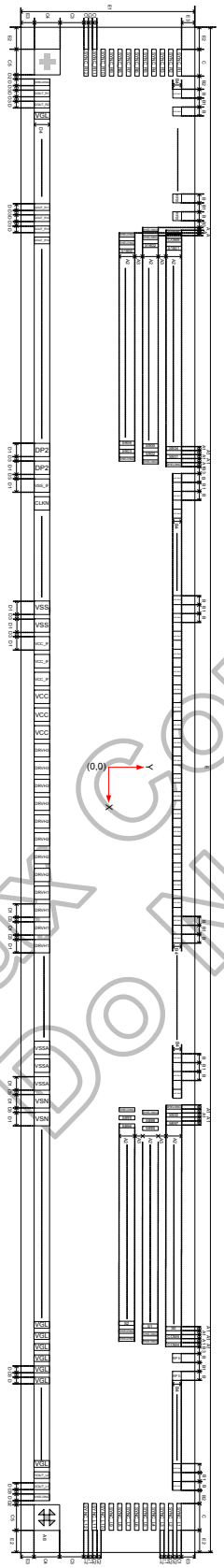


Figure 14.1: Pad sequence

14.2 Bump information

14.2.1 Chip outline dimensions



Chip size (w/o scribe line): 28420um x 695um
Chip size (w/i scribe line): 28500um x 775um
Bump height: 12um (+/-3um)
Bump hardness: 80HV (+/-20HV)
Total bump area: 3910060 um^2

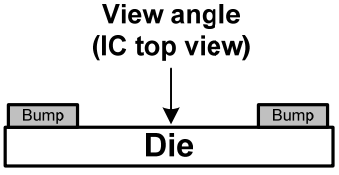


Figure 14.2: Chip outline dimensions

14.2.2 Pad information

(Unit: μm)

Symbol	Dimension
A	12
A1	18
A2	70
A3	35
B	40
B1	40
B2	59
B3	31
B4	40
C	120
C1	20
C2	18
C3	108
C4	115
C5	115
D	30
D1	60
D2	18
D3	20
D4	70
E	28500 **(max.)**
E1	775 **(max.)**
E2	97 **(max.)**
E3	57 **(max.)**

14.2.3 Alignment mark

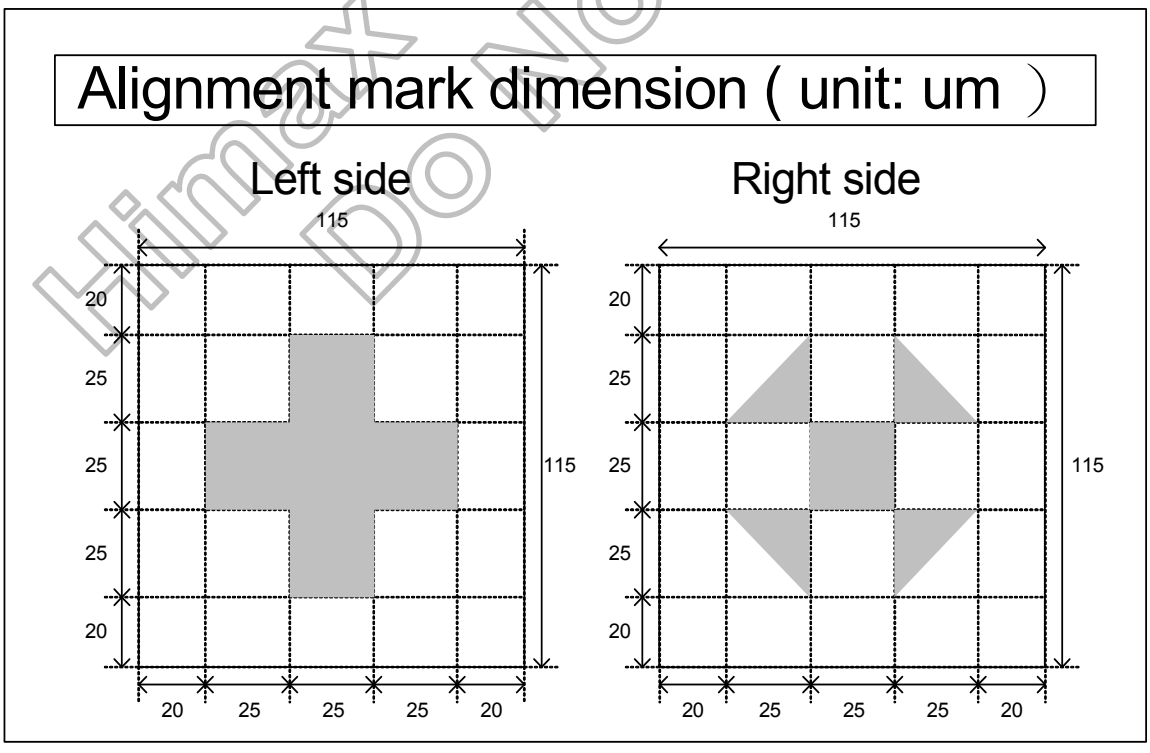


Figure 14.3: Alignment mark

14.3 Pad coordinates

(Unit: μm)

No.	Name	X	Y	Bump size
1	SHIELDING	-14005	-295.5	30x70
2	GOUT_R1	-13955	-295.5	30x70
3	GOUT_R2	-13905	-295.5	30x70
4	VGL	-13855	-295.5	30x70
5	VGL	-13805	-295.5	30x70
6	GOUT_R3	-13755	-295.5	30x70
7	GOUT_R4	-13705	-295.5	30x70
8	GOUT_R5	-13655	-295.5	30x70
9	GOUT_R6	-13605	-295.5	30x70
10	GOUT_R7	-13555	-295.5	30x70
11	GOUT_R8	-13505	-295.5	30x70
12	GOUT_R9	-13455	-295.5	30x70
13	GOUT_R10	-13405	-295.5	30x70
14	GOUT_R11	-13355	-295.5	30x70
15	GOUT_R12	-13305	-295.5	30x70
16	GOUT_R13	-13255	-295.5	30x70
17	GOUT_R14	-13205	-295.5	30x70
18	GOUT_R15	-13155	-295.5	30x70
19	GOUT_R16	-13105	-295.5	30x70
20	GOUT_R17	-13055	-295.5	30x70
21	GOUT_R18	-13005	-295.5	30x70
22	GOUT_R19	-12955	-295.5	30x70
23	GOUT_R20	-12905	-295.5	30x70
24	VGL1_R	-12855	-295.5	30x70
25	VGL1_R	-12805	-295.5	30x70
26	VGL1_R	-12755	-295.5	30x70
27	VGL	-12705	-295.5	30x70
28	VGL	-12655	-295.5	30x70
29	VGL	-12605	-295.5	30x70
30	VGL	-12555	-295.5	30x70
31	VGL	-12505	-295.5	30x70
32	VGL	-12455	-295.5	30x70
33	VGH	-12405	-295.5	30x70
34	VGH	-12355	-295.5	30x70
35	VGH	-12305	-295.5	30x70
36	COMR2	-12240	-295.5	60x70
37	COMR2	-12160	-295.5	60x70
38	COMR1	-12080	-295.5	60x70
39	COMR1	-12000	-295.5	60x70
40	SHIELDING	-11920	-295.5	60x70
41	SHIELDING	-11840	-295.5	60x70
42	SHIELDING	-11760	-295.5	60x70
43	SHIELDING	-11680	-295.5	60x70
44	SHIELDING	-11600	-295.5	60x70
45	RP2O	-11520	-295.5	60x70
46	RP2O	-11440	-295.5	60x70
47	RP2O	-11360	-295.5	60x70
48	SHIELDING	-11280	-295.5	60x70
49	SCK	-11200	-295.5	60x70
50	SDAO	-11120	-295.5	60x70
51	SHIELDING	-11040	-295.5	60x70
52	SHIELDING	-10960	-295.5	60x70
53	SHIELDING	-10880	-295.5	60x70
54	SHIELDING	-10800	-295.5	60x70
55	SHIELDING	-10720	-295.5	60x70
56	RESETB	-10640	-295.5	60x70
57	STBYB	-10560	-295.5	60x70
58	SHIELDING	-10480	-295.5	60x70
59	SHIELDING	-10400	-295.5	60x70
60	LEDON	-10320	-295.5	60x70
61	DIMO	-10240	-295.5	60x70
62	TP_SYNC	-10160	-295.5	60x70
63	SDAI	-10080	-295.5	60x70
64	PWMI	-10000	-295.5	60x70
65	SHIELDING	-9920	-295.5	60x70
66	RP2EN	-9840	-295.5	60x70
67	LED_EN	-9760	-295.5	60x70
68	SHIELDING	-9680	-295.5	60x70
69	CSB	-9600	-295.5	60x70
70	MASL	-9520	-295.5	60x70
71	SHIELDING	-9440	-295.5	60x70
72	SHIELDING	-9360	-295.5	60x70
73	SHIELDING	-9280	-295.5	60x70
74	RES0	-9200	-295.5	60x70
75	RES1	-9120	-295.5	60x70
76	SHIELDING	-9040	-295.5	60x70
77	SHIELDING	-8960	-295.5	60x70
78	MIPI_TYPE	-8880	-295.5	60x70
79	VCC	-8800	-295.5	60x70
80	VCC	-8720	-295.5	60x70
81	VCC	-8640	-295.5	60x70
82	VDD	-8560	-295.5	60x70
83	VDD	-8480	-295.5	60x70
84	VDD	-8400	-295.5	60x70
85	VSS	-8320	-295.5	60x70
86	VSS	-8240	-295.5	60x70
87	VSS	-8160	-295.5	60x70
88	VSP	-8080	-295.5	60x70
89	VSP	-8000	-295.5	60x70
90	VSP	-7920	-295.5	60x70
91	VSP	-7840	-295.5	60x70
92	VSP	-7760	-295.5	60x70
93	VSP	-7680	-295.5	60x70
94	VSSA	-7600	-295.5	60x70
95	VSSA	-7520	-295.5	60x70
96	VSSA	-7440	-295.5	60x70
97	VSSA	-7360	-295.5	60x70
98	VSSA	-7280	-295.5	60x70
99	VSSA	-7200	-295.5	60x70
100	VSN	-7120	-295.5	60x70
101	VSN	-7040	-295.5	60x70
102	VSN	-6960	-295.5	60x70
103	VSN	-6880	-295.5	60x70
104	VSN	-6800	-295.5	60x70
105	VSN	-6720	-295.5	60x70
106	SHIELDING	-6640	-295.5	60x70
107	SHIELDING	-6560	-295.5	60x70
108	TESTOUT4	-6480	-295.5	60x70
109	TESTOUT5	-6400	-295.5	60x70
110	TESTOUT6	-6320	-295.5	60x70
111	TESTOUT7	-6240	-295.5	60x70
112	TP0	-6160	-295.5	60x70
113	TP1	-6080	-295.5	60x70
114	SHIELDING	-6000	-295.5	60x70
115	SHIELDING	-5920	-295.5	60x70
116	SHIELDING	-5840	-295.5	60x70
117	SHIELDING	-5760	-295.5	60x70
118	SHIELDING	-5680	-295.5	60x70
119	VCOMO	-5600	-295.5	60x70
120	VCOMO	-5520	-295.5	60x70
121	VCOMO	-5440	-295.5	60x70
122	VCOMO	-5360	-295.5	60x70
123	VCOMO	-5280	-295.5	60x70
124	VCOMO	-5200	-295.5	60x70
125	VCOM_EN	-5120	-295.5	60x70
126	SHIELDING	-5040	-295.5	60x70
127	SHIELDING	-4960	-295.5	60x70
128	TESTA1	-4880	-295.5	60x70
129	VCL	-4800	-295.5	60x70
130	VCL	-4720	-295.5	60x70
131	VCL	-4640	-295.5	60x70
132	VCL	-4560	-295.5	60x70
133	VCL	-4480	-295.5	60x70
134	VCL	-4400	-295.5	60x70
135	TESTA2	-4320	-295.5	60x70
136	SHIELDING	-4240	-295.5	60x70
137	SHIELDING	-4160	-295.5	60x70
138	SHIELDING	-4080	-295.5	60x70
139	SHIELDING	-4000	-295.5	60x70
140	VCC	-3920	-295.5	60x70
141	VCC	-3840	-295.5	60x70
142	VCC	-3760	-295.5	60x70
143	VCC_IF	-3680	-295.5	60x70
144	VCC_IF	-3600	-295.5	60x70
145	VCC_IF	-3520	-295.5	60x70
146	VSS	-3440	-295.5	60x70
147	VSS	-3360	-295.5	60x70
148	VSS	-3280	-295.5	60x70
149	VSS_IF	-3200	-295.5	60x70
150	VSS_IF	-3120	-295.5	60x70
151	VSS_IF	-3040	-295.5	60x70
152	DN3	-2960	-295.5	60x70
153	DN3	-2880	-295.5	60x70
154	DP3	-2800	-295.5	60x70
155	DP3	-2720	-295.5	60x70
156	VSS_IF	-2640	-295.5	60x70
157	DN2	-2560	-295.5	60x70
158	DN2	-2480	-295.5	60x70
159	DP2	-2400	-295.5	60x70
160	DP2	-2320	-295.5	60x70
161	VSS_IF	-2240	-295.5	60x70
162	CLKN	-2160	-295.5	60x70
163	CLKN	-2080	-295.5	60x70
164	CLKP	-2000	-295.5	60x70
165	CLKP	-1920	-295.5	60x70
166	VSS_IF	-1840	-295.5	60x70
167	DN1	-1760	-295.5	60x70
168	DN1	-1680	-295.5	60x70
169	DP1	-1600	-295.5	60x70
170	DP1	-1520	-295.5	60x70
171	VSS_IF	-1440	-295.5	60x70
172	DN0	-1360	-295.5	60x70
173	DN0	-1280	-295.5	60x70
174	DP0	-1200	-295.5	60x70
175	DP0	-1120	-295.5	60x70
176	VSS_IF	-1040	-295.5	60x70
177	VSS_IF	-960	-295.5	60x70
178	VSS_IF	-880	-295.5	60x70
179	VSS	-800	-295.5	60x70
180	VSS	-720	-295.5	60x70
181	VSS	-640	-295.5	60x70
182	VCC_IF	-560	-295.5	60x70
183	VCC_IF	-480	-295.5	60x70
184	VCC_IF	-400	-295.5	60x70
185	VCC	-320	-295.5	60x70
186	VCC	-240	-295.5	60x70
187	VCC	-160	-295.5	60x70
188	DRVH3	-80	-295.5	60x70
189	DRVH3	0	-295.5	60x70
190	DRVH3	80	-295.5	60x70
191	DRVH3	160	-295.5	60x70
192	DRVH2	240	-295.5	60x70
193	DRVH2	320	-295.5	60x70
194	DRVH2	400	-295.5	60x70
195	DRVH2	480	-295.5	60x70
196	DRVH1	560	-295.5	60x70
197	DRVH1	640	-295.5	60x70
198	DRVH1	720	-295.5	60x70
199	DRVH1	800	-295.5	60x70
200	VSP_O	880	-295.5	60x70
201	VSP_O	960	-295.5	60x70
202	VSP_O	1040	-295.5	60x70
203	VSP_O	1120	-295.5	60x70
204	VSP	1200	-295.5	60x70
205	VSP	1280	-295.5	60x70
206	VSP	1360	-295.5	60x70
207	VSSA	1440	-295.5	60x70
208	VSSA	1520	-295.5	60x70
209	VSSA	1600	-295.5	60x70
210	VSSA	1680	-295.5	60x70
211	VSN	1760	-295.5	60x70
212	VSN	1840	-295.5	60x70
213	VSN	1920	-295.5	60x70
214	VSN_O	2000	-295.5	60x70
215	VSN_O	2080	-295.5	60x70
216	VSN_O	2160	-295.5	60x70
217	VSN_O	2240	-295.5	60x70
218	DRVL2	2320	-295.5	60x70
219	DRVL2	2400	-295.5	60x70
220	DRVL2	2480	-295.5	60x70
221	DRVL2	2560	-295.5	60x70
222	DRVL1	2640	-295.5	60x70
223	DRVL1	2720	-295.5	60x70
224	DRVL1	2800	-295.5	60x70
225	DRVL1	2880	-295.5	60x70
226	VLPH	2960	-295.5	60x70
227	VLPH	3040	-295.5	60x70
228	VLPH	3120	-295.5	60x70
229	VDD	3200	-295.5	60x70
230	VDD	3280	-295.5	60x70
231	VDD	3360	-295.5	60x70
232	VCC_EN	3440	-295.5	60x70
233	VCC	3520	-295.5	60x70
234	VCC	3600	-295.5	60x70
235	VCC	3680	-295.5	60x70
236	VSS	3760	-295.5	60x70
237	VSS	3840	-295.5	60x70
238	VSS	3920	-295.5	60x70
239	SHIELDING	4000	-295.5	60x70
240	SHIELDING	4080	-295.5	60x70

No.	Name	X	Y	Bump size
241	SHIELDING	4160	-295.5	60x70
242	VGPH	4240	-295.5	60x70
243	SHIELDING	4320	-295.5	60x70
244	VGPL	4400	-295.5	60x70
245	VGNL	4480	-295.5	60x70
246	SHIELDING	4560	-295.5	60x70
247	VGNH	4640	-295.5	60x70
248	SHIELDING	4720	-295.5	60x70
249	SHIELDING	4800	-295.5	60x70
250	VSP	4880	-295.5	60x70
251	VSP	4960	-295.5	60x70
252	VSP	5040	-295.5	60x70
253	VSP	5120	-295.5	60x70
254	VSP	5200	-295.5	60x70
255	VSP	5280	-295.5	60x70
256	VSSA	5360	-295.5	60x70
257	VSSA	5440	-295.5	60x70
258	VSSA	5520	-295.5	60x70
259	VSSA	5600	-295.5	60x70
260	VSSA	5680	-295.5	60x70
261	VSSA	5760	-295.5	60x70
262	VSN	5840	-295.5	60x70
263	VSN	5920	-295.5	60x70
264	VSN	6000	-295.5	60x70
265	VSN	6080	-295.5	60x70
266	VSN	6160	-295.5	60x70
267	VSN	6240	-295.5	60x70
268	SHIELDING	6320	-295.5	60x70
269	TESTOUT0	6400	-295.5	60x70
270	TESTOUT1	6480	-295.5	60x70
271	TESTOUT2	6560	-295.5	60x70
272	TESTOUT3	6640	-295.5	60x70
273	TP0	6720	-295.5	60x70
274	TP1	6800	-295.5	60x70
275	TESTIN0	6880	-295.5	60x70
276	TESTIN1	6960	-295.5	60x70
277	TESTIN2	7040	-295.5	60x70
278	TESTIN3	7120	-295.5	60x70
279	TESTIN4	7200	-295.5	60x70
280	TESTIN5	7280	-295.5	60x70
281	TESTIN6	7360	-295.5	60x70
282	TESTIN7	7440	-295.5	60x70
283	TESTIN8	7520	-295.5	60x70
284	TESTIN9	7600	-295.5	60x70
285	TESTIN10	7680	-295.5	60x70
286	TESTIN11	7760	-295.5	60x70
287	TESTIN12	7840	-295.5	60x70
288	TESTIN13	7920	-295.5	60x70
289	PNSW	8000	-295.5	60x70
290	SHIELDING	8080	-295.5	60x70
291	SHIELDING	8160	-295.5	60x70
292	BISTAUTO	8240	-295.5	60x70
293	BIST_ENB	8320	-295.5	60x70
294	SHIELDING	8400	-295.5	60x70
295	SHIELDING	8480	-295.5	60x70
296	CLK_EXT	8560	-295.5	60x70
297	PWRMD	8640	-295.5	60x70
298	SHIELDING	8720	-295.5	60x70
299	LNSW0	8800	-295.5	60x70
300	LNSW1	8880	-295.5	60x70
301	SHIELDING	8960	-295.5	60x70
302	SHIELDING	9040	-295.5	60x70
303	SHIELDING	9120	-295.5	60x70
304	SHIELDING	9200	-295.5	60x70
305	SHIELDING	9280	-295.5	60x70
306	SHIELDING	9360	-295.5	60x70
307	MIPI_LAN0	9440	-295.5	60x70
308	MIPI_LAN1	9520	-295.5	60x70
309	SHIELDING	9600	-295.5	60x70
310	ZTYPE	9680	-295.5	60x70
311	ZIGZAG	9760	-295.5	60x70
312	SHIELDING	9840	-295.5	60x70
313	NBW	9920	-295.5	60x70
314	SHIELDING	10000	-295.5	60x70
315	SHIELDING	10080	-295.5	60x70
316	SHIELDING	10160	-295.5	60x70
317	SHIELDING	10240	-295.5	60x70
318	SHIELDING	10320	-295.5	60x70
319	SHIELDING	10400	-295.5	60x70
320	GOA_EN	10480	-295.5	60x70
321	SHIELDING	10560	-295.5	60x70
322	SHIELDING	10640	-295.5	60x70
323	SHIELDING	10720	-295.5	60x70
324	SHIELDING	10800	-295.5	60x70
325	RP1EN	10880	-295.5	60x70
326	COM3	10960	-295.5	60x70
327	COM3	11040	-295.5	60x70
328	RP1O	11120	-295.5	60x70
329	RP1O	11200	-295.5	60x70
330	RP1O	11280	-295.5	60x70
331	SHIELDING	11360	-295.5	60x70
332	SHIELDING	11440	-295.5	60x70
333	SHIELDING	11520	-295.5	60x70
334	SHIELDING	11600	-295.5	60x70
335	SHIELDING	11680	-295.5	60x70
336	COML2	11760	-295.5	60x70
337	COML2	11840	-295.5	60x70
338	COML1	11920	-295.5	60x70
339	COML1	12000	-295.5	60x70
340	VPP	12080	-295.5	60x70
341	VPP	12160	-295.5	60x70
342	VPP	12240	-295.5	60x70
343	VGH	12305	-295.5	60x70
344	VGH	12355	-295.5	60x70
345	VGH	12405	-295.5	60x70
346	VGL	12455	-295.5	60x70
347	VGL	12505	-295.5	60x70
348	VGL	12555	-295.5	60x70
349	VGL	12605	-295.5	60x70
350	VGL	12655	-295.5	60x70
351	VGL	12705	-295.5	60x70
352	VGL1_L	12755	-295.5	60x70
353	VGL1_L	12805	-295.5	60x70
354	VGL1_L	12855	-295.5	60x70
355	GOUT_L20	12905	-295.5	60x70
356	GOUT_L19	12955	-295.5	60x70
357	GOUT_L18	13005	-295.5	60x70
358	GOUT_L17	13055	-295.5	60x70
359	GOUT_L16	13105	-295.5	60x70
360	GOUT_L15	13155	-295.5	60x70
361	GOUT_L14	13205	-295.5	60x70
362	GOUT_L13	13255	-295.5	60x70
363	GOUT_L12	13305	-295.5	60x70
364	GOUT_L11	13355	-295.5	60x70
365	GOUT_L10	13405	-295.5	60x70
366	GOUT_L9	13455	-295.5	60x70
367	GOUT_L8	13505	-295.5	60x70
368	GOUT_L7	13555	-295.5	60x70
369	GOUT_L6	13605	-295.5	60x70
370	GOUT_L5	13655	-295.5	60x70
371	GOUT_L4	13705	-295.5	60x70
372	GOUT_L3	13755	-295.5	60x70
373	VGL	13805	-295.5	60x70
374	VGL	13855	-295.5	60x70
375	GOUT_L2	13905	-295.5	60x70
376	GOUT_L1	13955	-295.5	60x70
377	SHIELDING	14005	-295.5	60x70
378	SYNC_L12	14093	-97.5	120x20
379	SYNC_L11	14093	-59.5	120x20
380	SYNC_L10	14093	-21.5	120x20
381	SYNC_L9	14093	16.5	120x20
382	SYNC_L8	14093	54.5	120x20
383	SYNC_L7	14093	92.5	120x20
384	SYNC_L6	14093	130.5	120x20
385	SYNC_L5	14093	168.5	120x20
386	SYNC_L4	14093	206.5	120x20
387	SYNC_L3	14093	244.5	120x20
388	SYNC_L2	14093	282.5	120x20
389	SYNC_L1	14093	320.5	120x20
390	SHIELDING	13954	310.5	40x40
391	SHIELDING	13874	310.5	40x40
392	SHIELDING	13794	310.5	40x40
393	SHIELDING	13714	310.5	40x40
394	SHIELDING	13634	310.5	40x40
395	SHIELDING	13554	310.5	40x40
396	SHIELDING	13474	310.5	40x40
397	SHIELDING	13394	310.5	40x40
398	SHIELDING	13314	310.5	40x40
399	SHIELDING	13234	310.5	40x40
400	COML1	13154	310.5	40x40
401	COML1	13074	310.5	40x40
402	COML2	12994	310.5	40x40
403	COML2	12914	310.5	40x40
404	RP1I	12834	310.5	40x40
405	RP1I	12754	310.5	40x40
406	COM4	12694	295.5	18x70
407	SHIELDING	12682	190.5	18x70
408	SHIELDING	12670	85.5	18x70
409	COM4	12658	295.5	18x70
410	SHIELDING	12646	190.5	18x70
411	SHIELDING	12634	85.5	18x70
412	S0	12622	295.5	18x70
413	S1	12610	190.5	18x70
414	S2	12598	85.5	18x70
415	S3	12586	295.5	18x70
416	S4	12574	190.5	18x70
417	S5	12562	85.5	18x70
418	S6	12550	295.5	18x70
419	S7	12538	190.5	18x70
420	S8	12526	85.5	18x70
421	S9	12514	295.5	18x70
422	S10	12502	190.5	18x70
423	S11	12490	85.5	18x70
424	S12	12478	295.5	18x70
425	S13	12466	190.5	18x70
426	S14	12454	85.5	18x70
427	S15	12442	295.5	18x70
428	S16	12430	190.5	18x70
429	S17	12418	85.5	18x70
430	S18	12406	295.5	18x70
431	S19	12394	190.5	18x70
432	S20	12382	85.5	18x70
433	S21	12370	295.5	18x70
434	S22	12358	190.5	18x70
435	S23	12346	85.5	18x70
436	S24	12334	295.5	18x70
437	S25	12322	190.5	18x70
438	S26	12310	85.5	18x70
439	S27	12298	295.5	18x70
440	S28	12286	190.5	18x70
441	S29	12274	85.5	18x70
442	S30	12262	295.5	18x70
443	S31	12250	190.5	18x70
444	S32	12238	85.5	18x70
445	S33	12226	295.5	18x70
446	S34	12214	190.5	18x70
447	S35	12202	85.5	18x70
448	S36	12190	295.5	18x70
449	S37	12178	190.5	18x70
450	S38	12166	85.5	18x70
451	S39	12154	295.5	18x70
452	S40	12142	190.5	18x70
453	S41	12130	85.5	18x70
454	S42	12118	295.5	18x70
455	S43	12106	190.5	18x70
456	S44	12094	85.5	18x70
457	S45	12082	295.5	18x70
458	S46	12070	190.5	18x70
459	S47	12058	85.5	18x70
460	S48	12046	295.5	18x70
461	S49	12034	190.5	18x70
462	S50	12022	85.5	18x70
463	S51	12010	295.5	18x70
464	S52	11998	190.5	18x70
465	S53	11986	85.5	18x70
466	S54	11974	295.5	18x70
467	S55	11962	190.5	18x70
468	S56	11950	85.5	18x70
469	S57	11938	295.5	18x70
470	S58	11926	190.5	18x70
471	S59	11914	85.5	18x70
472	S60	11902	295.5	18x70
473	S61	11890	190.5	18x70
474	S62	11878	85.5	18x70
475	S63	11866	295.5	18x70
476	S64	11854	190.5	18x70
477	S65	11842	85.5	18x70
478	S66	11830	295.5	18x70
479	S67	11818	190.5	18x70
480	S68	11806	85.5	18x70

No.	Name	X	Y	Bump size
481	S69	11794	295.5	18x70
482	S70	11782	190.5	18x70
483	S71	11770	85.5	18x70
484	S72	11758	295.5	18x70
485	S73	11746	190.5	18x70
486	S74	11734	85.5	18x70
487	S75	11722	295.5	18x70
488	S76	11710	190.5	18x70
489	S77	11698	85.5	18x70
490	S78	11686	295.5	18x70
491	S79	11674	190.5	18x70
492	S80	11662	85.5	18x70
493	S81	11650	295.5	18x70
494	S82	11638	190.5	18x70
495	S83	11626	85.5	18x70
496	S84	11614	295.5	18x70
497	S85	11602	190.5	18x70
498	S86	11590	85.5	18x70
499	S87	11578	295.5	18x70
500	S88	11566	190.5	18x70
501	S89	11554	85.5	18x70
502	S90	11542	295.5	18x70
503	S91	11530	190.5	18x70
504	S92	11518	85.5	18x70
505	S93	11506	295.5	18x70
506	S94	11494	190.5	18x70
507	S95	11482	85.5	18x70
508	S96	11470	295.5	18x70
509	S97	11458	190.5	18x70
510	S98	11446	85.5	18x70
511	S99	11434	295.5	18x70
512	S100	11422	190.5	18x70
513	S101	11410	85.5	18x70
514	S102	11398	295.5	18x70
515	S103	11386	190.5	18x70
516	S104	11374	85.5	18x70
517	S105	11362	295.5	18x70
518	S106	11350	190.5	18x70
519	S107	11338	85.5	18x70
520	S108	11326	295.5	18x70
521	S109	11314	190.5	18x70
522	S110	11302	85.5	18x70
523	S111	11290	295.5	18x70
524	S112	11278	190.5	18x70
525	S113	11266	85.5	18x70
526	S114	11254	295.5	18x70
527	S115	11242	190.5	18x70
528	S116	11230	85.5	18x70
529	S117	11218	295.5	18x70
530	S118	11206	190.5	18x70
531	S119	11194	85.5	18x70
532	S120	11182	295.5	18x70
533	S121	11170	190.5	18x70
534	S122	11158	85.5	18x70
535	S123	11146	295.5	18x70
536	S124	11134	190.5	18x70
537	S125	11122	85.5	18x70
538	S126	11110	295.5	18x70
539	S127	11098	190.5	18x70
540	S128	11086	85.5	18x70
541	S129	11074	295.5	18x70
542	S130	11062	190.5	18x70
543	S131	11050	85.5	18x70
544	S132	11038	295.5	18x70
545	S133	11026	190.5	18x70
546	S134	11014	85.5	18x70
547	S135	11002	295.5	18x70
548	S136	10990	190.5	18x70
549	S137	10978	85.5	18x70
550	S138	10966	295.5	18x70
551	S139	10954	190.5	18x70
552	S140	10942	85.5	18x70
553	S141	10930	295.5	18x70
554	S142	10918	190.5	18x70
555	S143	10906	85.5	18x70
556	S144	10894	295.5	18x70
557	S145	10882	190.5	18x70
558	S146	10870	85.5	18x70
559	S147	10858	295.5	18x70
560	S148	10846	190.5	18x70
561	S149	10834	85.5	18x70
562	S150	10822	295.5	18x70
563	S151	10810	190.5	18x70
564	S152	10798	85.5	18x70
565	S153	10786	295.5	18x70
566	S154	10774	190.5	18x70
567	S155	10762	85.5	18x70
568	S156	10750	295.5	18x70
569	S157	10738	190.5	18x70
570	S158	10726	85.5	18x70
571	S159	10714	295.5	18x70
572	S160	10702	190.5	18x70
573	S161	10690	85.5	18x70
574	S162	10678	295.5	18x70
575	S163	10666	190.5	18x70
576	S164	10654	85.5	18x70
577	S165	10642	295.5	18x70
578	S166	10630	190.5	18x70
579	S167	10618	85.5	18x70
580	S168	10606	295.5	18x70
581	S169	10594	190.5	18x70
582	S170	10582	85.5	18x70
583	S171	10570	295.5	18x70
584	S172	10558	190.5	18x70
585	S173	10546	85.5	18x70
586	S174	10534	295.5	18x70
587	S175	10522	190.5	18x70
588	S176	10510	85.5	18x70
589	S177	10498	295.5	18x70
590	S178	10486	190.5	18x70
591	S179	10474	85.5	18x70
592	S180	10462	295.5	18x70
593	S181	10450	190.5	18x70
594	S182	10438	85.5	18x70
595	S183	10426	295.5	18x70
596	S184	10414	190.5	18x70
597	S185	10402	85.5	18x70
598	S186	10390	295.5	18x70
599	S187	10378	190.5	18x70
600	S188	10366	85.5	18x70
601	S189	10354	295.5	18x70
602	S190	10342	190.5	18x70
603	S191	10330	85.5	18x70
604	S192	10318	295.5	18x70
605	S193	10306	190.5	18x70
606	S194	10294	85.5	18x70
607	S195	10282	295.5	18x70
608	S196	10270	190.5	18x70
609	S197	10258	85.5	18x70
610	S198	10246	295.5	18x70
611	S199	10234	190.5	18x70
612	S200	10222	85.5	18x70
613	S201	10210	295.5	18x70
614	S202	10198	190.5	18x70
615	S203	10186	85.5	18x70
616	S204	10174	295.5	18x70
617	S205	10162	190.5	18x70
618	S206	10150	85.5	18x70
619	S207	10138	295.5	18x70
620	S208	10126	190.5	18x70
621	S209	10114	85.5	18x70
622	S210	10102	295.5	18x70
623	S211	10090	190.5	18x70
624	S212	10078	85.5	18x70
625	S213	10066	295.5	18x70
626	S214	10054	190.5	18x70
627	S215	10042	85.5	18x70
628	S216	10030	295.5	18x70
629	S217	10018	190.5	18x70
630	S218	10006	85.5	18x70
631	S219	9994	295.5	18x70
632	S220	9982	190.5	18x70
633	S221	9970	85.5	18x70
634	S222	9958	295.5	18x70
635	S223	9946	190.5	18x70
636	S224	9934	85.5	18x70
637	S225	9922	295.5	18x70
638	S226	9910	190.5	18x70
639	S227	9898	85.5	18x70
640	S228	9886	295.5	18x70
641	S229	9874	190.5	18x70
642	S230	9862	85.5	18x70
643	S231	9850	295.5	18x70
644	S232	9838	190.5	18x70
645	S233	9826	85.5	18x70
646	S234	9814	295.5	18x70
647	S235	9802	190.5	18x70
648	S236	9790	85.5	18x70
649	S237	9778	295.5	18x70
650	S238	9766	190.5	18x70
651	S239	9754	85.5	18x70
652	S240	9742	295.5	18x70
653	S241	9730	190.5	18x70
654	S242	9718	85.5	18x70
655	S243	9706	295.5	18x70
656	S244	9694	190.5	18x70
657	S245	9682	85.5	18x70
658	S246	9670	295.5	18x70
659	S247	9658	190.5	18x70
660	S248	9646	85.5	18x70
661	S249	9634	295.5	18x70
662	S250	9622	190.5	18x70
663	S251	9610	85.5	18x70
664	S252	9598	295.5	18x70
665	S253	9586	190.5	18x70
666	S254	9574	85.5	18x70
667	S255	9562	295.5	18x70
668	S256	9550	190.5	18x70
669	S257	9538	85.5	18x70
670	S258	9526	295.5	18x70
671	S259	9514	190.5	18x70
672	S260	9502	85.5	18x70
673	S261	9490	295.5	18x70
674	S262	9478	190.5	18x70
675	S263	9466	85.5	18x70
676	S264	9454	295.5	18x70
677	S265	9442	190.5	18x70
678	S266	9430	85.5	18x70
679	S267	9418	295.5	18x70
680	S268	9406	190.5	18x70
681	S269	9394	85.5	18x70
682	S270	9382	295.5	18x70
683	S271	9370	190.5	18x70
684	S272	9358	85.5	18x70
685	S273	9346	295.5	18x70
686	S274	9334	190.5	18x70
687	S275	9322	85.5	18x70
688	S276	9310	295.5	18x70
689	S277	9298	190.5	18x70
690	S278	9286	85.5	18x70
691	S279	9274	295.5	18x70
692	S280	9262	190.5	18x70
693	S281	9250	85.5	18x70
694	S282	9238	295.5	18x70
695	S283	9226	190.5	18x70
696	S284	9214	85.5	18x70
697	S285	9202	295.5	18x70
698	S286	9190	190.5	18x70
699	S287	9178	85.5	18x70
700	S288	9166	295.5	18x70
701	S289	9154	190.5	18x70
702	S290	9142	85.5	18x70
703	S291	9130	295.5	18x70
704	S292	9118	190.5	18x70
705	S293	9106	85.5	18x70
706	S294	9094	295.5	18x70
707	S295	9082	190.5	18x70
708	S296	9070	85.5	18x70
709	S297	9058	295.5	18x70
710	S298	9046	190.5	18x70
711	S299	9034	85.5	18x70
712	S300	9022	295.5	18x70
713	S301	9010	190.5	18x70
714	S302	8998	85.5	18x70
715	S303	8986	295.5	18x70
716	S304	8974	190.5	18x70
717	S305	8962	85.5	18x70
718	S306	8950	295.5	18x70
719	S307	8938	190.5	18x70
720	S308	8926	85.5	18x70

No.	Name	X	Y	Bump size
721	S309	8914	295.5	18x70
722	S310	8902	190.5	18x70
723	S311	8890	85.5	18x70
724	S312	8878	295.5	18x70
725	S313	8866	190.5	18x70
726	S314	8854	85.5	18x70
727	S315	8842	295.5	18x70
728	S316	8830	190.5	18x70
729	S317	8818	85.5	18x70
730	S318	8806	295.5	18x70
731	S319	8794	190.5	18x70
732	S320	8782	85.5	18x70
733	S321	8770	295.5	18x70
734	S322	8758	190.5	18x70
735	S323	8746	85.5	18x70
736	S324	8734	295.5	18x70
737	S325	8722	190.5	18x70
738	S326	8710	85.5	18x70
739	S327	8698	295.5	18x70
740	S328	8686	190.5	18x70
741	S329	8674	85.5	18x70
742	S330	8662	295.5	18x70
743	S331	8650	190.5	18x70
744	S332	8638	85.5	18x70
745	S333	8626	295.5	18x70
746	S334	8614	190.5	18x70
747	S335	8602	85.5	18x70
748	S336	8590	295.5	18x70
749	S337	8578	190.5	18x70
750	S338	8566	85.5	18x70
751	S339	8554	295.5	18x70
752	S340	8542	190.5	18x70
753	S341	8530	85.5	18x70
754	S342	8518	295.5	18x70
755	S343	8506	190.5	18x70
756	S344	8494	85.5	18x70
757	S345	8482	295.5	18x70
758	S346	8470	190.5	18x70
759	S347	8458	85.5	18x70
760	S348	8446	295.5	18x70
761	S349	8434	190.5	18x70
762	S350	8422	85.5	18x70
763	S351	8410	295.5	18x70
764	S352	8398	190.5	18x70
765	S353	8386	85.5	18x70
766	S354	8374	295.5	18x70
767	S355	8362	190.5	18x70
768	S356	8350	85.5	18x70
769	S357	8338	295.5	18x70
770	S358	8326	190.5	18x70
771	S359	8314	85.5	18x70
772	S360	8302	295.5	18x70
773	S361	8290	190.5	18x70
774	S362	8278	85.5	18x70
775	S363	8266	295.5	18x70
776	S364	8254	190.5	18x70
777	S365	8242	85.5	18x70
778	S366	8230	295.5	18x70
779	S367	8218	190.5	18x70
780	S368	8206	85.5	18x70
781	S369	8194	295.5	18x70
782	S370	8182	190.5	18x70
783	S371	8170	85.5	18x70
784	S372	8158	295.5	18x70
785	S373	8146	190.5	18x70
786	S374	8134	85.5	18x70
787	S375	8122	295.5	18x70
788	S376	8110	190.5	18x70
789	S377	8098	85.5	18x70
790	S378	8086	295.5	18x70
791	S379	8074	190.5	18x70
792	S380	8062	85.5	18x70
793	S381	8050	295.5	18x70
794	S382	8038	190.5	18x70
795	S383	8026	85.5	18x70
796	S384	8014	295.5	18x70
797	S385	8002	190.5	18x70
798	S386	7990	85.5	18x70
799	S387	7978	295.5	18x70
800	S388	7966	190.5	18x70
801	S389	7954	85.5	18x70
802	S390	7942	295.5	18x70
803	S391	7930	190.5	18x70
804	S392	7918	85.5	18x70
805	S393	7906	295.5	18x70
806	S394	7894	190.5	18x70
807	S395	7882	85.5	18x70
808	S396	7870	295.5	18x70
809	S397	7858	190.5	18x70
810	S398	7846	85.5	18x70
811	S399	7834	295.5	18x70
812	S400	7822	190.5	18x70
813	S401	7810	85.5	18x70
814	S402	7798	295.5	18x70
815	S403	7786	190.5	18x70
816	S404	7774	85.5	18x70
817	S405	7762	295.5	18x70
818	S406	7750	190.5	18x70
819	S407	7738	85.5	18x70
820	S408	7726	295.5	18x70
821	S409	7714	190.5	18x70
822	S410	7702	85.5	18x70
823	S411	7690	295.5	18x70
824	S412	7678	190.5	18x70
825	S413	7666	85.5	18x70
826	S414	7654	295.5	18x70
827	S415	7642	190.5	18x70
828	S416	7630	85.5	18x70
829	S417	7618	295.5	18x70
830	S418	7606	190.5	18x70
831	S419	7594	85.5	18x70
832	S420	7582	295.5	18x70
833	S421	7570	190.5	18x70
834	S422	7558	85.5	18x70
835	S423	7546	295.5	18x70
836	S424	7534	190.5	18x70
837	S425	7522	85.5	18x70
838	S426	7510	295.5	18x70
839	S427	7498	190.5	18x70
840	S428	7486	85.5	18x70
841	S429	7474	295.5	18x70
842	S430	7462	190.5	18x70
843	S431	7450	85.5	18x70
844	S432	7438	295.5	18x70
845	S433	7426	190.5	18x70
846	S434	7414	85.5	18x70
847	S435	7402	295.5	18x70
848	S436	7390	190.5	18x70
849	S437	7378	85.5	18x70
850	S438	7366	295.5	18x70
851	S439	7354	190.5	18x70
852	S440	7342	85.5	18x70
853	S441	7330	295.5	18x70
854	S442	7318	190.5	18x70
855	S443	7306	85.5	18x70
856	S444	7294	295.5	18x70
857	S445	7282	190.5	18x70
858	S446	7270	85.5	18x70
859	S447	7258	295.5	18x70
860	S448	7246	190.5	18x70
861	S449	7234	85.5	18x70
862	S450	7222	295.5	18x70
863	S451	7210	190.5	18x70
864	S452	7198	85.5	18x70
865	S453	7186	295.5	18x70
866	S454	7174	190.5	18x70
867	S455	7162	85.5	18x70
868	S456	7150	295.5	18x70
869	S457	7138	190.5	18x70
870	S458	7126	85.5	18x70
871	S459	7114	295.5	18x70
872	S460	7102	190.5	18x70
873	S461	7090	85.5	18x70
874	S462	7078	295.5	18x70
875	S463	7066	190.5	18x70
876	S464	7054	85.5	18x70
877	S465	7042	295.5	18x70
878	S466	7030	190.5	18x70
879	S467	7018	85.5	18x70
880	S468	7006	295.5	18x70
881	S469	6994	190.5	18x70
882	S470	6982	85.5	18x70
883	S471	6970	295.5	18x70
884	S472	6958	190.5	18x70
885	S473	6946	85.5	18x70
886	S474	6934	295.5	18x70
887	S475	6922	190.5	18x70
888	S476	6910	85.5	18x70
889	S477	6898	295.5	18x70
890	S478	6886	190.5	18x70
891	S479	6874	85.5	18x70
892	S480	6862	295.5	18x70
893	S481	6850	190.5	18x70
894	S482	6838	85.5	18x70
895	S483	6826	295.5	18x70
896	S484	6814	190.5	18x70
897	S485	6802	85.5	18x70
898	S486	6790	295.5	18x70
899	S487	6778	190.5	18x70
900	S488	6766	85.5	18x70
901	S489	6754	295.5	18x70
902	S490	6742	190.5	18x70
903	S491	6730	85.5	18x70
904	S492	6718	295.5	18x70
905	S493	6706	190.5	18x70
906	S494	6694	85.5	18x70
907	S495	6682	295.5	18x70
908	S496	6670	190.5	18x70
909	S497	6658	85.5	18x70
910	S498	6646	295.5	18x70
911	S499	6634	190.5	18x70
912	S500	6622	85.5	18x70
913	S501	6610	295.5	18x70
914	S502	6598	190.5	18x70
915	S503	6586	85.5	18x70
916	S504	6574	295.5	18x70
917	S505	6562	190.5	18x70
918	S506	6550	85.5	18x70
919	S507	6538	295.5	18x70
920	S508	6526	190.5	18x70
921	S509	6514	85.5	18x70
922	S510	6502	295.5	18x70
923	S511	6490	190.5	18x70
924	S512	6478	85.5	18x70
925	S513	6466	295.5	18x70
926	S514	6454	190.5	18x70
927	S515	6442	85.5	18x70
928	S516	6430	295.5	18x70
929	S517	6418	190.5	18x70
930	S518	6406	85.5	18x70
931	S519	6394	295.5	18x70
932	S520	6382	190.5	18x70
933	S521	6370	85.5	18x70
934	S522	6358	295.5	18x70
935	S523	6346	190.5	18x70
936	S524	6334	85.5	18x70
937	S525	6322	295.5	18x70
938	S526	6310	190.5	18x70
939	S527	6298	85.5	18x70
940	S528	6286	295.5	18x70
941	S529	6274	190.5	18x70
942	S530	6262	85.5	18x70
943	S531	6250	295.5	18x70
944	S532	6238	190.5	18x70
945	S533	6226	85.5	18x70
946	S534	6214	295.5	18x70
947	S535	6202	190.5	18x70
948	S536	6190	85.5	18x70
949	S537	6178	295.5	18x70
950	S538	6166	190.5	18x70
951	S539	6154	85.5	18x70
952	S540	6142	295.5	18x70
953	S541	6130	190.5	18x70
954	S542	6118	85.5	18x70
955	S543	6106	295.5	18x70
956	S544	6094	190.5	18x70
957	S545	6082	85.5	18x70
958	S546	6070	295.5	18x70
959	S547	6058	190.5	18x70
960	S548	6046	85.5	18x70

No.	Name	X	Y	Bump size
961	S549	6034	295.5	18x70
962	S550	6022	190.5	18x70
963	S551	6010	85.5	18x70
964	S552	5998	295.5	18x70
965	S553	5986	190.5	18x70
966	S554	5974	85.5	18x70
967	S555	5962	295.5	18x70
968	S556	5950	190.5	18x70
969	S557	5938	85.5	18x70
970	S558	5926	295.5	18x70
971	S559	5914	190.5	18x70
972	S560	5902	85.5	18x70
973	S561	5890	295.5	18x70
974	S562	5878	190.5	18x70
975	S563	5866	85.5	18x70
976	S564	5854	295.5	18x70
977	S565	5842	190.5	18x70
978	S566	5830	85.5	18x70
979	S567	5818	295.5	18x70
980	S568	5806	190.5	18x70
981	S569	5794	85.5	18x70
982	S570	5782	295.5	18x70
983	S571	5770	190.5	18x70
984	S572	5758	85.5	18x70
985	S573	5746	295.5	18x70
986	S574	5734	190.5	18x70
987	S575	5722	85.5	18x70
988	S576	5710	295.5	18x70
989	S577	5698	190.5	18x70
990	S578	5686	85.5	18x70
991	S579	5674	295.5	18x70
992	S580	5662	190.5	18x70
993	S581	5650	85.5	18x70
994	S582	5638	295.5	18x70
995	S583	5626	190.5	18x70
996	S584	5614	85.5	18x70
997	S585	5602	295.5	18x70
998	S586	5590	190.5	18x70
999	S587	5578	85.5	18x70
1000	S588	5566	295.5	18x70
1001	S589	5554	190.5	18x70
1002	S590	5542	85.5	18x70
1003	S591	5530	295.5	18x70
1004	S592	5518	190.5	18x70
1005	S593	5506	85.5	18x70
1006	S594	5494	295.5	18x70
1007	S595	5482	190.5	18x70
1008	S596	5470	85.5	18x70
1009	S597	5458	295.5	18x70
1010	S598	5446	190.5	18x70
1011	S599	5434	85.5	18x70
1012	S600	5422	295.5	18x70
1013	S601	5410	190.5	18x70
1014	S602	5398	85.5	18x70
1015	S603	5386	295.5	18x70
1016	S604	5374	190.5	18x70
1017	S605	5362	85.5	18x70
1018	S606	5350	295.5	18x70
1019	S607	5338	190.5	18x70
1020	S608	5326	85.5	18x70
1021	S609	5314	295.5	18x70
1022	S610	5302	190.5	18x70
1023	S611	5290	85.5	18x70
1024	S612	5278	295.5	18x70
1025	S613	5266	190.5	18x70
1026	S614	5254	85.5	18x70
1027	S615	5242	295.5	18x70
1028	S616	5230	190.5	18x70
1029	S617	5218	85.5	18x70
1030	S618	5206	295.5	18x70
1031	S619	5194	190.5	18x70
1032	S620	5182	85.5	18x70
1033	S621	5170	295.5	18x70
1034	S622	5158	190.5	18x70
1035	S623	5146	85.5	18x70
1036	S624	5134	295.5	18x70
1037	S625	5122	190.5	18x70
1038	S626	5110	85.5	18x70
1039	S627	5098	295.5	18x70
1040	S628	5086	190.5	18x70
1041	S629	5074	85.5	18x70
1042	S630	5062	295.5	18x70
1043	S631	5050	190.5	18x70
1044	S632	5038	85.5	18x70
1045	S633	5026	295.5	18x70
1046	S634	5014	190.5	18x70
1047	S635	5002	85.5	18x70
1048	S636	4990	295.5	18x70
1049	S637	4978	190.5	18x70
1050	S638	4966	85.5	18x70
1051	S639	4954	295.5	18x70
1052	S640	4942	190.5	18x70
1053	S641	4930	85.5	18x70
1054	S642	4918	295.5	18x70
1055	S643	4906	190.5	18x70
1056	S644	4894	85.5	18x70
1057	S645	4882	295.5	18x70
1058	S646	4870	190.5	18x70
1059	S647	4858	85.5	18x70
1060	S648	4846	295.5	18x70
1061	S649	4834	190.5	18x70
1062	S650	4822	85.5	18x70
1063	S651	4810	295.5	18x70
1064	S652	4798	190.5	18x70
1065	S653	4786	85.5	18x70
1066	S654	4774	295.5	18x70
1067	S655	4762	190.5	18x70
1068	S656	4750	85.5	18x70
1069	S657	4738	295.5	18x70
1070	S658	4726	190.5	18x70
1071	S659	4714	85.5	18x70
1072	S660	4702	295.5	18x70
1073	S661	4690	190.5	18x70
1074	S662	4678	85.5	18x70
1075	S663	4666	295.5	18x70
1076	S664	4654	190.5	18x70
1077	S665	4642	85.5	18x70
1078	S666	4630	295.5	18x70
1079	S667	4618	190.5	18x70
1080	S668	4606	85.5	18x70
1081	S669	4594	295.5	18x70
1082	S670	4582	190.5	18x70
1083	S671	4570	85.5	18x70
1084	S672	4558	295.5	18x70
1085	S673	4546	190.5	18x70
1086	S674	4534	85.5	18x70
1087	S675	4522	295.5	18x70
1088	S676	4510	190.5	18x70
1089	S677	4498	85.5	18x70
1090	S678	4486	295.5	18x70
1091	S679	4474	190.5	18x70
1092	S680	4462	85.5	18x70
1093	S681	4450	295.5	18x70
1094	S682	4438	190.5	18x70
1095	S683	4426	85.5	18x70
1096	S684	4414	295.5	18x70
1097	S685	4402	190.5	18x70
1098	S686	4390	85.5	18x70
1099	S687	4378	295.5	18x70
1100	S688	4366	190.5	18x70
1101	S689	4354	85.5	18x70
1102	S690	4342	295.5	18x70
1103	S691	4330	190.5	18x70
1104	S692	4318	85.5	18x70
1105	S693	4306	295.5	18x70
1106	S694	4294	190.5	18x70
1107	S695	4282	85.5	18x70
1108	S696	4270	295.5	18x70
1109	S697	4258	190.5	18x70
1110	S698	4246	85.5	18x70
1111	S699	4234	295.5	18x70
1112	S700	4222	190.5	18x70
1113	S701	4210	85.5	18x70
1114	S702	4198	295.5	18x70
1115	S703	4186	190.5	18x70
1116	S704	4174	85.5	18x70
1117	S705	4162	295.5	18x70
1118	S706	4150	190.5	18x70
1119	S707	4138	85.5	18x70
1120	S708	4126	295.5	18x70
1121	S709	4114	190.5	18x70
1122	S710	4102	85.5	18x70
1123	S711	4090	295.5	18x70
1124	S712	4078	190.5	18x70
1125	S713	4066	85.5	18x70
1126	S714	4054	295.5	18x70
1127	S715	4042	190.5	18x70
1128	S716	4030	85.5	18x70
1129	S717	4018	295.5	18x70
1130	S718	4006	190.5	18x70
1131	S719	3994	85.5	18x70
1132	S720	3982	295.5	18x70
1133	S721	3970	190.5	18x70
1134	S722	3958	85.5	18x70
1135	S723	3946	295.5	18x70
1136	S724	3934	190.5	18x70
1137	S725	3922	85.5	18x70
1138	S726	3910	295.5	18x70
1139	S727	3898	190.5	18x70
1140	S728	3886	85.5	18x70
1141	S729	3874	295.5	18x70
1142	S730	3862	190.5	18x70
1143	S731	3850	85.5	18x70
1144	S732	3838	295.5	18x70
1145	S733	3826	190.5	18x70
1146	S734	3814	85.5	18x70
1147	S735	3802	295.5	18x70
1148	S736	3790	190.5	18x70
1149	S737	3778	85.5	18x70
1150	S738	3766	295.5	18x70
1151	S739	3754	190.5	18x70
1152	S740	3742	85.5	18x70
1153	S741	3730	295.5	18x70
1154	S742	3718	190.5	18x70
1155	S743	3706	85.5	18x70
1156	S744	3694	295.5	18x70
1157	S745	3682	190.5	18x70
1158	S746	3670	85.5	18x70
1159	S747	3658	295.5	18x70
1160	S748	3646	190.5	18x70
1161	S749	3634	85.5	18x70
1162	S750	3622	295.5	18x70
1163	S751	3610	190.5	18x70
1164	S752	3598	85.5	18x70
1165	S753	3586	295.5	18x70
1166	S754	3574	190.5	18x70
1167	S755	3562	85.5	18x70
1168	S756	3550	295.5	18x70
1169	S757	3538	190.5	18x70
1170	S758	3526	85.5	18x70
1171	S759	3514	295.5	18x70
1172	S760	3502	190.5	18x70
1173	S761	3490	85.5	18x70
1174	S762	3478	295.5	18x70
1175	S763	3466	190.5	18x70
1176	S764	3454	85.5	18x70
1177	S765	3442	295.5	18x70
1178	S766	3430	190.5	18x70
1179	S767	3418	85.5	18x70
1180	S768	3406	295.5	18x70
1181	S769	3394	190.5	18x70
1182	S770	3382	85.5	18x70
1183	S771	3370	295.5	18x70
1184	S772	3358	190.5	18x70
1185	S773	3346	85.5	18x70
1186	S774	3334	295.5	18x70
1187	S775	3322	190.5	18x70
1188	S776	3310	85.5	18x70
1189	S777	3298	295.5	18x70
1190	S778	3286	190.5	18x70
1191	S779	3274	85.5	18x70
1192	S780	3262	295.5	18x70
1193	S781	3250	190.5	18x70
1194	S782	3238	85.5	18x70
1195	S783	3226	295.5	18x70
1196	S784	3214	190.5	18x70
1197	S785	3202	85.5	18x70
1198	S786	3190	295.5	18x70
1199	S787	3178	190.5	18x70
1200	S788	3166	85.5	18x70

No.	Name	X	Y	Bump size
1201	S789	3154	295.5	18x70
1202	S790	3142	190.5	18x70
1203	S791	3130	85.5	18x70
1204	S792	3118	295.5	18x70
1205	S793	3106	190.5	18x70
1206	S794	3094	85.5	18x70
1207	S795	3082	295.5	18x70
1208	S796	3070	190.5	18x70
1209	S797	3058	85.5	18x70
1210	S798	3046	295.5	18x70
1211	S799	3034	190.5	18x70
1212	S800	3022	85.5	18x70
1213	S801	3010	295.5	18x70
1214	S802	2998	190.5	18x70
1215	S803	2986	85.5	18x70
1216	S804	2974	295.5	18x70
1217	S805	2962	190.5	18x70
1218	S806	2950	85.5	18x70
1219	S807	2938	295.5	18x70
1220	S808	2926	190.5	18x70
1221	S809	2914	85.5	18x70
1222	S810	2902	295.5	18x70
1223	S811	2890	190.5	18x70
1224	S812	2878	85.5	18x70
1225	S813	2866	295.5	18x70
1226	S814	2854	190.5	18x70
1227	S815	2842	85.5	18x70
1228	S816	2830	295.5	18x70
1229	S817	2818	190.5	18x70
1230	S818	2806	85.5	18x70
1231	S819	2794	295.5	18x70
1232	S820	2782	190.5	18x70
1233	S821	2770	85.5	18x70
1234	S822	2758	295.5	18x70
1235	S823	2746	190.5	18x70
1236	S824	2734	85.5	18x70
1237	S825	2722	295.5	18x70
1238	S826	2710	190.5	18x70
1239	S827	2698	85.5	18x70
1240	S828	2686	295.5	18x70
1241	S829	2674	190.5	18x70
1242	S830	2662	85.5	18x70
1243	S831	2650	295.5	18x70
1244	S832	2638	190.5	18x70
1245	S833	2626	85.5	18x70
1246	S834	2614	295.5	18x70
1247	S835	2602	190.5	18x70
1248	S836	2590	85.5	18x70
1249	S837	2578	295.5	18x70
1250	S838	2566	190.5	18x70
1251	S839	2554	85.5	18x70
1252	S840	2542	295.5	18x70
1253	S841	2530	190.5	18x70
1254	S842	2518	85.5	18x70
1255	S843	2506	295.5	18x70
1256	S844	2494	190.5	18x70
1257	S845	2482	85.5	18x70
1258	S846	2470	295.5	18x70
1259	S847	2458	190.5	18x70
1260	S848	2446	85.5	18x70
1261	S849	2434	295.5	18x70
1262	S850	2422	190.5	18x70
1263	S851	2410	85.5	18x70
1264	S852	2398	295.5	18x70
1265	S853	2386	190.5	18x70
1266	S854	2374	85.5	18x70
1267	S855	2362	295.5	18x70
1268	S856	2350	190.5	18x70
1269	S857	2338	85.5	18x70
1270	S858	2326	295.5	18x70
1271	S859	2314	190.5	18x70
1272	S860	2302	85.5	18x70
1273	S861	2290	295.5	18x70
1274	S862	2278	190.5	18x70
1275	S863	2266	85.5	18x70
1276	S864	2254	295.5	18x70
1277	S865	2242	190.5	18x70
1278	S866	2230	85.5	18x70
1279	S867	2218	295.5	18x70
1280	S868	2206	190.5	18x70
1281	S869	2194	85.5	18x70
1282	S870	2182	295.5	18x70
1283	S871	2170	190.5	18x70
1284	S872	2158	85.5	18x70
1285	S873	2146	295.5	18x70
1286	S874	2134	190.5	18x70
1287	S875	2122	85.5	18x70
1288	S876	2110	295.5	18x70
1289	S877	2098	190.5	18x70
1290	S878	2086	85.5	18x70
1291	S879	2074	295.5	18x70
1292	S880	2062	190.5	18x70
1293	S881	2050	85.5	18x70
1294	S882	2038	295.5	18x70
1295	S883	2026	190.5	18x70
1296	S884	2014	85.5	18x70
1297	S885	2002	295.5	18x70
1298	S886	1990	190.5	18x70
1299	S887	1978	85.5	18x70
1300	S888	1966	295.5	18x70
1301	S889	1954	190.5	18x70
1302	S890	1942	85.5	18x70
1303	S891	1930	295.5	18x70
1304	S892	1918	190.5	18x70
1305	S893	1906	85.5	18x70
1306	S894	1894	295.5	18x70
1307	S895	1882	190.5	18x70
1308	S896	1870	85.5	18x70
1309	S897	1858	295.5	18x70
1310	S898	1846	190.5	18x70
1311	S899	1834	85.5	18x70
1312	S900	1822	295.5	18x70
1313	SHIELDING	1810	190.5	18x70
1314	SHIELDING	1798	85.5	18x70
1315	SHIELDING	1786	295.5	18x70
1316	SHIELDING	1726	310.5	40x40
1317	SHIELDING	1646	310.5	40x40
1318	SHIELDING	1566	310.5	40x40
1319	SHIELDING	1486	310.5	40x40
1320	SHIELDING	1406	310.5	40x40
1321	SHIELDING	1326	310.5	40x40
1322	SHIELDING	1246	310.5	40x40
1323	SHIELDING	1166	310.5	40x40
1324	SHIELDING	1086	310.5	40x40
1325	SHIELDING	1006	310.5	40x40
1326	SHIELDING	926	310.5	40x40
1327	SHIELDING	846	310.5	40x40
1328	SHIELDING	766	310.5	40x40
1329	SHIELDING	686	310.5	40x40
1330	SHIELDING	606	310.5	40x40
1331	SHIELDING	526	310.5	40x40
1332	SHIELDING	446	310.5	40x40
1333	SHIELDING	366	310.5	40x40
1334	SHIELDING	286	310.5	40x40
1335	SHIELDING	206	310.5	40x40
1336	SHIELDING	126	310.5	40x40
1337	SHIELDING	46	310.5	40x40
1338	SHIELDING	-34	310.5	40x40
1339	SHIELDING	-114	310.5	40x40
1340	SHIELDING	-194	310.5	40x40
1341	SHIELDING	-274	310.5	40x40
1342	SHIELDING	-354	310.5	40x40
1343	SHIELDING	-434	310.5	40x40
1344	SHIELDING	-514	310.5	40x40
1345	SHIELDING	-594	310.5	40x40
1346	SHIELDING	-674	310.5	40x40
1347	SHIELDING	-754	310.5	40x40
1348	SHIELDING	-834	310.5	40x40
1349	SHIELDING	-914	310.5	40x40
1350	SHIELDING	-994	310.5	40x40
1351	SHIELDING	-1074	310.5	40x40
1352	SHIELDING	-1154	310.5	40x40
1353	SHIELDING	-1234	310.5	40x40
1354	SHIELDING	-1314	310.5	40x40
1355	SHIELDING	-1394	310.5	40x40
1356	SHIELDING	-1474	310.5	40x40
1357	SHIELDING	-1554	310.5	40x40
1358	SHIELDING	-1634	310.5	40x40
1359	SHIELDING	-1714	310.5	40x40
1360	SHIELDING	-1794	310.5	40x40
1361	SHIELDING	-1874	310.5	40x40
1362	SHIELDING	-1954	310.5	40x40
1363	SHIELDING	-2034	310.5	40x40
1364	SHIELDING	-2114	310.5	40x40
1365	SHIELDING	-2194	310.5	40x40
1366	SHIELDING	-2274	310.5	40x40
1367	SHIELDING	-2334	295.5	18x70
1368	SHIELDING	-2346	190.5	18x70
1369	SHIELDING	-2358	85.5	18x70
1370	S901	-2370	295.5	18x70
1371	S902	-2382	190.5	18x70
1372	S903	-2394	85.5	18x70
1373	S904	-2406	295.5	18x70
1374	S905	-2418	190.5	18x70
1375	S906	-2430	85.5	18x70
1376	S907	-2442	295.5	18x70
1377	S908	-2454	190.5	18x70
1378	S909	-2466	85.5	18x70
1379	S910	-2478	295.5	18x70
1380	S911	-2490	190.5	18x70
1381	S912	-2502	85.5	18x70
1382	S913	-2514	295.5	18x70
1383	S914	-2526	190.5	18x70
1384	S915	-2538	85.5	18x70
1385	S916	-2550	295.5	18x70
1386	S917	-2562	190.5	18x70
1387	S918	-2574	85.5	18x70
1388	S919	-2586	295.5	18x70
1389	S920	-2598	190.5	18x70
1390	S921	-2610	85.5	18x70
1391	S922	-2622	295.5	18x70
1392	S923	-2634	190.5	18x70
1393	S924	-2646	85.5	18x70
1394	S925	-2658	295.5	18x70
1395	S926	-2670	190.5	18x70
1396	S927	-2682	85.5	18x70
1397	S928	-2694	295.5	18x70
1398	S929	-2706	190.5	18x70
1399	S930	-2718	85.5	18x70
1400	S931	-2730	295.5	18x70
1401	S932	-2742	190.5	18x70
1402	S933	-2754	85.5	18x70
1403	S934	-2766	295.5	18x70
1404	S935	-2778	190.5	18x70
1405	S936	-2790	85.5	18x70
1406	S937	-2802	295.5	18x70
1407	S938	-2814	190.5	18x70
1408	S939	-2826	85.5	18x70
1409	S940	-2838	295.5	18x70
1410	S941	-2850	190.5	18x70
1411	S942	-2862	85.5	18x70
1412	S943	-2874	295.5	18x70
1413	S944	-2886	190.5	18x70
1414	S945	-2898	85.5	18x70
1415	S946	-2910	295.5	18x70
1416	S947	-2922	190.5	18x70
1417	S948	-2934	85.5	18x70
1418	S949	-2946	295.5	18x70
1419	S950	-2958	190.5	18x70
1420	S951	-2970	85.5	18x70
1421	S952	-2982	295.5	18x70
1422	S953	-2994	190.5	18x70
1423	S954	-3006	85.5	18x70
1424	S955	-3018	295.5	18x70
1425	S956	-3030	190.5	18x70
1426	S957	-3042	85.5	18x70
1427	S958	-3054	295.5	18x70
1428	S959	-3066	190.5	18x70
1429	S960	-3078	85.5	18x70
1430	S961	-3090	295.5	18x70
1431	S962	-3102	190.5	18x70
1432	S963	-3114	85.5	18x70
1433	S964	-3126	295.5	18x70
1434	S965	-3138	190.5	18x70
1435	S966	-3150	85.5	18x70
1436	S967	-3162	295.5	18x70
1437	S968	-3174	190.5	18x70
1438	S969	-3186	85.5	18x70
1439	S970	-3198	295.5	18x70
1440	S971	-3210	190.5	18x70

No.	Name	X	Y	Bump size
1441	S972	-3222	85.5	18x70
1442	S973	-3234	295.5	18x70
1443	S974	-3246	190.5	18x70
1444	S975	-3258	85.5	18x70
1445	S976	-3270	295.5	18x70
1446	S977	-3282	190.5	18x70
1447	S978	-3294	85.5	18x70
1448	S979	-3306	295.5	18x70
1449	S980	-3318	190.5	18x70
1450	S981	-3330	85.5	18x70
1451	S982	-3342	295.5	18x70
1452	S983	-3354	190.5	18x70
1453	S984	-3366	85.5	18x70
1454	S985	-3378	295.5	18x70
1455	S986	-3390	190.5	18x70
1456	S987	-3402	85.5	18x70
1457	S988	-3414	295.5	18x70
1458	S989	-3426	190.5	18x70
1459	S990	-3438	85.5	18x70
1460	S991	-3450	295.5	18x70
1461	S992	-3462	190.5	18x70
1462	S993	-3474	85.5	18x70
1463	S994	-3486	295.5	18x70
1464	S995	-3498	190.5	18x70
1465	S996	-3510	85.5	18x70
1466	S997	-3522	295.5	18x70
1467	S998	-3534	190.5	18x70
1468	S999	-3546	85.5	18x70
1469	S1000	-3558	295.5	18x70
1470	S1001	-3570	190.5	18x70
1471	S1002	-3582	85.5	18x70
1472	S1003	-3594	295.5	18x70
1473	S1004	-3606	190.5	18x70
1474	S1005	-3618	85.5	18x70
1475	S1006	-3630	295.5	18x70
1476	S1007	-3642	190.5	18x70
1477	S1008	-3654	85.5	18x70
1478	S1009	-3666	295.5	18x70
1479	S1010	-3678	190.5	18x70
1480	S1011	-3690	85.5	18x70
1481	S1012	-3702	295.5	18x70
1482	S1013	-3714	190.5	18x70
1483	S1014	-3726	85.5	18x70
1484	S1015	-3738	295.5	18x70
1485	S1016	-3750	190.5	18x70
1486	S1017	-3762	85.5	18x70
1487	S1018	-3774	295.5	18x70
1488	S1019	-3786	190.5	18x70
1489	S1020	-3798	85.5	18x70
1490	S1021	-3810	295.5	18x70
1491	S1022	-3822	190.5	18x70
1492	S1023	-3834	85.5	18x70
1493	S1024	-3846	295.5	18x70
1494	S1025	-3858	190.5	18x70
1495	S1026	-3870	85.5	18x70
1496	S1027	-3882	295.5	18x70
1497	S1028	-3894	190.5	18x70
1498	S1029	-3906	85.5	18x70
1499	S1030	-3918	295.5	18x70
1500	S1031	-3930	190.5	18x70
1501	S1032	-3942	85.5	18x70
1502	S1033	-3954	295.5	18x70
1503	S1034	-3966	190.5	18x70
1504	S1035	-3978	85.5	18x70
1505	S1036	-3990	295.5	18x70
1506	S1037	-4002	190.5	18x70
1507	S1038	-4014	85.5	18x70
1508	S1039	-4026	295.5	18x70
1509	S1040	-4038	190.5	18x70
1510	S1041	-4050	85.5	18x70
1511	S1042	-4062	295.5	18x70
1512	S1043	-4074	190.5	18x70
1513	S1044	-4086	85.5	18x70
1514	S1045	-4098	295.5	18x70
1515	S1046	-4110	190.5	18x70
1516	S1047	-4122	85.5	18x70
1517	S1048	-4134	295.5	18x70
1518	S1049	-4146	190.5	18x70
1519	S1050	-4158	85.5	18x70
1520	S1051	-4170	295.5	18x70
1521	S1052	-4182	190.5	18x70
1522	S1053	-4194	85.5	18x70
1523	S1054	-4206	295.5	18x70
1524	S1055	-4218	190.5	18x70
1525	S1056	-4230	85.5	18x70
1526	S1057	-4242	295.5	18x70
1527	S1058	-4254	190.5	18x70
1528	S1059	-4266	85.5	18x70
1529	S1060	-4278	295.5	18x70
1530	S1061	-4290	190.5	18x70
1531	S1062	-4302	85.5	18x70
1532	S1063	-4314	295.5	18x70
1533	S1064	-4326	190.5	18x70
1534	S1065	-4338	85.5	18x70
1535	S1066	-4350	295.5	18x70
1536	S1067	-4362	190.5	18x70
1537	S1068	-4374	85.5	18x70
1538	S1069	-4386	295.5	18x70
1539	S1070	-4398	190.5	18x70
1540	S1071	-4410	85.5	18x70
1541	S1072	-4422	295.5	18x70
1542	S1073	-4434	190.5	18x70
1543	S1074	-4446	85.5	18x70
1544	S1075	-4458	295.5	18x70
1545	S1076	-4470	190.5	18x70
1546	S1077	-4482	85.5	18x70
1547	S1078	-4494	295.5	18x70
1548	S1079	-4506	190.5	18x70
1549	S1080	-4518	85.5	18x70
1550	S1081	-4530	295.5	18x70
1551	S1082	-4542	190.5	18x70
1552	S1083	-4554	85.5	18x70
1553	S1084	-4566	295.5	18x70
1554	S1085	-4578	190.5	18x70
1555	S1086	-4590	85.5	18x70
1556	S1087	-4602	295.5	18x70
1557	S1088	-4614	190.5	18x70
1558	S1089	-4626	85.5	18x70
1559	S1090	-4638	295.5	18x70
1560	S1091	-4650	190.5	18x70
1561	S1052	-4182	190.5	18x70
1562	S1053	-4194	85.5	18x70
1563	S1054	-4206	295.5	18x70
1564	S1055	-4218	190.5	18x70
1565	S1056	-4230	85.5	18x70
1566	S1057	-4242	295.5	18x70
1567	S1058	-4254	190.5	18x70
1568	S1059	-4266	85.5	18x70
1569	S1060	-4278	295.5	18x70
1570	S1061	-4290	190.5	18x70
1571	S1062	-4302	85.5	18x70
1572	S1063	-4314	295.5	18x70
1573	S1064	-4326	190.5	18x70
1574	S1065	-4338	85.5	18x70
1575	S1066	-4350	295.5	18x70
1576	S1067	-4362	190.5	18x70
1577	S1068	-4374	85.5	18x70
1578	S1069	-4386	295.5	18x70
1579	S1070	-4398	190.5	18x70
1580	S1071	-4410	85.5	18x70
1581	S1072	-4422	295.5	18x70
1582	S1073	-4434	190.5	18x70
1583	S1074	-4446	85.5	18x70
1584	S1075	-4458	295.5	18x70
1585	S1076	-4470	190.5	18x70
1586	S1077	-4482	85.5	18x70
1587	S1078	-4494	295.5	18x70
1588	S1079	-4506	190.5	18x70
1589	S1080	-4518	85.5	18x70
1590	S1081	-4530	295.5	18x70
1591	S1082	-4542	190.5	18x70
1592	S1083	-4554	85.5	18x70
1593	S1084	-4566	295.5	18x70
1594	S1085	-4578	190.5	18x70
1595	S1086	-4590	85.5	18x70
1596	S1087	-4602	295.5	18x70
1597	S1088	-4614	190.5	18x70
1598	S1089	-4626	85.5	18x70
1599	S1090	-4638	295.5	18x70
1600	S1091	-4650	190.5	18x70
1601	S1092	-4662	85.5	18x70
1602	S1093	-4674	295.5	18x70
1603	S1094	-4686	190.5	18x70
1604	S1095	-4698	85.5	18x70
1605	S1096	-4710	295.5	18x70
1606	S1097	-4722	190.5	18x70
1607	S1098	-4734	85.5	18x70
1608	S1099	-4746	295.5	18x70
1609	S1100	-4758	190.5	18x70
1610	S1101	-4770	85.5	18x70
1611	S1102	-4782	295.5	18x70
1612	S1103	-4794	190.5	18x70
1613	S1104	-4806	85.5	18x70
1614	S1105	-4818	295.5	18x70
1615	S1106	-4830	190.5	18x70
1616	S1107	-4842	85.5	18x70
1617	S1108	-4854	295.5	18x70
1618	S1109	-4866	190.5	18x70
1619	S1110	-4878	85.5	18x70
1620	S1111	-4890	295.5	18x70
1621	S1112	-4902	190.5	18x70
1622	S1113	-4914	85.5	18x70
1623	S1114	-4926	295.5	18x70
1624	S1115	-4938	190.5	18x70
1625	S1116	-4950	85.5	18x70
1626	S1117	-4962	295.5	18x70
1627	S1118	-4974	190.5	18x70
1628	S1119	-4986	85.5	18x70
1629	S1120	-4998	295.5	18x70
1630	S1121	-5010	190.5	18x70
1631	S1122	-5022	85.5	18x70
1632	S1123	-5034	295.5	18x70
1633	S1124	-5046	190.5	18x70
1634	S1125	-5058	85.5	18x70
1635	S1126	-5070	295.5	18x70
1636	S1127	-5082	190.5	18x70
1637	S1128	-5094	85.5	18x70
1638	S1129	-5106	295.5	18x70
1639	S1130	-5118	190.5	18x70
1640	S1131	-5130	85.5	18x70
1641	S1132	-5142	295.5	18x70
1642	S1133	-5154	190.5	18x70
1643	S1134	-5166	85.5	18x70
1644	S1135	-5178	295.5	18x70
1645	S1136	-5190	190.5	18x70
1646	S1137	-5202	85.5	18x70
1647	S1138	-5214	295.5	18x70
1648	S1139	-5226	190.5	18x70
1649	S1140	-5238	85.5	18x70
1650	S1141	-5250	295.5	18x70
1651	S1142	-5262	190.5	18x70
1652	S1143	-5274	85.5	18x70
1653	S1144	-5286	295.5	18x70
1654	S1145	-5298	190.5	18x70
1655	S1146	-5310	85.5	18x70
1656	S1147	-5322	295.5	18x70
1657	S1148	-5334	190.5	18x70
1658	S1149	-5346	85.5	18x70
1659	S1150	-5358	295.5	18x70
1660	S1151	-5370	190.5	18x70
1661	S1152	-5382	85.5	18x70
1662	S1153	-5394	295.5	18x70
1663	S1154	-5406	190.5	18x70
1664	S1155	-5418	85.5	18x70
1665	S1156	-5430	295.5	18x70
1666	S1157	-5442	190.5	18x70
1667	S1158	-5454	85.5	18x70
1668	S1159	-5466	295.5	18x70
1669	S1160	-5478	190.5	18x70
1670	S1161	-5490	85.5	18x70
1671	S1162	-5502	295.5	18x70
1672	S1163	-5514	190.5	18x70
1673	S1164	-5526	85.5	18x70
1674	S1165	-5538	295.5	18x70
1675	S1166	-5550	190.5	18x70
1676	S1167	-5562	85.5	18x70
1677	S1168	-5574	295.5	18x70
1678	S1169	-5586	190.5	18x70
1679	S1170	-5598	85.5	18x70
1680	S1171	-5610	295.5	18x70

No.	Name	X	Y	Bump size
1681	S1212	-6102	85.5	18x70
1682	S1213	-6114	295.5	18x70
1683	S1214	-6126	190.5	18x70
1684	S1215	-6138	85.5	18x70
1685	S1216	-6150	295.5	18x70
1686	S1217	-6162	190.5	18x70
1687	S1218	-6174	85.5	18x70
1688	S1219	-6186	295.5	18x70
1689	S1220	-6198	190.5	18x70
1690	S1221	-6210	85.5	18x70
1691	S1222	-6222	295.5	18x70
1692	S1223	-6234	190.5	18x70
1693	S1224	-6246	85.5	18x70
1694	S1225	-6258	295.5	18x70
1695	S1226	-6270	190.5	18x70
1696	S1227	-6282	85.5	18x70
1697	S1228	-6294	295.5	18x70
1698	S1229	-6306	190.5	18x70
1699	S1230	-6318	85.5	18x70
1700	S1231	-6330	295.5	18x70
1701	S1232	-6342	190.5	18x70
1702	S1233	-6354	85.5	18x70
1703	S1234	-6366	295.5	18x70
1704	S1235	-6378	190.5	18x70
1705	S1236	-6390	85.5	18x70
1706	S1237	-6402	295.5	18x70
1707	S1238	-6414	190.5	18x70
1708	S1239	-6426	85.5	18x70
1709	S1240	-6438	295.5	18x70
1710	S1241	-6450	190.5	18x70
1711	S1242	-6462	85.5	18x70
1712	S1243	-6474	295.5	18x70
1713	S1244	-6486	190.5	18x70
1714	S1245	-6498	85.5	18x70
1715	S1246	-6510	295.5	18x70
1716	S1247	-6522	190.5	18x70
1717	S1248	-6534	85.5	18x70
1718	S1249	-6546	295.5	18x70
1719	S1250	-6558	190.5	18x70
1720	S1251	-6570	85.5	18x70
1721	S1252	-6582	295.5	18x70
1722	S1253	-6594	190.5	18x70
1723	S1254	-6606	85.5	18x70
1724	S1255	-6618	295.5	18x70
1725	S1256	-6630	190.5	18x70
1726	S1257	-6642	85.5	18x70
1727	S1258	-6654	295.5	18x70
1728	S1259	-6666	190.5	18x70
1729	S1260	-6678	85.5	18x70
1730	S1261	-6690	295.5	18x70
1731	S1262	-6702	190.5	18x70
1732	S1263	-6714	85.5	18x70
1733	S1264	-6726	295.5	18x70
1734	S1265	-6738	190.5	18x70
1735	S1266	-6750	85.5	18x70
1736	S1267	-6762	295.5	18x70
1737	S1268	-6774	190.5	18x70
1738	S1269	-6786	85.5	18x70
1739	S1270	-6798	295.5	18x70
1740	S1271	-6810	190.5	18x70
1741	S1272	-6822	85.5	18x70
1742	S1273	-6834	295.5	18x70
1743	S1274	-6846	190.5	18x70
1744	S1275	-6858	85.5	18x70
1745	S1276	-6870	295.5	18x70
1746	S1277	-6882	190.5	18x70
1747	S1278	-6894	85.5	18x70
1748	S1279	-6906	295.5	18x70
1749	S1280	-6918	190.5	18x70
1750	S1281	-6930	85.5	18x70
1751	S1282	-6942	295.5	18x70
1752	S1283	-6954	190.5	18x70
1753	S1284	-6966	85.5	18x70
1754	S1285	-6978	295.5	18x70
1755	S1286	-6990	190.5	18x70
1756	S1287	-7002	85.5	18x70
1757	S1288	-7014	295.5	18x70
1758	S1289	-7026	190.5	18x70
1759	S1290	-7038	85.5	18x70
1760	S1291	-7050	295.5	18x70
1761	S1292	-7062	190.5	18x70
1762	S1293	-7074	85.5	18x70
1763	S1294	-7086	295.5	18x70
1764	S1295	-7098	190.5	18x70
1765	S1296	-7110	85.5	18x70
1766	S1297	-7122	295.5	18x70
1767	S1298	-7134	190.5	18x70
1768	S1299	-7146	85.5	18x70
1769	S1300	-7158	295.5	18x70
1770	S1301	-7170	190.5	18x70
1771	S1302	-7182	85.5	18x70
1772	S1303	-7194	295.5	18x70
1773	S1304	-7206	190.5	18x70
1774	S1305	-7218	85.5	18x70
1775	S1306	-7230	295.5	18x70
1776	S1307	-7242	190.5	18x70
1777	S1308	-7254	85.5	18x70
1778	S1309	-7266	295.5	18x70
1779	S1310	-7278	190.5	18x70
1780	S1311	-7290	85.5	18x70
1781	S1312	-7302	295.5	18x70
1782	S1313	-7314	190.5	18x70
1783	S1314	-7326	85.5	18x70
1784	S1315	-7338	295.5	18x70
1785	S1316	-7350	190.5	18x70
1786	S1317	-7362	85.5	18x70
1787	S1318	-7374	295.5	18x70
1788	S1319	-7386	190.5	18x70
1789	S1320	-7398	85.5	18x70
1790	S1321	-7410	295.5	18x70
1791	S1322	-7422	190.5	18x70
1792	S1323	-7434	85.5	18x70
1793	S1324	-7446	295.5	18x70
1794	S1325	-7458	190.5	18x70
1795	S1326	-7470	85.5	18x70
1796	S1327	-7482	295.5	18x70
1797	S1328	-7494	190.5	18x70
1798	S1329	-7506	85.5	18x70
1799	S1330	-7518	295.5	18x70
1800	S1331	-7530	190.5	18x70
1801	S1332	-7542	85.5	18x70
1802	S1333	-7554	295.5	18x70
1803	S1334	-7566	190.5	18x70
1804	S1335	-7578	85.5	18x70
1805	S1336	-7590	295.5	18x70
1806	S1337	-7602	190.5	18x70
1807	S1338	-7614	85.5	18x70
1808	S1339	-7626	295.5	18x70
1809	S1340	-7638	190.5	18x70
1810	S1341	-7650	85.5	18x70
1811	S1342	-7662	295.5	18x70
1812	S1343	-7674	190.5	18x70
1813	S1344	-7686	85.5	18x70
1814	S1345	-7698	295.5	18x70
1815	S1346	-7710	190.5	18x70
1816	S1347	-7722	85.5	18x70
1817	S1348	-7734	295.5	18x70
1818	S1349	-7746	190.5	18x70
1819	S1350	-7758	85.5	18x70
1820	S1351	-7770	295.5	18x70
1821	S1352	-7782	190.5	18x70
1822	S1353	-7794	85.5	18x70
1823	S1354	-7806	295.5	18x70
1824	S1355	-7818	190.5	18x70
1825	S1356	-7830	85.5	18x70
1826	S1357	-7842	295.5	18x70
1827	S1358	-7854	190.5	18x70
1828	S1359	-7866	85.5	18x70
1829	S1360	-7878	295.5	18x70
1830	S1361	-7890	190.5	18x70
1831	S1362	-7902	85.5	18x70
1832	S1363	-7914	295.5	18x70
1833	S1364	-7926	190.5	18x70
1834	S1365	-7938	85.5	18x70
1835	S1366	-7950	295.5	18x70
1836	S1367	-7962	190.5	18x70
1837	S1368	-7974	85.5	18x70
1838	S1369	-7986	295.5	18x70
1839	S1370	-7998	190.5	18x70
1840	S1371	-8010	85.5	18x70
1841	S1372	-8022	295.5	18x70
1842	S1373	-8034	190.5	18x70
1843	S1374	-8046	85.5	18x70
1844	S1375	-8058	295.5	18x70
1845	S1376	-8070	190.5	18x70
1846	S1377	-8082	85.5	18x70
1847	S1378	-8094	295.5	18x70
1848	S1379	-8106	190.5	18x70
1849	S1380	-8118	85.5	18x70
1850	S1381	-8130	295.5	18x70
1851	S1382	-8142	190.5	18x70
1852	S1383	-8154	85.5	18x70
1853	S1384	-8166	295.5	18x70
1854	S1385	-8178	190.5	18x70
1855	S1386	-8190	85.5	18x70
1856	S1387	-8202	295.5	18x70
1857	S1388	-8214	190.5	18x70
1858	S1389	-8226	85.5	18x70
1859	S1390	-8238	295.5	18x70
1860	S1391	-8250	190.5	18x70
1861	S1392	-8262	85.5	18x70
1862	S1393	-8274	295.5	18x70
1863	S1394	-8286	190.5	18x70
1864	S1395	-8298	85.5	18x70
1865	S1396	-8310	295.5	18x70
1866	S1397	-8322	190.5	18x70
1867	S1398	-8334	85.5	18x70
1868	S1399	-8346	295.5	18x70
1869	S1400	-8358	190.5	18x70
1870	S1401	-8370	85.5	18x70
1871	S1402	-8382	295.5	18x70
1872	S1403	-8394	190.5	18x70
1873	S1404	-8406	85.5	18x70
1874	S1405	-8418	295.5	18x70
1875	S1406	-8430	190.5	18x70
1876	S1407	-8442	85.5	18x70
1877	S1408	-8454	295.5	18x70
1878	S1409	-8466	190.5	18x70
1879	S1410	-8478	85.5	18x70
1880	S1411	-8490	295.5	18x70
1881	S1412	-8502	190.5	18x70
1882	S1413	-8514	85.5	18x70
1883	S1414	-8526	295.5	18x70
1884	S1415	-8538	190.5	18x70
1885	S1416	-8550	85.5	18x70
1886	S1417	-8562	295.5	18x70
1887	S1418	-8574	190.5	18x70
1888	S1419	-8586	85.5	18x70
1889	S1420	-8598	295.5	18x70
1890	S1421	-8610	190.5	18x70
1891	S1422	-8622	85.5	18x70
1892	S1423	-8634	295.5	18x70
1893	S1424	-8646	190.5	18x70
1894	S1425	-8658	85.5	18x70
1895	S1426	-8670	295.5	18x70
1896	S1427	-8682	190.5	18x70
1897	S1428	-8694	85.5	18x70
1898	S1429	-8706	295.5	18x70
1899	S1430	-8718	190.5	18x70
1900	S1431	-8730	85.5	18x70
1901	S1432	-8742	295.5	18x70
1902	S1433	-8754	190.5	18x70
1903	S1434	-8766	85.5	18x70
1904	S1435	-8778	295.5	18x70
1905	S1436	-8790	190.5	18x70
1906	S1437	-8802	85.5	18x70
1907	S1438	-8814	295.5	18x70
1908	S1439	-8826	190.5	18x70
1909	S1440	-8838	85.5	18x70
1910	S1441	-8850	295.5	18x70
1911	S1442	-8862	190.5	18x70
1912	S1443	-8874	85.5	18x70
1913	S1444	-8886	295.5	18x70
1914	S1445	-8898	190.5	18x70
1915	S1446	-8910	85.5	18x70
1916	S1447	-8922	295.5	18x70
1917	S1448	-8934	190.5	18x70
1918	S1449	-8946	85.5	18x70
1919	S1450	-8958	295.5	18x70
1920	S1451	-8970	190.5	18x70

No.	Name	X	Y	Bump size
1921	S1452	-8982	85.5	18x70
1922	S1453	-8994	295.5	18x70
1923	S1454	-9006	190.5	18x70
1924	S1455	-9018	85.5	18x70
1925	S1456	-9030	295.5	18x70
1926	S1457	-9042	190.5	18x70
1927	S1458	-9054	85.5	18x70
1928	S1459	-9066	295.5	18x70
1929	S1460	-9078	190.5	18x70
1930	S1461	-9090	85.5	18x70
1931	S1462	-9102	295.5	18x70
1932	S1463	-9114	190.5	18x70
1933	S1464	-9126	85.5	18x70
1934	S1465	-9138	295.5	18x70
1935	S1466	-9150	190.5	18x70
1936	S1467	-9162	85.5	18x70
1937	S1468	-9174	295.5	18x70
1938	S1469	-9186	190.5	18x70
1939	S1470	-9198	85.5	18x70
1940	S1471	-9210	295.5	18x70
1941	S1472	-9222	190.5	18x70
1942	S1473	-9234	85.5	18x70
1943	S1474	-9246	295.5	18x70
1944	S1475	-9258	190.5	18x70
1945	S1476	-9270	85.5	18x70
1946	S1477	-9282	295.5	18x70
1947	S1478	-9294	190.5	18x70
1948	S1479	-9306	85.5	18x70
1949	S1480	-9318	295.5	18x70
1950	S1481	-9330	190.5	18x70
1951	S1482	-9342	85.5	18x70
1952	S1483	-9354	295.5	18x70
1953	S1484	-9366	190.5	18x70
1954	S1485	-9378	85.5	18x70
1955	S1486	-9390	295.5	18x70
1956	S1487	-9402	190.5	18x70
1957	S1488	-9414	85.5	18x70
1958	S1489	-9426	295.5	18x70
1959	S1490	-9438	190.5	18x70
1960	S1491	-9450	85.5	18x70
1961	S1492	-9462	295.5	18x70
1962	S1493	-9474	190.5	18x70
1963	S1494	-9486	85.5	18x70
1964	S1495	-9498	295.5	18x70
1965	S1496	-9510	190.5	18x70
1966	S1497	-9522	85.5	18x70
1967	S1498	-9534	295.5	18x70
1968	S1499	-9546	190.5	18x70
1969	S1500	-9558	85.5	18x70
1970	S1501	-9570	295.5	18x70
1971	S1502	-9582	190.5	18x70
1972	S1503	-9594	85.5	18x70
1973	S1504	-9606	295.5	18x70
1974	S1505	-9618	190.5	18x70
1975	S1506	-9630	85.5	18x70
1976	S1507	-9642	295.5	18x70
1977	S1508	-9654	190.5	18x70
1978	S1509	-9666	85.5	18x70
1979	S1510	-9678	295.5	18x70
1980	S1511	-9690	190.5	18x70
1981	S1512	-9702	85.5	18x70
1982	S1513	-9714	295.5	18x70
1983	S1514	-9726	190.5	18x70
1984	S1515	-9738	85.5	18x70
1985	S1516	-9750	295.5	18x70
1986	S1517	-9762	190.5	18x70
1987	S1518	-9774	85.5	18x70
1988	S1519	-9786	295.5	18x70
1989	S1520	-9798	190.5	18x70
1990	S1521	-9810	85.5	18x70
1991	S1522	-9822	295.5	18x70
1992	S1523	-9834	190.5	18x70
1993	S1524	-9846	85.5	18x70
1994	S1525	-9858	295.5	18x70
1995	S1526	-9870	190.5	18x70
1996	S1527	-9882	85.5	18x70
1997	S1528	-9894	295.5	18x70
1998	S1529	-9906	190.5	18x70
1999	S1530	-9918	85.5	18x70
2000	S1531	-9930	295.5	18x70

No.	Name	X	Y	Bump size
2001	S1532	-9942	190.5	18x70
2002	S1533	-9954	85.5	18x70
2003	S1534	-9966	295.5	18x70
2004	S1535	-9978	190.5	18x70
2005	S1536	-9990	85.5	18x70
2006	S1537	-10002	295.5	18x70
2007	S1538	-10014	190.5	18x70
2008	S1539	-10026	85.5	18x70
2009	S1540	-10038	295.5	18x70
2010	S1541	-10050	190.5	18x70
2011	S1542	-10062	85.5	18x70
2012	S1543	-10074	295.5	18x70
2013	S1544	-10086	190.5	18x70
2014	S1545	-10098	85.5	18x70
2015	S1546	-10110	295.5	18x70
2016	S1547	-10122	190.5	18x70
2017	S1548	-10134	85.5	18x70
2018	S1549	-10146	295.5	18x70
2019	S1550	-10158	190.5	18x70
2020	S1551	-10170	85.5	18x70
2021	S1552	-10182	295.5	18x70
2022	S1553	-10194	190.5	18x70
2023	S1554	-10206	85.5	18x70
2024	S1555	-10218	295.5	18x70
2025	S1556	-10230	190.5	18x70
2026	S1557	-10242	85.5	18x70
2027	S1558	-10254	295.5	18x70
2028	S1559	-10266	190.5	18x70
2029	S1560	-10278	85.5	18x70
2030	S1561	-10290	295.5	18x70
2031	S1562	-10302	190.5	18x70
2032	S1563	-10314	85.5	18x70
2033	S1564	-10326	295.5	18x70
2034	S1565	-10338	190.5	18x70
2035	S1566	-10350	85.5	18x70
2036	S1567	-10362	295.5	18x70
2037	S1568	-10374	190.5	18x70
2038	S1569	-10386	85.5	18x70
2039	S1570	-10398	295.5	18x70
2040	S1571	-10410	190.5	18x70
2041	S1572	-10422	85.5	18x70
2042	S1573	-10434	295.5	18x70
2043	S1574	-10446	190.5	18x70
2044	S1575	-10458	85.5	18x70
2045	S1576	-10470	295.5	18x70
2046	S1577	-10482	190.5	18x70
2047	S1578	-10494	85.5	18x70
2048	S1579	-10506	295.5	18x70
2049	S1580	-10518	190.5	18x70
2050	S1581	-10530	85.5	18x70
2051	S1582	-10542	295.5	18x70
2052	S1583	-10554	190.5	18x70
2053	S1584	-10566	85.5	18x70
2054	S1585	-10578	295.5	18x70
2055	S1586	-10590	190.5	18x70
2056	S1587	-10602	85.5	18x70
2057	S1588	-10614	295.5	18x70
2058	S1589	-10626	190.5	18x70
2059	S1590	-10638	85.5	18x70
2060	S1591	-10650	295.5	18x70
2061	S1592	-10662	190.5	18x70
2062	S1593	-10674	85.5	18x70
2063	S1594	-10686	295.5	18x70
2064	S1595	-10698	190.5	18x70
2065	S1596	-10710	85.5	18x70
2066	S1597	-10722	295.5	18x70
2067	S1598	-10734	190.5	18x70
2068	S1599	-10746	85.5	18x70
2069	S1600	-10758	295.5	18x70
2070	S1601	-10770	190.5	18x70
2071	S1602	-10782	85.5	18x70
2072	S1603	-10794	295.5	18x70
2073	S1604	-10806	190.5	18x70
2074	S1605	-10818	85.5	18x70
2075	S1606	-10830	295.5	18x70
2076	S1607	-10842	190.5	18x70
2077	S1608	-10854	85.5	18x70
2078	S1609	-10866	295.5	18x70
2079	S1610	-10878	190.5	18x70
2080	S1611	-10890	85.5	18x70

No.	Name	X	Y	Bump size
2081	S1612	-10902	295.5	18x70
2082	S1613	-10914	190.5	18x70
2083	S1614	-10926	85.5	18x70
2084	S1615	-10938	295.5	18x70
2085	S1616	-10950	190.5	18x70
2086	S1617	-10962	85.5	18x70
2087	S1618	-10974	295.5	18x70
2088	S1619	-10986	190.5	18x70
2089	S1620	-10998	85.5	18x70
2090	S1621	-11010	295.5	18x70
2091	S1622	-11022	190.5	18x70
2092	S1623	-11034	85.5	18x70
2093	S1624	-11046	295.5	18x70
2094	S1625	-11058	190.5	18x70
2095	S1626	-11070	85.5	18x70
2096	S1627	-11082	295.5	18x70
2097	S1628	-11094	190.5	18x70
2098	S1629	-11106	85.5	18x70
2099	S1630	-11118	295.5	18x70
2100	S1631	-11130	190.5	18x70
2101	S1632	-11142	85.5	18x70
2102	S1633	-11154	295.5	18x70
2103	S1634	-11166	190.5	18x70
2104	S1635	-11178	85.5	18x70
2105	S1636	-11190	295.5	18x70
2106	S1637	-11202	190.5	18x70
2107	S1638	-11214	85.5	18x70
2108	S1639	-11226	295.5	18x70
2109	S1640	-11238	190.5	18x70
2110	S1641	-11250	85.5	18x70
2111	S1642	-11262	295.5	18x70
2112	S1643	-11274	190.5	18x70
2113	S1644	-11286	85.5	18x70
2114	S1645	-11298	295.5	18x70
2115	S1646	-11310	190.5	18x70
2116	S1647	-11322	85.5	18x70
2117	S1648	-11334	295.5	18x70
2118	S1649	-11346	190.5	18x70
2119	S1650	-11358	85.5	18x70
2120	S1651	-11370	295.5	18x70
2121	S1652	-11382	190.5	18x70
2122	S1653	-11394	85.5	18x70
2123	S1654	-11406	295.5	18x70
2124	S1655	-11418	190.5	18x70
2125	S1656	-11430	85.5	18x70
2126	S1657	-11442	295.5	18x70
2127	S1658	-11454	190.5	18x70
2128	S1659	-11466	85.5	18x70
2129	S1660	-11478	295.5	18x70
2130	S1661	-11490	190.5	18x70
2131	S1662	-11502	85.5	18x70
2132	S1663	-11514	295.5	18x70
2133	S1664	-11526	190.5	18x70
2134	S1665	-11538	85.5	18x70
2135	S1666	-11550	295.5	18x70
2136	S1667	-11562	190.5	18x70
2137	S1668	-11574	85.5	18x70
2138	S1669	-11586	295.5	18x70
2139	S1670	-11598	190.5	18x70
2140	S1671	-11610	85.5	18x70
2141	S1672	-11622	295.5	18x70
2142	S1673	-11634	190.5	18x70
2143	S1674	-11646	85.5	18x70
2144	S1675	-11658	295.5	18x70
2145	S1676	-11670	190.5	18x70
2146	S1677	-11682	85.5	18x70
2147	S1678	-11694	295.5	18x70
2148	S1679	-11706	190.5	18x70
2149	S1680	-11718	85.5	18x70
2150	S1681	-11730	295.5	18x70
2151	S1682	-11742	190.5	18x70
2152	S1683	-11754	85.5	18x70
2153	S1684	-11766	295.5	18x70
2154	S1685	-11778	190.5	18x70
2155	S1686	-11790	85.5	18x70
2156	S1687	-11802	295.5	18x70
2157	S1688	-11814	190.5	18x70
2158	S1689	-11826	85.5	18x70
2159	S1690	-11838	295.5	18x70
2160	S1691	-11850	190.5	18x70

No.	Name	X	Y	Bump size
2161	S1692	-11862	85.5	18x70
2162	S1693	-11874	295.5	18x70
2163	S1694	-11886	190.5	18x70
2164	S1695	-11898	85.5	18x70
2165	S1696	-11910	295.5	18x70
2166	S1697	-11922	190.5	18x70
2167	S1698	-11934	85.5	18x70
2168	S1699	-11946	295.5	18x70
2169	S1700	-11958	190.5	18x70
2170	S1701	-11970	85.5	18x70
2171	S1702	-11982	295.5	18x70
2172	S1703	-11994	190.5	18x70
2173	S1704	-12006	85.5	18x70
2174	S1705	-12018	295.5	18x70
2175	S1706	-12030	190.5	18x70
2176	S1707	-12042	85.5	18x70
2177	S1708	-12054	295.5	18x70
2178	S1709	-12066	190.5	18x70
2179	S1710	-12078	85.5	18x70
2180	S1711	-12090	295.5	18x70
2181	S1712	-12102	190.5	18x70
2182	S1713	-12114	85.5	18x70
2183	S1714	-12126	295.5	18x70
2184	S1715	-12138	190.5	18x70
2185	S1716	-12150	85.5	18x70
2186	S1717	-12162	295.5	18x70
2187	S1718	-12174	190.5	18x70
2188	S1719	-12186	85.5	18x70
2189	S1720	-12198	295.5	18x70
2190	S1721	-12210	190.5	18x70
2191	S1722	-12222	85.5	18x70
2192	S1723	-12234	295.5	18x70
2193	S1724	-12246	190.5	18x70
2194	S1725	-12258	85.5	18x70
2195	S1726	-12270	295.5	18x70
2196	S1727	-12282	190.5	18x70
2197	S1728	-12294	85.5	18x70
2198	S1729	-12306	295.5	18x70
2199	S1730	-12318	190.5	18x70
2200	S1731	-12330	85.5	18x70
2201	S1732	-12342	295.5	18x70
2202	S1733	-12354	190.5	18x70
2203	S1734	-12366	85.5	18x70
2204	S1735	-12378	295.5	18x70
2205	S1736	-12390	190.5	18x70
2206	S1737	-12402	85.5	18x70
2207	S1738	-12414	295.5	18x70
2208	S1739	-12426	190.5	18x70
2209	S1740	-12438	85.5	18x70
2210	S1741	-12450	295.5	18x70
2211	S1742	-12462	190.5	18x70
2212	S1743	-12474	85.5	18x70
2213	S1744	-12486	295.5	18x70
2214	S1745	-12498	190.5	18x70
2215	S1746	-12510	85.5	18x70
2216	S1747	-12522	295.5	18x70
2217	S1748	-12534	190.5	18x70
2218	S1749	-12546	85.5	18x70
2219	S1750	-12558	295.5	18x70
2220	S1751	-12570	190.5	18x70
2221	S1752	-12582	85.5	18x70
2222	S1753	-12594	295.5	18x70
2223	S1754	-12606	190.5	18x70
2224	S1755	-12618	85.5	18x70
2225	S1756	-12630	295.5	18x70
2226	S1757	-12642	190.5	18x70
2227	S1758	-12654	85.5	18x70
2228	S1759	-12666	295.5	18x70
2229	S1760	-12678	190.5	18x70
2230	S1761	-12690	85.5	18x70
2231	S1762	-12702	295.5	18x70
2232	S1763	-12714	190.5	18x70
2233	S1764	-12726	85.5	18x70
2234	S1765	-12738	295.5	18x70
2235	S1766	-12750	190.5	18x70
2236	S1767	-12762	85.5	18x70
2237	S1768	-12774	295.5	18x70
2238	S1769	-12786	190.5	18x70
2239	S1770	-12798	85.5	18x70
2240	S1771	-12810	295.5	18x70
2241	S1772	-12822	190.5	18x70

No.	Name	X	Y	Bump size
2242	S1773	-12834	85.5	18x70
2243	S1774	-12846	295.5	18x70
2244	S1775	-12858	190.5	18x70
2245	S1776	-12870	85.5	18x70
2246	S1777	-12882	295.5	18x70
2247	S1778	-12894	190.5	18x70
2248	S1779	-12906	85.5	18x70
2249	S1780	-12918	295.5	18x70
2250	S1781	-12930	190.5	18x70
2251	S1782	-12942	85.5	18x70
2252	S1783	-12954	295.5	18x70
2253	S1784	-12966	190.5	18x70
2254	S1785	-12978	85.5	18x70
2255	S1786	-12990	295.5	18x70
2256	S1787	-13002	190.5	18x70
2257	S1788	-13014	85.5	18x70
2258	S1789	-13026	295.5	18x70
2259	S1790	-13038	190.5	18x70
2260	S1791	-13050	85.5	18x70
2261	S1792	-13062	295.5	18x70
2262	S1793	-13074	190.5	18x70
2263	S1794	-13086	85.5	18x70
2264	S1795	-13098	295.5	18x70
2265	S1796	-13110	190.5	18x70
2266	S1797	-13122	85.5	18x70
2267	S1798	-13134	295.5	18x70
2268	S1799	-13146	190.5	18x70
2269	S1800	-13158	85.5	18x70
2270	S1801	-13170	295.5	18x70
2271	S1802	-13182	190.5	18x70
2272	SHIELDING	-13194	85.5	18x70
2273	COM5	-13206	295.5	18x70
2274	SHIELDING	-13218	190.5	18x70
2275	SHIELDING	-13230	85.5	18x70
2276	COM5	-13242	295.5	18x70
2277	SHIELDING	-13254	190.5	18x70
2278	RP2I	-13314	310.5	40x40
2279	RP2I	-13394	310.5	40x40
2280	COMR1	-13474	310.5	40x40
2281	COMR1	-13554	310.5	40x40
2282	COMR2	-13634	310.5	40x40
2283	COMR2	-13714	310.5	40x40
2284	SHIELDING	-13794	310.5	40x40
2285	SHIELDING	-13874	310.5	40x40
2286	SHIELDING	-13954	310.5	40x40
2287	SYNC_R1	-14093	320.5	120x20
2288	SYNC_R2	-14093	282.5	120x20
2289	SYNC_R3	-14093	244.5	120x20
2290	SYNC_R4	-14093	206.5	120x20
2291	SYNC_R5	-14093	168.5	120x20
2292	SYNC_R6	-14093	130.5	120x20
2293	SYNC_R7	-14093	92.5	120x20
2294	SYNC_R8	-14093	54.5	120x20
2295	SYNC_R9	-14093	16.5	120x20
2296	SYNC_R10	-14093	-21.5	120x20
2297	SYNC_R11	-14093	-59.5	120x20
2298	SYNC_R12	-14093	-97.5	120x20

Name	X	Y	Bump size
Alignment_Mark	-14095.5	-273	115x115
Alignment_Mark	14095.5	-273	115x115

15. Ordering Information

Part No.	Package Type
HX8279-D01XPDxxx	X : mean fab code PD : mean COG xxx : mean chip thickness **(μm)**