DATA SHEET

FT8206

Super In-Cell IC Integrates TFT LCD Driver and Touch Panel Controller Into a Single Chip. Cascade Function for Amorphous TFT-LCDs and Touch Controller Support Real Multi-Touch Capability.

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Preliminary

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1. GENERAL DESCRIPTION

FT8206 highly integrates TFT LCD driver and Super in-cell Touch controller. Combined with Super in-cell panel technology, FT8206 provides high performance and high-quality human-machine interactive solutions for tablet display terminals.

FT8206 also support cascade function to achieve higher resolution and smaller sensing pitch, the LCD driver in FT8206 supports 2-chip cascade function maximum resolutions WQXGA (MUX 1:1 1600RGBx2560 ; MUX 1:2 2560RGBx1600) resolution, provides the number of colors up to 16.7M. In addition, FT8206 uses RGB colors each with independently adjustable Gamma correction, 1-dot / 2-dot / 1+2-dot / 1-Column / 2-Column / Zigzag liquid crystal reversion mode and CABC / CE image processing technology, so that it can achieve high resolution, multi-color, high-quality display characteristics.

The touch panel controller of FT8206 uses a 32-bit high-performance single-cycle instruction-set MCU. With its built-in high-speed high-performance hardware-accelerated computing modules, it provides superior data processing capabilities. FT8206 AFE can support up to 1280 channels for touch sensing. Combined with Time-Division and Area-Division scanning technology, it greatly reduces the scanning time of touch panel, so that the maximum of point reporting rate could up to 144Hz. With Focaltech's patented drive technology and algorithms, the touch controller has excellent waterproof performance, strong anti-noise-and-interference ability and high signal to noise ratio. Its touch experience can achieve up to 10 points. FT8206 AFE can support stylus sensing and communication.

In addition, the external Flash of FT8206 can store not only the firmware used for Touch controller, but also the Initial code of LCD driver. After loading the initial code through the external Flash, the HOST only needs to send out "Sleep out" and "Display on" to turn on the LCD. This will greatly simplify the operation of the HOST to LCD, making the configuration process both flexible and simple. Furthermore, when ESD occurs, HOST reloads Initial code directly from Flash, greatly improving the IC's ESD capability.

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2. FEATURES

2.1. Touch Function feature list

- **32-bit embedded single-cycle instruction-set MCU**
  - Built-in hardware acceleration module
  - Program storage size: 128K Byte SRAM
  - Data storage size: 128K Byte SRAM
- **Super self-capacitance detection technology**
- **Supports up to 1280 SX channels**
- **Supports up to 10pF capacitive sensing per channel**
- **10-point Real Touch**
- **Anti-floating**
- **Anti-power interference**
- **Anti-stress from external**
- **Anti-RF interference**
- **Point reporting rate up to 120Hz**
- **I2C data communication interface**
- **SPI data communication interface**
- **Support THP(Touch Host Processing)**
- **Supports stylus**

Note : A crystal will be added refer to the pen's protocol.

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2.2. Display Function feature list

- **Support HD+ a-Si TFT LCD Driver without GRAM**
- **Support Flash initialization with initial code inside**
- **Support 144Hz/120Hz/90Hz/60Hz/30Hz/15Hz frame rate & VESA DSC 3X decode**
- **Support Resolution :**
  - 2-chip with cascade : 2560RGB x (1600, others) ; 2000RGB x (3000, others) ; 1880RGB x (2880, others) ; 1600RGB x (2560, others) ; 1536RGB x (2048, others) ; 1440RGB x(2560, others) ; 1280RGB x (2048, others) ; 1200RGB x (1920, others)
  - 1 chip : 1280RGB x (2560, others) ; 1200RGB x (1920, others) ; 800RGB x (1280, others) ; 720RGB x (1280, others) ; 600RGB x (1024, others) ; 540RGB x (960, others)

  *Note: Please contact our sales for further help if your resolution is not listed here.
- **Color Display**
  - Full color mode : 16.7M (24-bit, 8(R):8(G):8(B))
- **Support the features that refresh the display function for N-lines with an adjusted pause of 0 ~ 400us (for touch scan) and then continue to refresh the display function for N lines**
- **Display features**
  - Supports independently adjustable RGB gamma correction
  - Support 1-dot / 2-dot and 1-Column / 2-Column / Zigzag LCD reversion modes
  - Support OverDrive / Slew Rate control on Source driver
- **Built-in Focal CleverColor Image processing functions**
  - CleverColor – Color Enhancement$_{opt1.0}$
  - CleverColor – CABC$_{opt1.0}$
  - CleverColor – AIE$_{opt1.0}$
  - CleverColor – Digital Gamma$_{opt1.0}$
  - CleverColor – Contrast$_{opt1.0}$
  - CleverColor – WA$_{opt1.0}$
  - CleverColor – Sharpness Enhancement$_{opt1.0}$ (Not Support in Cascade Mode)
- **Interface**
  - MIPI Interface (DSI V1.0, DCS V1.3 and DPHY V1.1 with 2/3/4 Lane) , Max Speed 1.3Gbps
  - MIPI Interface (DSI V1.0, DCS V1.3 and CPHY V1.1 with 1/2/3 trio), Max Speed 1.2Gsps
- **On Chip function**
  - Built-in VCOM Generator
  - Provide OTP to store VCOM/ID1/ID2/ID3
  - Save command setting in external flash memory
  - Built-in Oscillator for display clock generation
  - On module checksum checking
  - Built-in 24 GOUT signals (GOUT1 ~ GOUT24) on each side of the chip, providing the drive signals to the GIP circuit on the LCD panel

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- Temperature Compensation for VGHO/VGLO/VCOM

- **Output voltage levels**
  - Source output voltage level: (GVDDP~+0.1V) and (-0.1V~GVDDN)
  - Gamma voltage range: GVDDP: 3.75V ~ 6.3V, GVDDN: -3.75V~-6.3V
  - Positive gate driver output voltage range VGH: X2(2*AVDD), X3(2*AVDD-AVEE), X4(2*AVDD-2*AVEE)
  - Negative gate driver output voltage range VGL: X2(2*AVEE), X3(2*AVEE-AVDD)
  - Common electrode output voltage level VCOM: -0.3V ~ -3.85V
- **Supply Voltage Range**
  - I/O and logical circuit power: 1.65V ~ 1.95V
  - Positive Analog supply voltage range: 4.5V ~ 6.5V
  - Negative Analog supply voltage range: -4.5V ~ -6.5V
- **Support OTP Multiple Program Times**
  - ID for 5 times programmable
  - GVDD for 2 times programmable
  - Gamma for 2 times programmable
  - VCOM for 8 times programmable
  - User Info for 5 times programmable
  - Please refer to the application note to get detailed information about multiple program times.
- **Support Power Mode:**
  - 3 Power Mode: VDDI / VSP / VSN
  - 4 power Mode: VDDI / VSP / VSN / VDD
  - 5 power Mode: VDDI / VSP / VSN / VGH / VGL
  - 6 power Mode: VDDI / VSP / VSN / VGH / VGL / VDD

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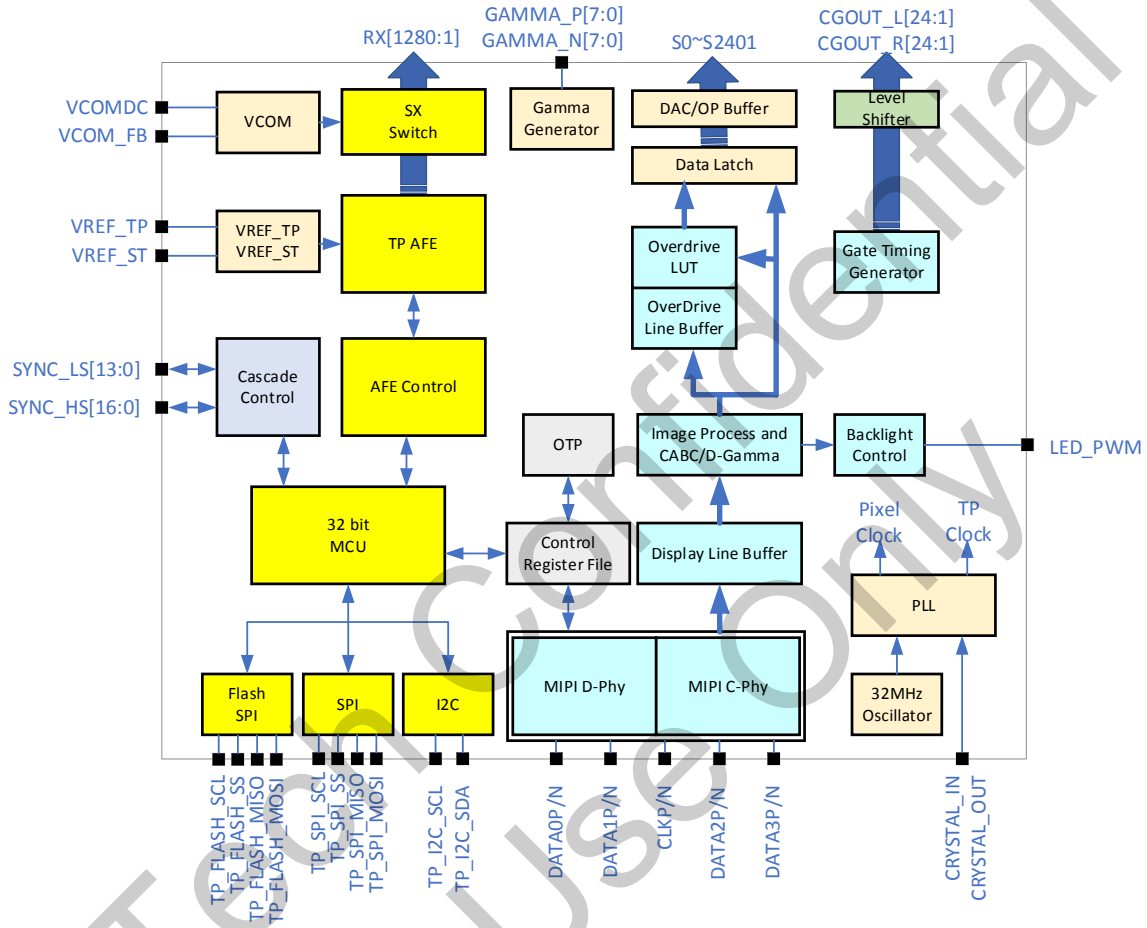
3. BLOCK DIAGRAM

3.1. Block Function



3.1.1. System interface

FT8206 supports the video data transmitted through the high-speed system interface, MIPI (Mobile Industry Processor) interface, and I2C/SPI interface for the touch point-reporting function.

In normal operating mode, touch controller scans the screen, and detects the touch and stylus actions. The default setting of point-reporting rate is set as 60Hz/120Hz and can be adjusted up or down. The default setting of stylus point-reporting rate is set as 240Hz and can be adjusted up or down if permitted by the pen protocol.

In touch detection mode, touch controller enters low-power mode, detects and scans touch-screen body. Detection scanning frequency is 30Hz, can also be adjusted up or down. During touch detection mode, majority of the algorithm will be terminated, and only a simple detection algorithm is retained to detect if there is a touch action happened. Whenever a touch is detected, touch controller will immediately enter the normal operating mode.

In sleep mode, touch controller enters ultra low-power standby mode, HOST can only wake-up touch controller via "RESET" or "WAKEUP" signal to enter the normal operating mode. The power consumption in this mode is extremely small, can greatly extend the standby time of mobile portable devices.

3.1.2. AFE Controller

AFE controller completes the driving and scanning functions of the sensors in the touch panel, and sends the data from touch sensors after scanning to the MCU for data processing.

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3.1.3. Embedded MCU

MCU and SOC subsystems complete the control, data processing, LCD operation and coordination, HOST communication and other functions of the whole touch systems. Firmware, stored in external flash memory, can be loaded into the internal SRAM by HOST via the I2C or SPI interface. Firmware can also be download from HOST through SPI interface without external FLASH required.

3.1.4. I2C/SPI Serial Interface

FT8206 can support I2C or SPI for touch communication with HOST. The control interface is consisted of two signals, INT and TP_EXT_RSTN. Whenever there is an effective touch sensed on the touch screen, touch controller will send data transfer request to the HOST via INT port, and complete the point report to the HOST. HOST can communicate with FT8206 via I2C. HOST can also reset Touch controller through TP_EXT_RSTN port.

3.1.5. External Flash

External Flash, used to store the Firmware, internal voltage regulator generates 1.8V power supply, which is to provide power to an external 1.8V Flash. In non-Flash application, Firmware could be downloaded from HOST through SPI interface.

3.1.6. Watch Dog

Watchdog clock is used to ensure the stability of the chip when in operation

3.1.7. Timing controller

The timing controller generates timing signals for the operations of internal circuits such as gate/source/vcom/ touch scan output timing.

3.1.8. Source driver circuit

The source driver circuit is consisted of 2400-channels source driver (S1 ~ S2400). The RGB Data from MIPI interface are latched when a single line data has been accumulated. The latched data generates the liquid crystal drive voltage from the source based on the grayscale settings in gamma correction function.

3.1.9. Gate driver circuit

The gate driver circuit outputs gate driver signals at either VGHO or VGLO level while LCD driving.

3.1.10. SX driver circuit

Supply VCOM level when LCD driving. Generates TP sensing pulse when TP driving.

3.1.11. Oscillator (OSC)

FT8206 also features an internal oscillator to generate RC oscillation with an internal resistor.

3.1.12. Grayscale voltage generating circuit

FT8206 has true 8-bit resolution D/A converter, which generates 256 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register and RGB can be adjusted separately.

3.1.13. LCD driving power supply circuit

The LCD driving power supply circuit generates the voltage levels AVDD, AVEE, VGH, VGL and VCOM for driving an LCD. All these voltages can be adjusted by register setting.

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4. PIN DESCRIPTIONS

4.1. Pin Definition

Pad Symbol	I/O	Pad Type	Function
Power Supply			
AVDD AVDD_DC	P	Analog Power	+4.5V ~ +6.5V external analog power supply
TAVDD_L/TAVDD_R	P	Analog Power	+4.5V ~ +6.5V external analog power for Touch Analog circuit
AVEE AVEE_DC	P	Analog Power	-4.5V ~ -6.5V external analog power supply
AVSS AVSS_DC LVDSVSS	P	Analog Ground	0V. Ground for analog units.
TAVSS_L/TAVSS_R	P	Analog Ground	0V. Ground for touch analog circuits.
VSS	P	Digital Ground	0V. Ground for digital circuits.
VSS_TP_OSC	P	Analog Ground	0V. Ground for Oscillator.
VDDI	P	IO Power	+1.65V ~ +3.6V. Power supply for peripheral.
DC-DC Converter related pads			
VGH_L / VGH_R	O	Internal Power	Positive charge pump output. Connect together with FPC.
VGHB	O	Internal Power	Require a capacitor between VGH_L/VGH_R and VGHB.
VGL	O	Internal Power	Negative charge pump power output. Connect a capacitor for stabilization.
C21P / C21 N	IO	Analog output	Flying capacitor connection pins for VGH. Require a capacitor between C21P and C21N.
C22P / C22N	IO	Analog output	Flying capacitor connection pins for VGH. Require a capacitor between C22P and C22N.
C31P / C31N	IO	Analog output	Flying capacitor connection pins for VGL. Require a capacitor between C31P and C31N.
Regulator Pads			
VGHO_L VGHO_R	O	Internal Power	Positive HV regulator output of GOA FPC connects VGHO_L and VGHO_R together.
VGH1_R VGH2_L	I	Power Input	Input power for GOA circuits. This pin is used for discharge function. Short to VGHO if not used.
VGHOB	O	Internal Power	Connect a capacitor between VGHO and VGHOB
VGLO_L VGLO_R	O	Internal Power	Negative HV regulator output of GOA FPC connects VGLO_L and VGLO_R together.
VGLOB	O	Internal Power	Connect a capacitor between VGLO and VGLOB.
VCL	O	Internal Power	Regulator output voltage. Connect a capacitor for stabilization.
VDD	O	Internal Power	Regulator output for internal logic circuit power. This power will drop to VSS in deep standby mode. Connect a capacitor for stabilization.
LVDSVDD	O	Internal Power	Regulator output for MIPI interface circuit power. Connect a capacitor for stabilization.
VDD_TP VDD_TP_OSC	O	Internal Power	Regulator output for touch logic/oscillator circuit power. Connect a capacitor for stabilization.

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VREF_TP_L VREF_TP_R	O	Internal Power	Regulator output for TP reference voltage. Connect a capacitor for stabilization.
VREF_ST_L VREF_ST_R	O	Internal Power	Regulator output for TP reference voltage. Connect a capacitor for stabilization.
VCOM_L / VCOM_R VCOMDC / VCOM	O	Internal Power	Regulator output for VCOM. Connect a capacitor in middle of FPC.
VCOM_FB	I	Internal Power	Feedback path for VCOM circuit
GVDDP	O	AVDD	Regulator output for positive gamma. Needs an external capacitor for voltage stabilization.
GVDDN	O	AVEE	Regulator output for negative gamma. Needs an external capacitor for voltage stabilization.
DCHG1	O	VGH	For gate signal power-off slope control(group1). Need connect to a resistor when used, otherwise tie to VSS.
DCHG2	O	VGH	For gate signal power-off slope control(group 2). Need connect to a resistor when used, otherwise tie to VSS.
Interface : MIPI I2C SPI			
CLKP/CLKN	I	LVDSVDD	MIPI DSI clock differential input, tie to LVDSVSS if not used.
DATAP[0]/DATAN[0]	IO	LVDSVDD	MIPI DSI data differential pair 0, tie to LVDSVSS if not used.
DATAP[1]/DATAN[1]	IO	LVDSVDD	MIPI DSI data differential pair 1, tie to LVDSVSS if not used.
DATAP[2]/DATAN[2]	IO	LVDSVDD	MIPI DSI data differential pair 2, tie to LVDSVSS if not used.
DATAP[3]/DATAN[3]	IO	LVDSVDD	MIPI DSI data differential pair 3, tie to LVDSVSS if not used.
TP_FLASH_HOLD	IO	VDDI	Flash SPI interface hold pin. Keep float if not used.
TP_FLASH_SCL	IO	VDDI	Flash SPI interface clock pin. Keep float if not used.
TP_FLASH_MISO	IO	VDDI	Flash SPI interface data input pin. Keep float if not used.
TP_FLASH_MOSI	IO	VDDI	Flash SPI interface data output pin. Keep float if not used.
TP_FLASH_SS	IO	VDDI	Flash SPI interface chip select pin. Keep float if not used.
TP_FLASH_WP	IO	VDDI	Flash SPI interface write protect pin. Keep float if not used.
TP_SPI_SCL	I	VDDI	Touch SPI interface clock pin. Keep float if not used.
TP_SPI_MISO	O	VDDI	Touch SPI interface data output pin. Keep float if not used.
TP_SPI_MOSI	I	VDDI	Touch SPI interface data input pin. Keep float if not used.
TP_SPI_SS	I	VDDI	Touch SPI interface chip select pin. Keep float if not used.
TP_I2C_SCL	I	VDDI	Touch SPI interface clock input pin. Keep float if not used.
TP_I2C_SDA	IO	VDDI	Touch SPI interface data pin. Keep float if not used.
TP_INT	I/O	VDDI	External interrupt pin for host interrupt. Keep float if not used.
TP_WAKE	I/O	VDDI	External wake up pin, for Host wake up touch function. Keep float if not used.
Logic Setting Control			
RESX	I	VDDI	Global Reset. Low assertive. (Internal pull high)
TP_EXT_RSTN	I	VDDI	Touch circuit external reset. Low assertive. Keep float if not used.
TP_MS	I	VDDI	Master / Slave Select pin. (Internal pull high) 1 : Cascade Master IC or single chip 0 : Cascade Slave IC.
TP_BOOT_DEVICE	I	VDDI	0 : support SPI flash

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			1 : support non-flash
TP_BUS_SEL	I	VDDI	TP report Bus select 1 : SPI as report bus 0 : I2C as report bus
EN_EXT_HV	I	VDDI	Enable external VGH/VGL. (Internal pull low) 1 : VGH/VGL power form external power IC. 0 : VGH/VGL generated by internal charge pump.
EN_EXT_VCOM	I	VDDI	Enable external VCOM. (Internal pull low) 1 : VCOM power form external power IC. 0 : VCOM generated by internal VCOM buffer.
EN_EXT_VDD	I	VDDI	Enable external VDD. (Internal pull low) 1 : VDD/VDD_TP power form external power IC. 0 : VDD/VDD_TP generated by internal regulator.
BIST_EN	I	VDDI	BIST mode enable, high assertive. (Internal pull low) Keep float if not used.
IM	I	VDDI	Select MIPI interface. (Internal pull low) 0 : D-PHY 1 :C-PHY
LANSEL[1:0]	I	VDDI	MIPI Lane Count Select. Please refer to section 6.2. (Internal pull high)
DSWAP[1:0]	I	VDDI	MIPI Data Pin Out Select. Please refer to section 6.2. (Internal pull high)
PNSWAP	I	VDDI	MIPI P/N Polarity Select. Please refer to section 6.2. (Internal pull high)
CRYSTAL_SEL[1:0]	I	VDDI	External Crystal Frequency Select. (Internal pull low) **CRYSTAL_SEL[1:0] / Interface Selection** 00 (Default) / OFF 01 / 8MHz 10 / 12MHz 11 / 16MHz
CRYSTAL_IN CRYSTAL_OUT	IO	VDDI	Connect to external crystal.
LED_PWM	O	VDDI	Backlight LED driver control pin. Keep float if not used.
ENB_CASCADE	I	VDDI	Cascade enable. (Internal pull high) 0 : Dual chip 1 : Single chip.
Gate Control			
CGOUT_R[24:1] CGOUT_L[24:1]	O	VGH / VGL	GOA control output Please left unused pins floating
Source / Sx			
RX[1280 : 1]	IO	AVDD/AVEE	Touch Sensor Pads
S[2401 : 0]	O	AVDD/AVEE	Source output pin. S[0] / S[2401] for zigzag use.
VCOM_OPT_L VCOM_OPT_R	O	AVDD/AVEE	For Panel outline ring use.
Cascade Controls			

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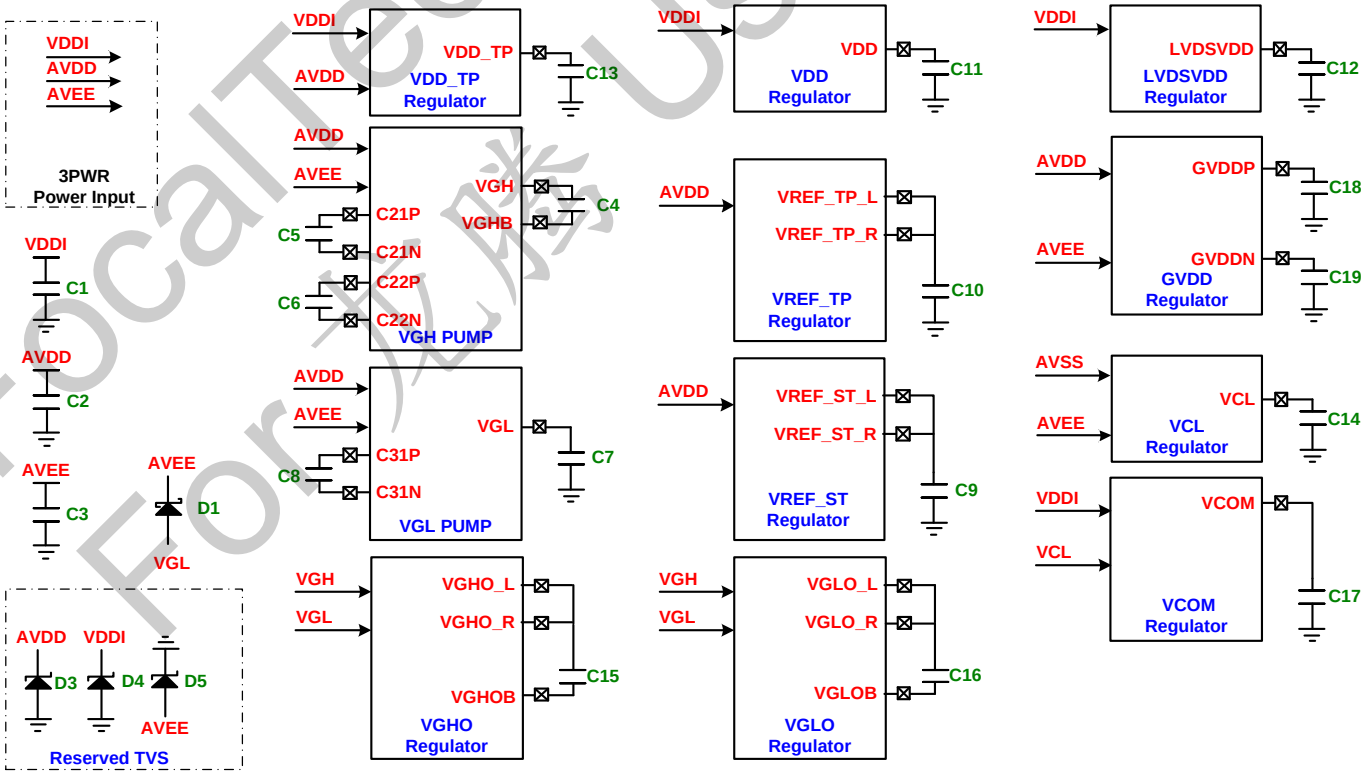
GAMMA_N_L[7:0] GAMMA_N_R[7:0]	IO	AVDD/AVEE	Negative Gamma Sync Pins. Connect master/slave GAMMA_N_L and GAMMA_N_R in cascade mode
GAMMA_P_L[7:0] GAMMA_P_R[7:0]	IO	AVDD/AVEE	Positive Gamma Sync Pins. Connect master/slave GAMMA_P_L and GAMMA_P_R in cascade mode
SYNC_HS[16:0]	IO	VDDI	High Speed Cascade Sync Pins. Reserve these pins on the FPC connection in cascade application and connect master HS_SYNC and slave HS_SYNC.
SYNC_LS_L[13:0]	IO	VDDI	Low Speed Cascade Sync Pins. Reserve these pins on the FPC connection in cascade application and connect master LS_SYNC_L and slave LS_SYNC_L.
Test and Misc. Pins			
AFE_TEST_L/L0/R0/R1	IO	AVDD	TP analog test pins. Leave it floating.
POR12 / POR18	O	VDDI	TP POR pad, leave it floating.
TEST[16:0]	IO	VDDI	Test pins, leave these pins floating. (Internal pull low)
TP_AFE_SCAN_MODE	I	VDDI	Test mode with AFE scan/normal mode selection. Leave this pin floating.
LCD_SCL / LCD_SDA	IO	VDDI	LCD debug interface. Leave these pins floating. (Internal pull high)
LCD_EXT_OSC	I	VDDI	LCD test mode for external clock input. Keep float in normal use. (Internal pull low)
LCD_GPIO[1:0]	IO	VDDI	Test Pins for LCD. Keep float in normal use. (Internal pull low)
TP_GPIO[1:0]	IO	VDDI	Test Pins for Touch. Keep float in normal use.

4.2. Power Block Diagram



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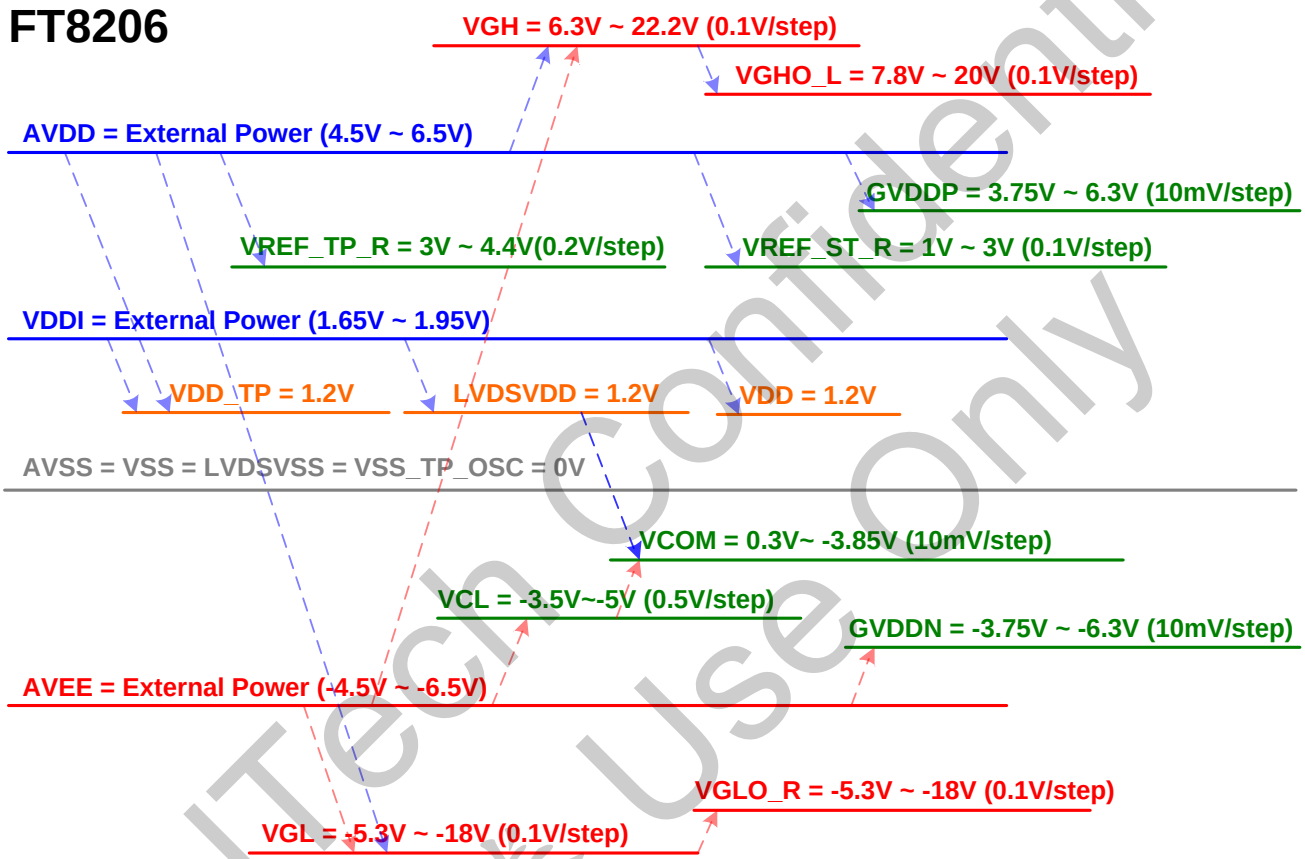
4.3. Power Supply Configuration



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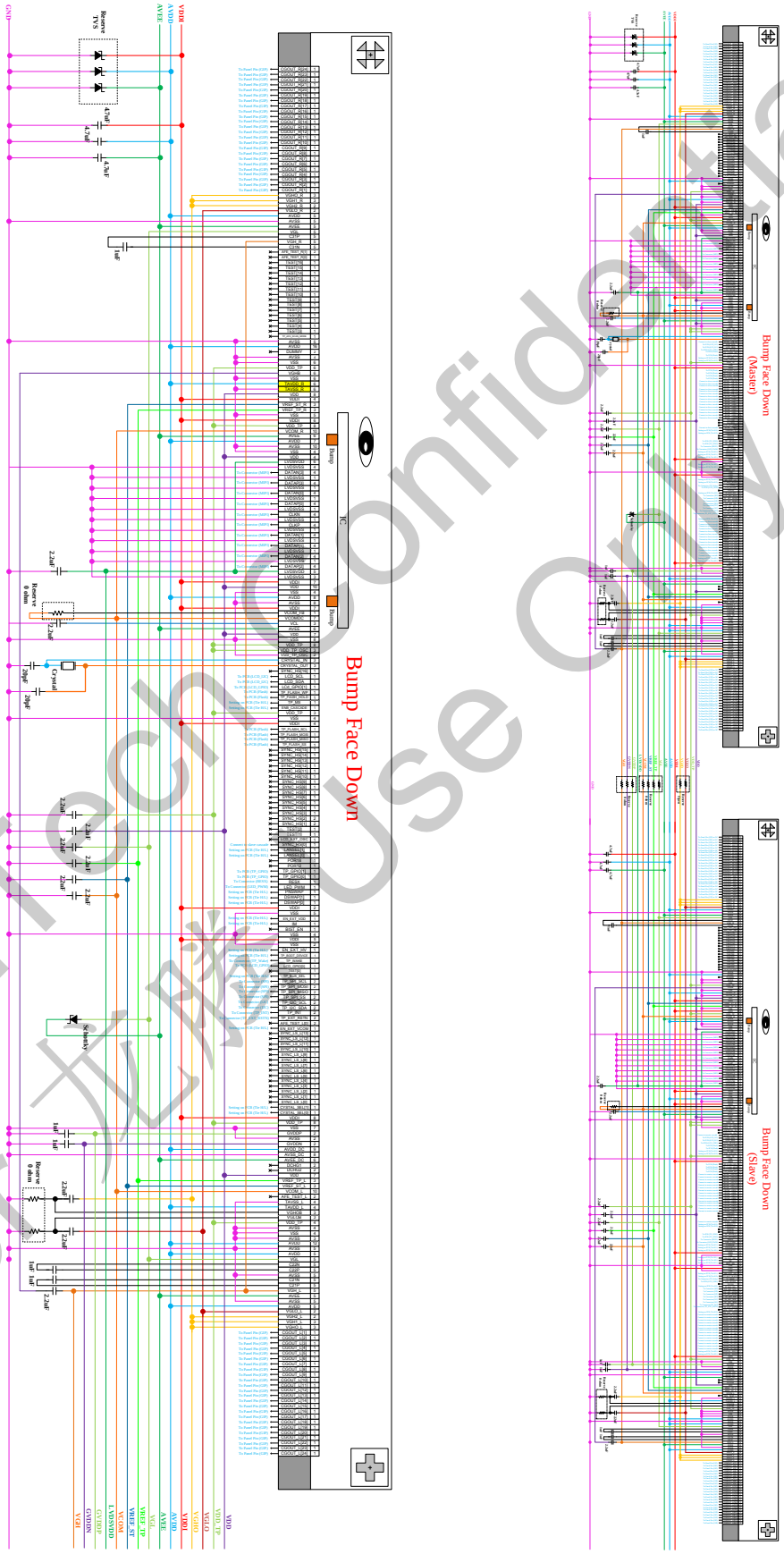
4.4. Application Circuit



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5. INSTRUCTION

5.1. Outline

The FT8206 supports high speed serial interface, MIPI, to configure system via accessing command register. When the command register is executed, sending the command information to specify which index register would be accessed and following the data to that control register. The MIPI-DSI is compliant with MIPI Alliance Standard for Display Serial Interface (DSI), Version 1.2, D-PHY Version 1.1, Display Command Set (DCS), Version 1.2.

The FT8206 has the following major categories of instructions:

(1). System function instructions (User Command Set).

(2). Customer Command List and Description (Manufacturer Command Set / Command 2).

These instructions are asynchronous to the FT8206 internal clock, requiring no wait cycles. Because the writing of instruction data does not interfere with the host controller processing, instructions can be handles smoothly and efficiently. The following describes details of instruction settings.

5.1.1. System function command list and description

After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer “RESET TABLE” section). Commands 28h and 29h are updated during V-Blanking to avoid abnormal visual effects. By the way, all commands in master and slave side can be updated concurrently during V-Blanking via MIPI DSI v1.2 FSC function.

System function command access flow is described as following example.

Example 1: Sleep Out

Address 0x11

Example 2: Display On

Address 0x29

Example 3: Bypass Mode

Address 0x09

DATWR 0x01

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System Function Command List

Command	(Hex)	Write/Read /Command	Function	Parameter Number	MIPI Transmission
SWRESET	01	**W**	Software Reset.	0	LPDT/HSDT
BISTEN	02	**WR**	BIST Mode Enable. 0x5A : Enable ; Others : Disable	1	LPDT/HSDT
DSCEN	03	**R**	Read VESA DSC Status. 0x00: VDSC Disabled; 0x01: VDSC Enabled	1	LPDT/HSDT
DSTB0	04	**WR**	Deep Standby Mode Enable 0. {DSTB0, DSTB1} = 0x5A5A Enter Deep Standby mode ; others no action.	1	LPDT/HSDT
DSTB1	05	**WR**	Deep Standby Mode Enable 1. {DSTB0, DSTB1} = 0x5A5A Enter Deep Standby mode ; others no action.	1	LPDT/HSDT
LONGH_ENB	09	**WR**	Long-H Mode Disable. 1 : Long-V Mode only ; 0 : Long-H Mode	1	LPDT/HSDT
SLPIN	10	**C**	Sleep in	0	LPDT/HSDT
SLPOUT	11	**C**	Sleep out	0	LPDT/HSDT
MA_TERMR_EN	14	**WR**	Master MIPI Termination Resistor Enable. 0xA5 : Disable Master termination. 0x5A : Force Master Termination. Others : Follow MIPI state	1	LPDT/HSDT
SL_TERMR_EN	15	**WR**	Master MIPI Termination Resistor Enable. 0xA5 : Disable Master termination. 0x5A : Force Master Termination. Others : Follow MIPI state	1	LPDT/HSDT
DISPOFF	28	**C**	Display off	0	LPDT/HSDT
DISPON	29	**C**	Display on	0	LPDT/HSDT
OTP_STOP_RELOAD	41 4E	**WR**	Both [41]/[4E] not equal to 0x5A, OTP perform self-reload periodically. [41] = 0x5A or [4E] = 0x5A, data bus is controlled by external interface and stop OTP reload.	1	LPDT/HSDT
EXT_ADR	42	**WR**	Extended address of I2C and MIPI. SysAddr = {EXT_ADR[6:0] + OFFSET[6:0]}	1	LPDT/HSDT
CMD_REPLY_EN	43	**WR**	0xC3 : Only Slave reply I2C/MIPI readout request Others : Only master reply I2C/MIPI readout request	1	LPDT/HSDT
OTP_CTRL_STS	48	**WR**	OTP Control and status.	1	LPDT/HSDT
DISBV_SET	51h	**W**	Display Brightness Value Setting	1	LPDT/HSDT
DISBV_RD	52h	**W/R**	Read Display Brightness Value	1	LPDT/HSDT
DISBV_CTRL	53h	**W/R**	Display Brightness Value Control	1	LPDT/HSDT
RDDISBV_CTRL	54h	**R**	Read Display Brightness Value Control	1	LPDT/HSDT
WRFCC_CABC	55h	**W**	Write Content Adaptive Brightness Control	1	LPDT/HSDT
RDFCC_CABC	56h	**R**	Read Content Adaptive Brightness Control	1	LPDT/HSDT
OTP_PROG	58h	**W/R**	OTP Program	1	LPDT/HSDT

Note: LPDT (Low Power Mode), HSDT (High Speed Mode)

Note: At MIPI direct mode, no matter MASTER IC or SLAVE IC , cmd need writing by each MIPI bus. Master can't pass cmd to Slave.

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5.2. System Function Command Description

5.2.1. SWRESET (01h): Software Reset

Bank -									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
01H (SWRST)	No Parameter								-

Description
SWRST：Software Reset Address = '01H' - When the Software Reset command is written, it causes a software reset to display circuit only. - It resets the commands and parameters to their reset default values and all source & gate outputs are set to VSS (display off). (See default tables in each command description) Restriction and notes： - It will be necessary to wait 100msec before sending new command following software reset. - The display module loads all display supplier's factory default values to the registers during 100msec. - Software Reset command cannot work during Deep Standby State.

5.2.2. BIST_MODE (02H): Enter BIST mode

Bank -									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
02H	bist_en[7:0]								A5h

Description
bist_en[7:0]： - This command is used to set BIST Mode function '5Ah' = Enter BIST Mode. 'Others' = Exit BIST Mode. Restriction and notes： - Both register software setting and I/O hardware pin can enter BIST Mode function. (Control ORed) - In CASCADE/Direct Mode application, this command should send to Master side that dominates state of both sides.

5.2.3. DSCEN (03H): VESA DSC Enable

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
03H	Reserved							VDSC_EN	00h

Description
VDSC_EN： - This command is used to set BIST Mode function '1' = Enable VESA DSC. '0' = Disable VESA DSC. Restriction and notes： - .

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5.2.4. DEEP_STBY (04H/05H): Enter Deep Standby Mode

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
04H	DEEP_STBY0[7:0]								00h
05H	DEEP_STBY1[7:0]								00h

Description
- These two command are used to set Deep Standby Mode function. - There are 2 methods that can enter Deep Standby State： Method 1 : Set DEEP_STBY0[7:0] = 5Ah and DEEP_STBY1[7:0] = 5Ah in any state. Method 2 : Set DEEP_STBY0[7:0] = A5h and DEEP_STBY1[7:0] = A5h when Sleep In Mode. Restriction and notes： - In CASCADE/Direct Mode application, these commands should send to Master side that dominates state of both sides. - Only Hardware Reset can exit Deep Standby Mode, and it will be necessary to wait 100msec before sending new command following hardware reset. - The display module loads all display supplier's factory default values to the registers during 100msec.

5.2.5. LONGH_MODE (09H): Long-H mode disable

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
09H	Reserved							longH_enb	00h

Description
LONGH_ENB： - This command is used to disable/enable Long-H Mode function. '1' = Long-H Mode disable.. '0' = Long-H Mode enable.(Default) Restriction： - In CASCADE application, this command should send to Master side that dominates state of both sides.

5.2.6. SLPIN (10H) & SLPOUT (11H) : Sleep-In & Sleep-Out

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
10H (SLPIN)	No Parameter								-
11H (SLPOUT)	No Parameter								-

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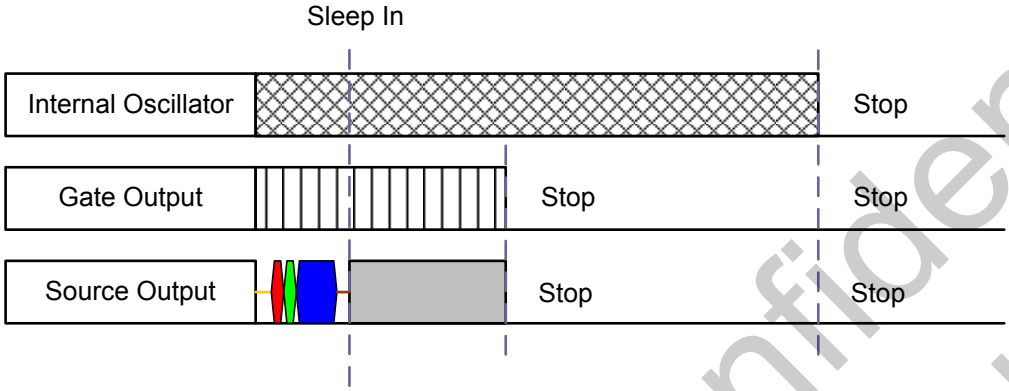
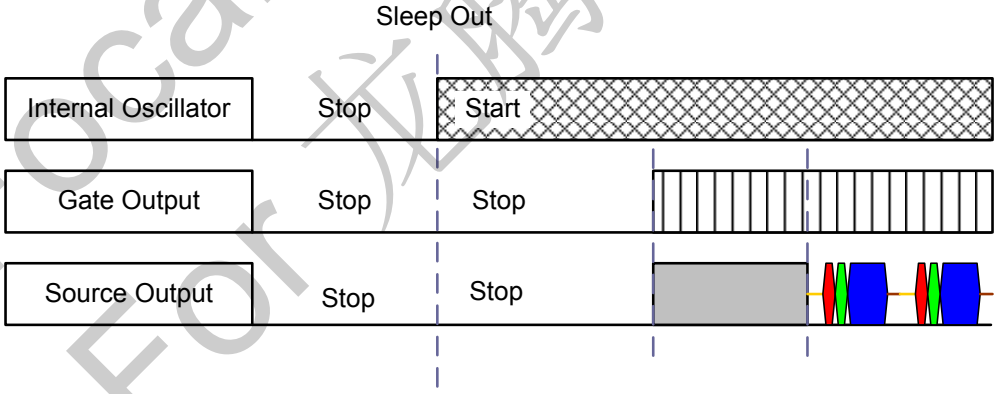
Description

SLPIN：Sleep-In (Enter Standby Mode)
Address = '10H'
- This command causes the LCD module to enter the power consumption reduced mode.
- In this mode, internal display oscillator is stopped, and panel scanning is stopped.
- Only the command path are still working to support the exit from Standby Mode.



Restriction：
- This command has no effect when module is already in sleep in mode. Standby Mode can only be exit by the SLPOUT Command (11H).

SLPOUT：Sleep-Out (Exit Standby Mode)
Address = '11H'
- This command causes the LCD module to exit the power consumption reduced mode.
- In this mode, internal display oscillator is started, and panel scanning is started.



Restriction：
- This command has no effect when module is already in sleep out mode.
- Sleep Out Mode can only be exit by the SLPIN Command (10H).

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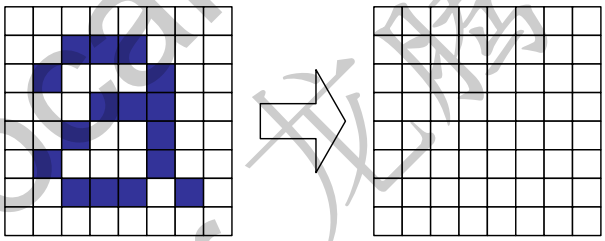
5.2.7. TERMR_EN (14H~15H): MIPI TermR Enable

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
14H	MA_TERMR_EN								FFh
15H	SL_TERMR_EN								FFh

Description
MA_TERMR_EN：Master Side MIPI TermR Enable - This command is used to set Master side MIPI TermR enable, disable or normal operation. '5Ah' = Force to enable MIPI TermR 'A5h' = Force to disable MIPI TermR 'Others' = Normal operation that depends on MIPI High Speed Mode SL_TERMR_EN：Slave Side MIPI TermR Enable - This command is used to set Slave2 side MIPI TermR enable, disable or normal operation. '5Ah' = Force to enable MIPI TermR 'A5h' = Force to disable MIPI TermR 'Others' = Normal operation that depends on MIPI High Speed Mode

5.2.8. DISPLAY_CTRL (28H~29H) : Display Control

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
28H (DISPOFF)	No Parameter								-
29H (DISPON)	No Parameter								-

Description
DISPOFF：Display Off Address = '28H' - This command is used to enter into DISPLAY OFF mode. In this mode, the output from the Memory is disables and blank page is inserted. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29H) (Example) Memory Display    Restriction： -This command has no effect when module is already in Display Off mode. DISPON：Display On Address = '29H' - This command is used to recover from DISPLAY OFF mode. Output from the Memory is enabled. - This command does not change any other status.

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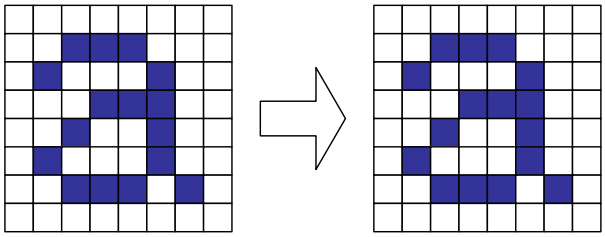
(Example)

Memory

Display



Restriction：
- This command has no effect when module is already in Display On mode.

5.2.9. OTP_STOP_RELOAD (41H/4EH): OTP Stop Reload Enable

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
41H	OTP_STOP_RELOAD[7:0]								00h
4EH	OTP_STOP_RELOAD[7:0]								00h

Description
OTP_STOP_RELOAD：OTP Stop Reload Enable - This command is used to enable OTP stop reload function 'REG41=5Ah or REG4E=5Ah' : Stop OTP reload and switch bus to external interface. 'Others' : Enable OTP reload and switch bus to reload controller.

5.2.10. EXT_ADR (42H): Extended Address of Command Interface

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
42H		Bank_Sel[6:0]							2Fh

Description
Bank_Sel[6:0]：Bank Selection of following command groups for I2C, MIPI and SYSTEM interface. - This command is used to set extended address of I2C, MIPI and SYSTEM interface.

5.2.11. CMD_REPLY_EN (43H): Command Reply Enable

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
43H	CMD_REPLY_EN[7:0]								00h

Description
CMD_REPLY_EN：Command Reply Enable - This command is used to set which side will reply command read data. 'C3h' = Slave side replies read data. 'Others' = Master side replies read data.

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5.2.12. OTP_CTRL_STATUS (48H): OTP Control & Status

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
48H	Reserved	OTP_LOAD_FINISH	OTP_RELOAD_FINISH	SPI_LOAD_FINISH	Reserved	OTP_OP_MODE[2:0]			00h

Description
OTP_LOAD_FINISH (Read-Only)：OTP Initial Load Finish Flag '1' = OTP initial load finish OTP_RELOAD_FINISH (Read-Only)：OTP Reload Finish Flag '1' = OTP reload finish SPI_LOAD_FINISH (Read-Only)：SPI Flash Load Finish Flag '1' = SPI flash load finish OTP_OP_MODE：OTP Operation Mode '000' = Normal Mode '001' = Program Entry '001' = Initial Margin Read '100' = Program Margin Read

5.2.13. DISBV_SET (51H/52H): Display Brightness Value Setting

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
51H	DBV[11:4]								FFh
52H	Reserved				DBV[3:0]				FFh

Description
- This command is used to adjust the brightness value of the display. - It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. - In principle relationship is that 000h value means the lowest brightness and FFFh value means the highest brightness.

5.2.14. DISBV_RD (52H/53H): Read Display Brightness Value

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
52H	DBV[11:4]								FFh
53H	Reserved				DBV[3:0]				FFh

Description
- This command returns the brightness value of the display. - This command can be used to read the brightness value of the display also when Display brightness control is in automatic mode. - It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. - In principle the relationship is that 000h value means the lowest brightness and FFFh value means the highest brightness. - DBV[11:0] is reset when display is in sleep-in mode. - DBV[11:0] is '0' when bit BCTRL of "Display Brightness Value Control (53H)" command is '0'. - DBV[11:0] is manual set brightness specified with "Display Brightness Value Control (53H)" command when bit BCTRL is '1'. - See command "Display Brightness Value Setting (51H)".

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5.2.15. DISBV_CTRL (53H): Display Brightness Value Control

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
53H	Reserved		BCTRL	Reserved	DD	BL	Reserved		00h

Description
- This command is used to control ambient light, brightness and gamma settings. BCTRL：Brightness Control Block On/Off. This bit is always used to switch brightness for display and keyboard. ‘0’ = Off (Brightness registers are 00h) ‘1’ = On (Brightness registers are active, according to the other parameters.) DD：Display Dimming - Dimming function is adapted to the brightness registers for display and keyboard when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. ‘0’ = Display Dimming is off ‘1’ = Display Dimming is on BL：Backlight On/Off - When BL bit change from “On” to “Off”, backlight is turned off ‘0’ = Off (Completely turn off backlight circuit. Control lines must be low.) ‘1’ = On

5.2.16. RDDISBV_CTRL (54H): Read Display Brightness Value Control

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
54H	Reserved		BCTRL	Reserved	DD	BL	Reserved		00h

Description
- This command returns ambient light and brightness control values, see command “Display Brightness Value Control (53H) ” . BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display. ‘0’ = Off ‘1’ = On ... DD: Display Dimming ‘0’ = Display Dimming is off ‘1’ = Display Dimming is on ... BL: Backlight On/Off, This bit is always controlled by the user ‘0’ = Off (completely turn off backlight circuit) ‘1’ = On

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5.2.17. WRFCC_CABC (55H): Write Focal CleverColor – Content Adaptive Brightness Control

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
55H	Reserved						CABC_MODE[1:0]		00h

Description

- This command is used to set parameters for power functionality.
- There is possible to use 3 different modes for content adaptive image functionality, which are defined on a table below.

CABC_MODE	Function	Note
0h	Power Save Off	CABC Off
1h	Power Save Low	User Interface Image(UI)
2h	Power Save Medium	Still Picture(ST)
3h	Power Save High	Moving Image(MV)

CABC = Content Adaptive Brightness Control

5.2.18. RDFCC_CABC (56H): Read Focal CleverColor – Content Adaptive Brightness Control

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
56H	Reserved						CABC_MODE[1:0]		00h

Description

- This command returns for power functionality see command “Write Focal CleverColor – Content Adaptive Brightness Control (55H) ” .

5.2.19. OTP_PROG (58H/5AH/64H/65H/66H/67H) : OTP Program

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
58H	OTP_PROG_UNLOCK[7:0]								00h
5AH	OTP_PROG_START[7:0]								00h
64H	OTP_PROG_BANK[7:0]								00h
65H	OTP_PROG_BANK[15:8]								00h
66H	OTP_PROG_BANK[23:16]								00h
67H	OTP_PROG_BANK[31:24]								00h

Description

OTP_PROG_UNLOCK：OTP Programming Function Unlock
- This command is used to set OTP programming function unlock.
‘96h’ = Unlock OTP programming function.
‘Others’ = Lock OTP programming function.

OTP_PROG_START：OTP Bank Programming Start
- This command is used to set OTP bank programming start.
- When OTP bank programming is done, register value will be set to EDh.
‘AAh’ = Start OTP bank programming.
‘Others’ = Not programming.

OTP_PROG_BANK：OTP Programming Bank Set
- This command is used to set OTP programming bank from Register/SRAM into OTP.

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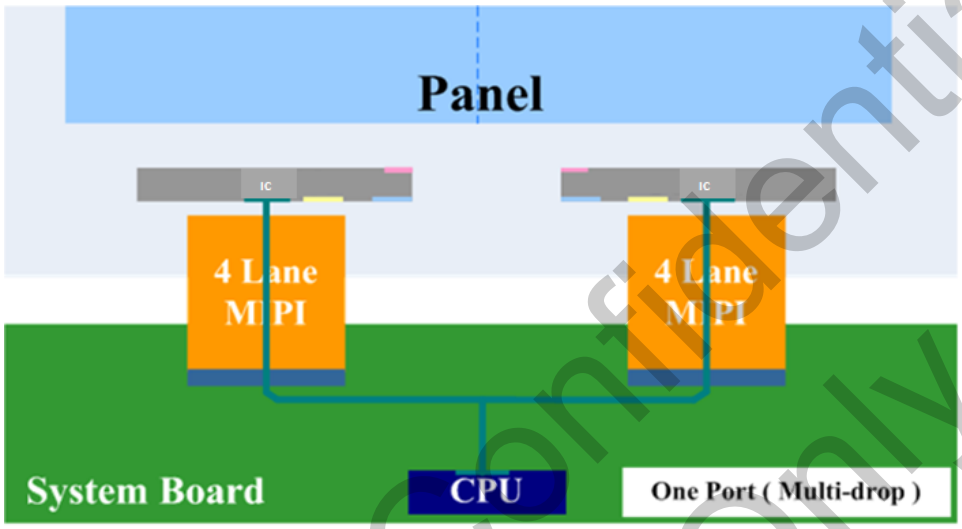
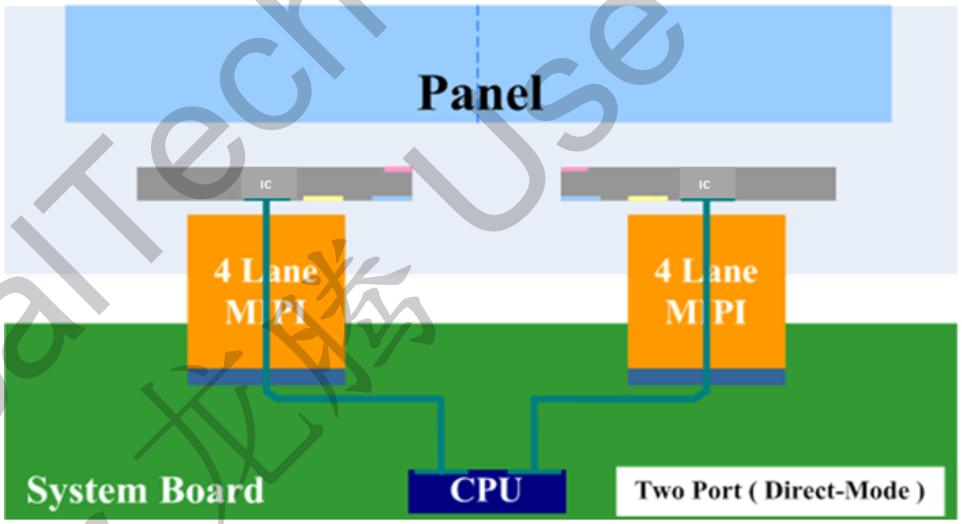
6. FUNCTIONS

6.1. Interface Architecture

FT8206 can support both multi-drop and direct mode architecture for MIPI interface for 2-chip configuration.





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6.2. Interface Type Selection

The MIPI interfaces of FT8206 support D-PHY MIPI 4-Lanes or C-PHY MIPI 3-trios.

LANESEL1	LANESEL0	Interface format
0	1	D-PHY MIPI-2 Lane C-PHY MIPI-1 trio
1	0	D-PHY MIPI-3 Lane C-PHY MIPI21 trio
1	1	D-PHY MIPI-4 Lane C-PHY MIPI-3 trio

TYPE	PSWAP	DSWAP		Physical IC PIN (FT8206)									
		[1:0]		DATAP[2]	DATAN[2]	DATAP[1]	DATAN[1]	CLKP	CLKN	DATAP[0]	DATAN[0]	DATAP[3]	DATAN[3]
DPHY	0	0	0	D3_N	D3_P	D2_N	D2_P	CLK_N	CLK_P	D1_N	D1_P	D0_N	D0_P
	0	0	1	D3_N	D3_P	D0_N	D0_P	CLK_N	CLK_P	D1_N	D1_P	D2_N	D2_P
	0	1	0	D0_N	D0_P	D1_N	D1_P	CLK_N	CLK_P	D2_N	D2_P	D3_N	D3_P
	0	1	1	D2_N	D2_P	D1_N	D1_P	CLK_N	CLK_P	D0_N	D0_P	D3_N	D3_P
	1	0	0	D3_P	D3_N	D2_P	D2_N	CLK_P	CLK_N	D1_P	D1_N	D0_P	D0_N
	1	0	1	D3_P	D3_N	D0_P	D0_N	CLK_P	CLK_N	D1_P	D1_N	D2_P	D2_N
	1	1	0	D0_P	D0_N	D1_P	D1_N	CLK_P	CLK_N	D2_P	D2_N	D3_P	D3_N
	1	1	1	D2_P	D2_N	D1_P	D1_N	CLK_P	CLK_N	D0_P	D0_N	D3_P	D3_N
CPHY	0	0	0	NC	A0	B0	C0	A2	B2	C2	A1	B1	C1
	0	0	1	NC	A1	B1	C1	A2	B2	C2	A0	B0	C0
	0	1	0	NC	A0	B0	C0	A1	B1	C1	A2	B2	C2
	0	1	1	NC	A2	B2	C2	A1	B1	C1	A0	B0	C0
	1	0	0	NC	C0	B0	A0	C2	B2	A2	C1	B1	A1
	1	0	1	NC	C1	B1	A1	C2	B2	A2	C0	B0	A0
	1	1	0	NC	C0	B0	A0	C1	B1	A1	C2	B2	A2
	1	1	1	NC	C2	B2	A2	C1	B1	A1	C0	B0	A0

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6.3 MIPI-DSI Interface (D-option)

6.3.1 General description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface Level : Low level communication
- Packet level : High level communication

6.3.2 Interface level communication

6.3.2.1 General

The display module uses data and clock lane differential pairs for DSI . Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode. Data lane1 can be driven High Speed mode only.

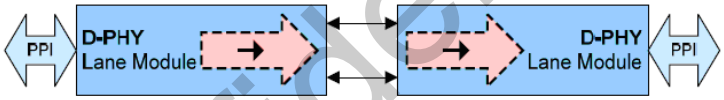
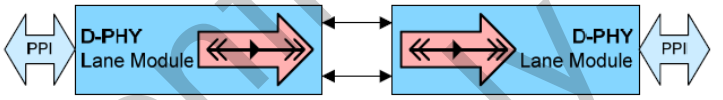
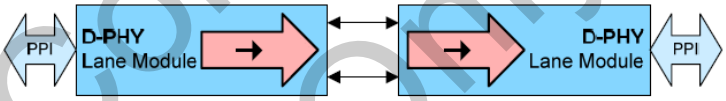
-	Lane support mode	MPU(Host) FT8201AA(Slave)
Clock Lane	Unidirectional lane • High-Speed Clock only • Simplified Escape Mode (ULPS Only)	
Data Lane0	Bi-directional lane • Forward high-speed only • Bi-directional Escape Mode • Bi-direction LPDT	
Data Lane1	Unidirectional lane • Forward high-speed only • Simplified Escape Mode (ULPS Only)	

Table: Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table: High Speed and Low-Power Lane Pair State Descriptions

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6.3.2.2 DSI-CLK lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

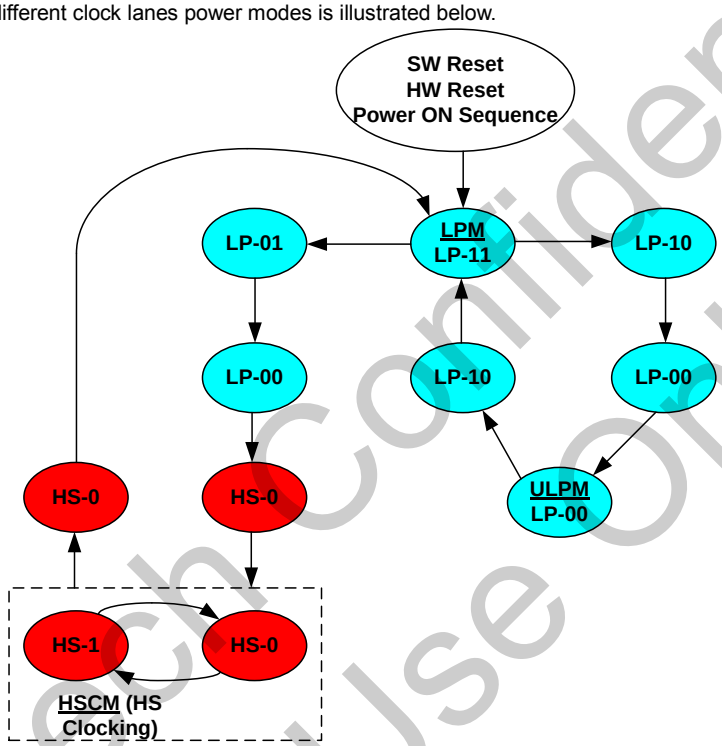

Figure: Clock Lanes Power Modes

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

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Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

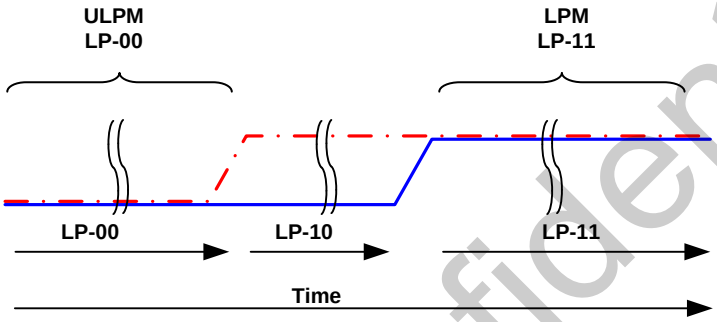

Figure: From ULPM to LPM

3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

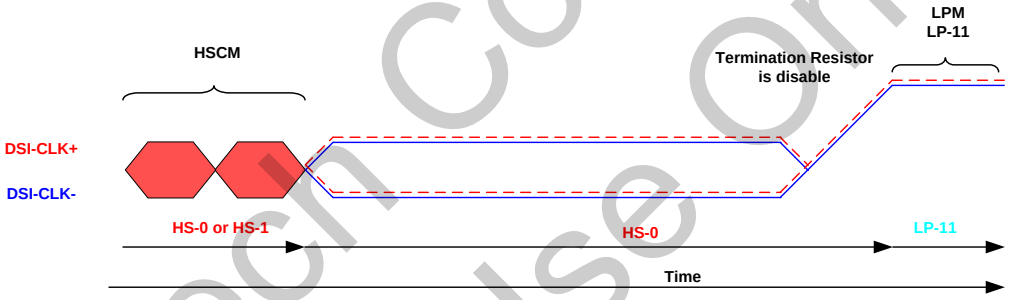

Figure: From HSCM to LPM

All three mode changes are illustrated a flow chart below.

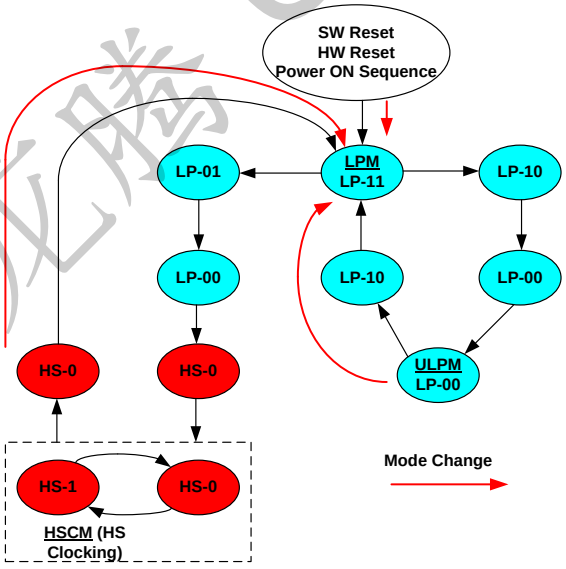

Figure: All three mode changes to LPM

Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM).

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This sequence is illustrated below.

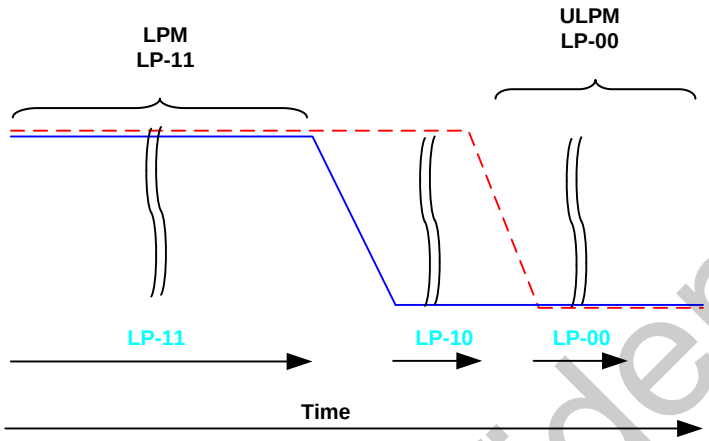

Figure: From LPM to UPLM

The mode change is also illustrated below:

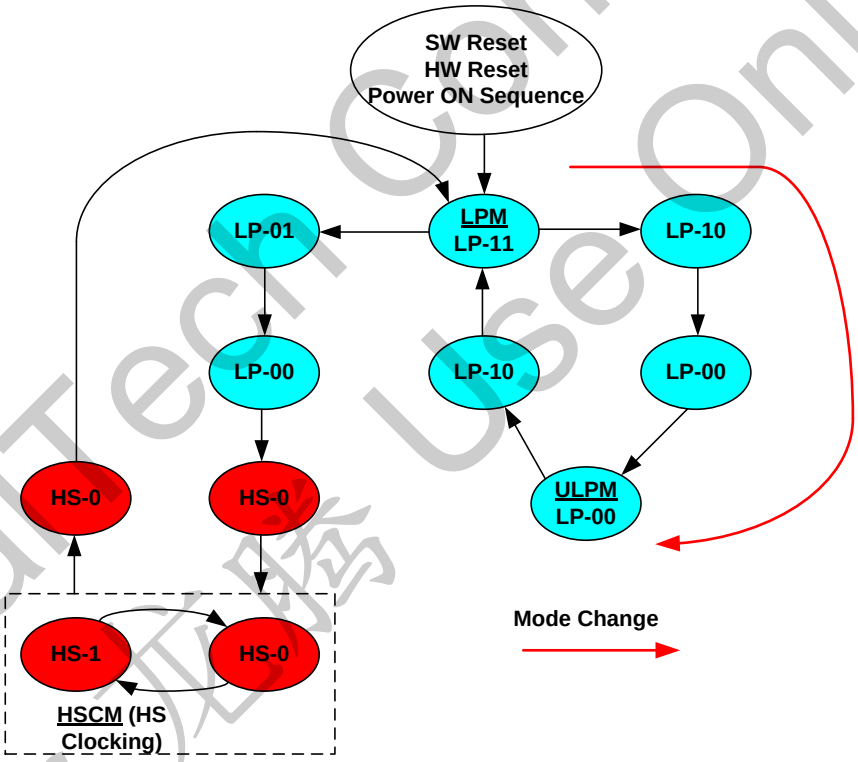

Figure: The mode change from LPM to UPLM

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High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM).

This sequence is illustrated below.

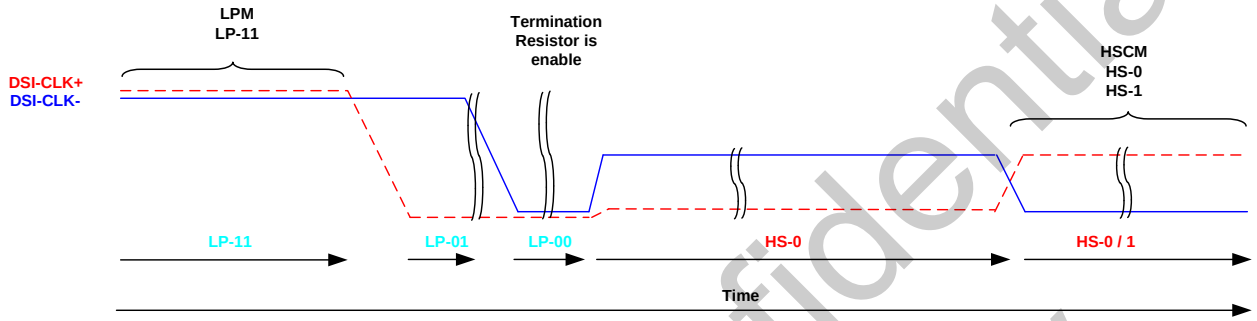

Figure: From LPM to HSCM

The mode change is also illustrated below:

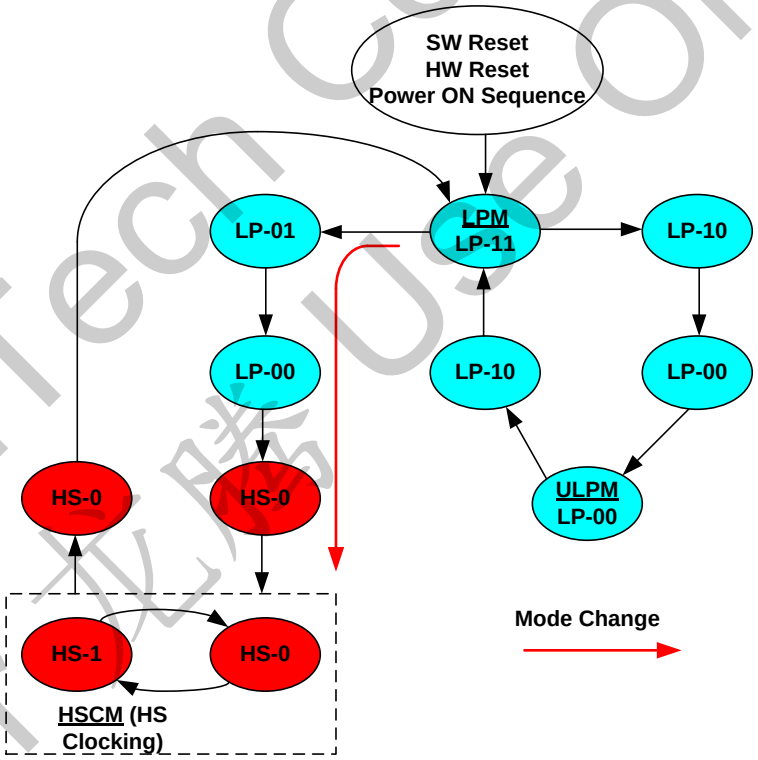

Figure: Mode change from LPM to HSCM

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The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

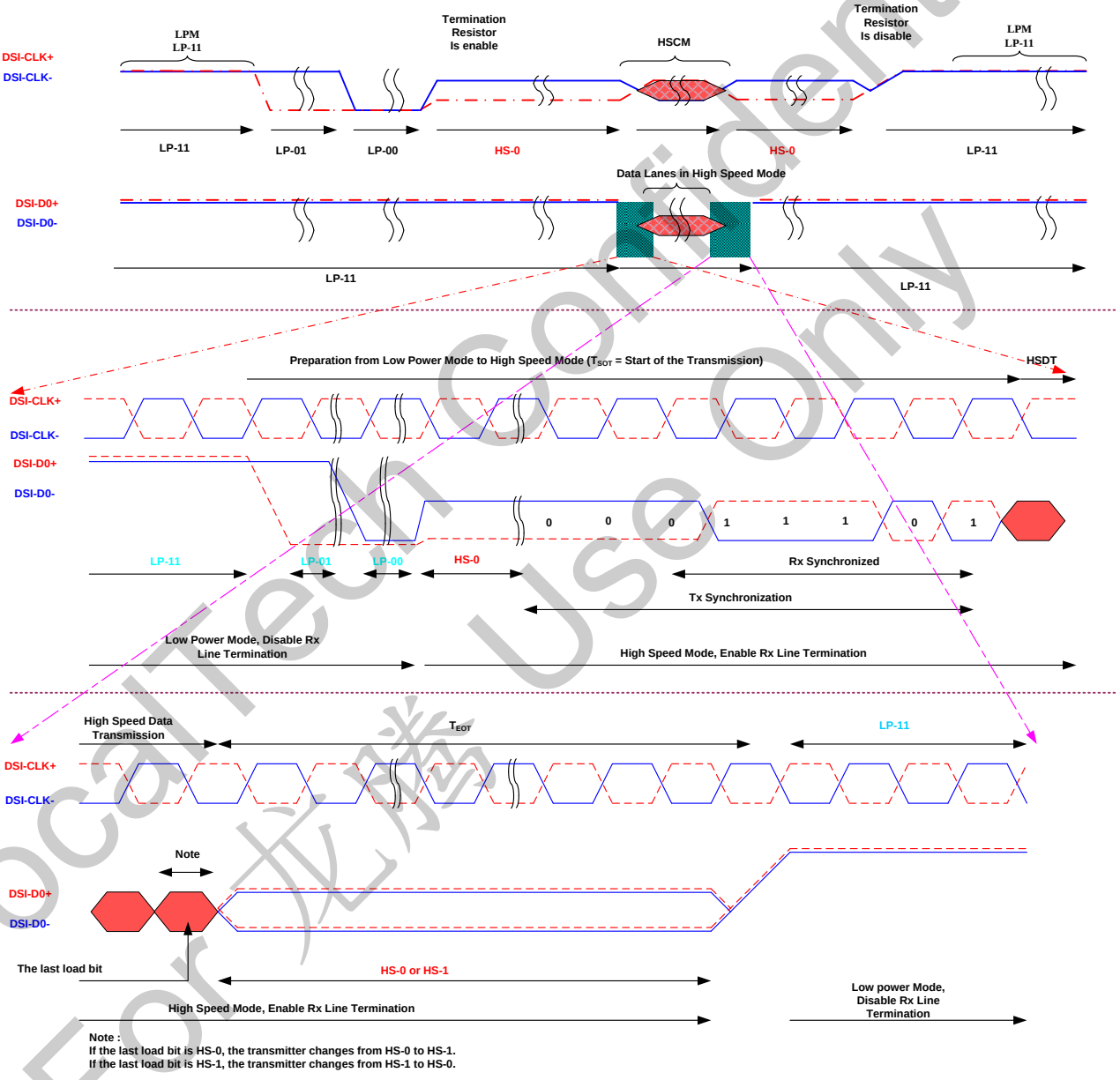

Figure: High speed clock burst

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6.3.3 DSI data lanes

6.3.3.1 General

DSI-Dn+/- Data Lanes can be driven in different modes which are:

- Escape Mode (only support DSI_D0 data lane pair)
- High-Speed Data Transmission (support all data lane pairs)
- Bus Turnaround Request (only support DSI_D0 data lane pair)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	LP-00 =>LP-10 =>LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z, Note

Table: Entering and leaving sequences

6.3.3.2 Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and Reverse direction.

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command , which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit.
- A payload stream if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action.

All currently available Escape mode commands and actions are list below.

- Send or receive “Low-Power Data Transmission” (LPDT)
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is resetting the display module (same as S/W Reset function)
- Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the MCU,
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU.

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The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.

For Data Lane1 and 2, only support ULPS Escape mode commands.

- Drive data lanes to "Ultra-Low Power State" (ULPS)

The basic construction is illustrated below:

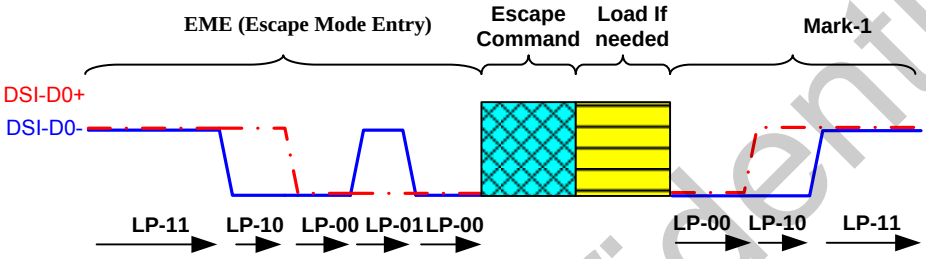

Figure: General Escape mode sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided 2 different groups: Mode or Trigger. Escape command groups are defined below.

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001bin
Ultra-Low Power Mode	Mode	0001 1110bin
Remote Application Reset	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin
Acknowledge	Trigger	0010 0001 bin

Table: Escape commands

The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode.

The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Payload (Data):
  - One or more bytes
  - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

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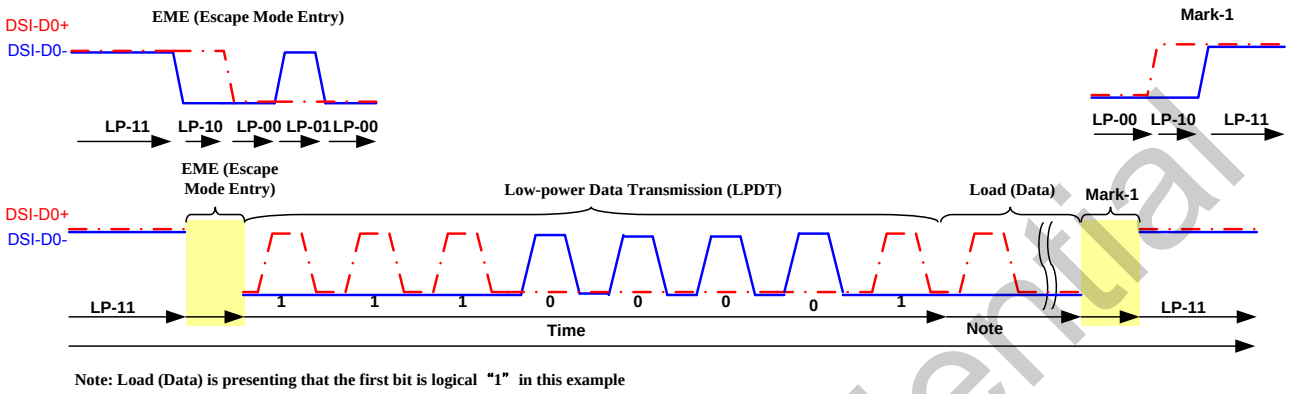

Note: Load (Data) is presenting that the first bit is logical "1" in this example

Figure: Low-power data transmission

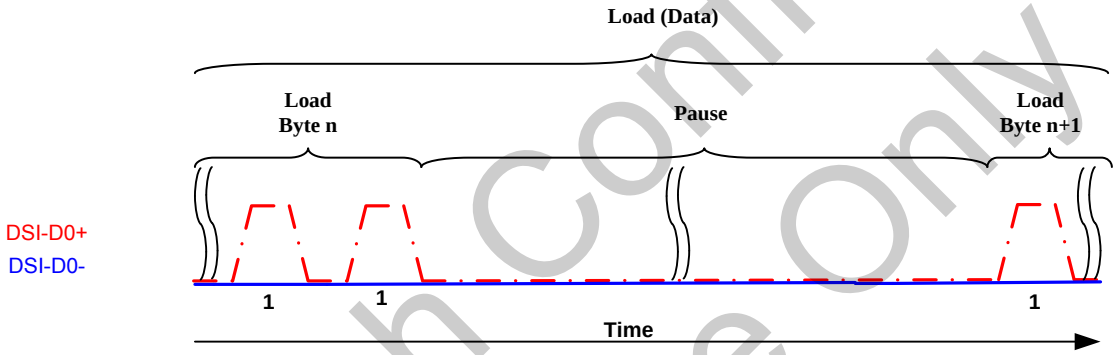

Figure: Pause (example)

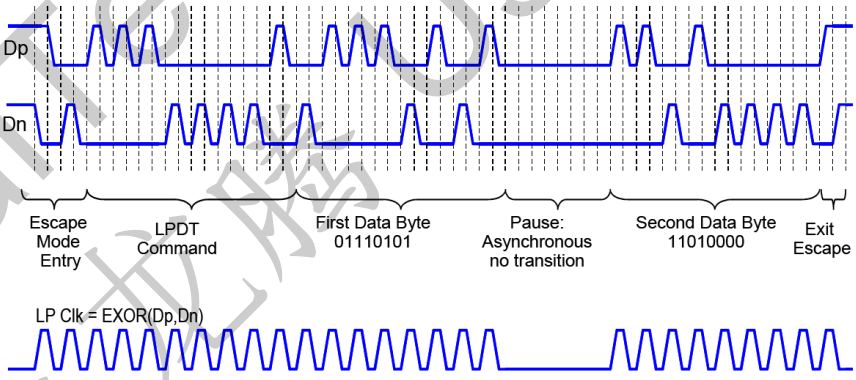

Figure: Two Data Byte Low-Power Data Transmission Example

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Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

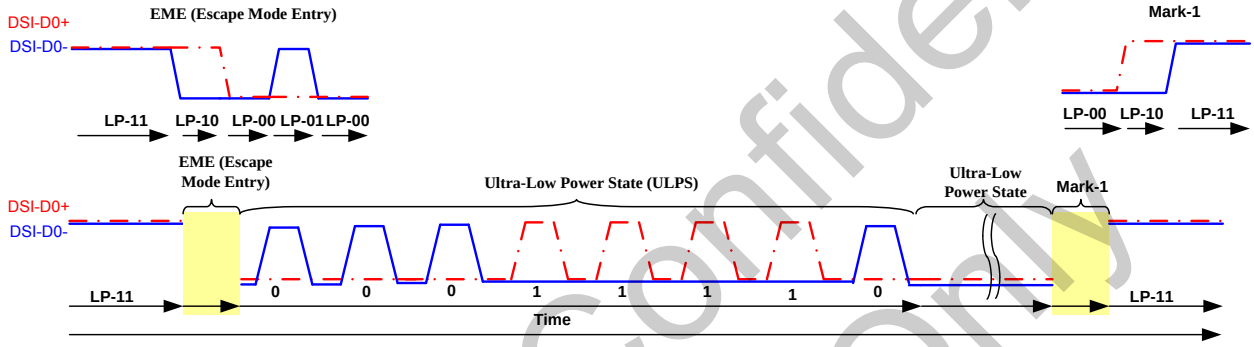

Figure: Ultra-low power state (ULPS)

Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

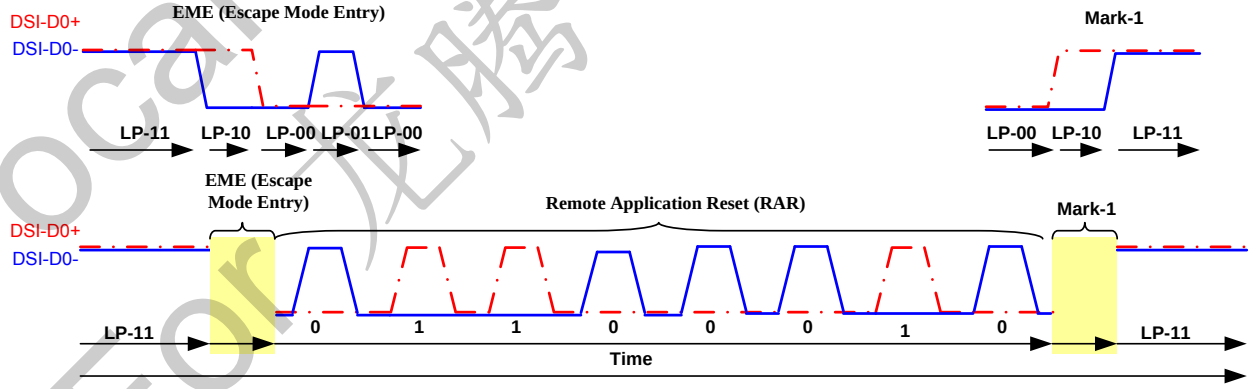

Figure: Remote Application Reset (RAR)

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Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

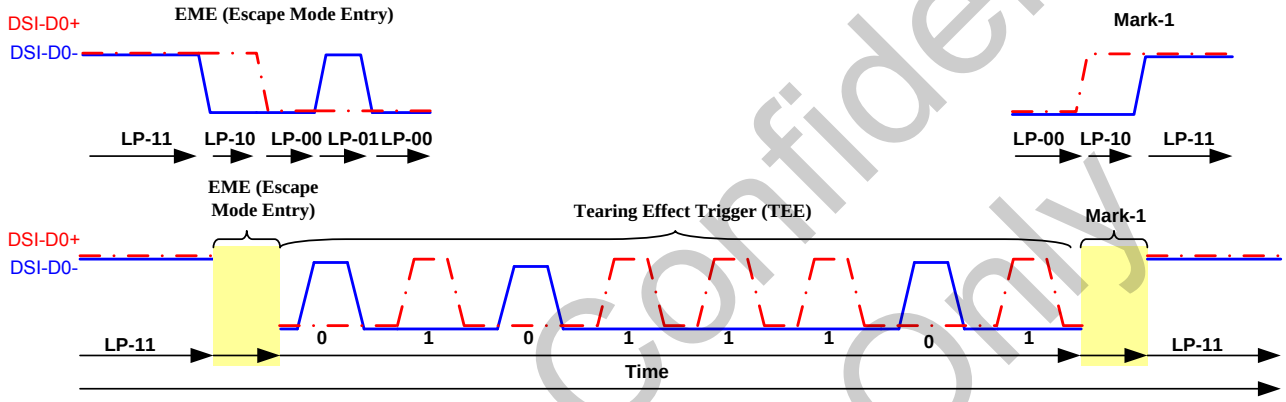

Figure: Tearing effect (TEE)

Acknowledgement (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

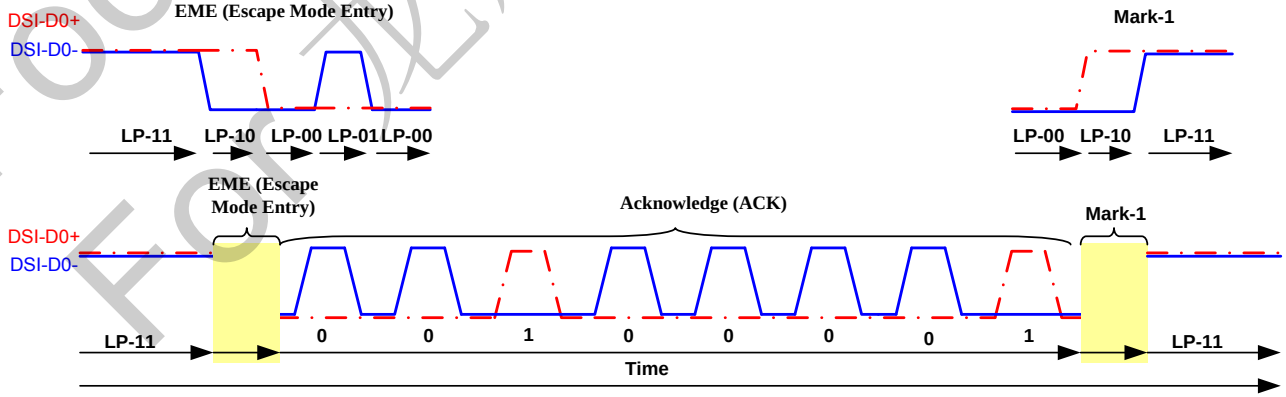

Figure: Acknowledgement (ACK)

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6.3.3.3 High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (T_{sot} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are entering (TSOT) in the High-Speed Data Transmission(HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below.

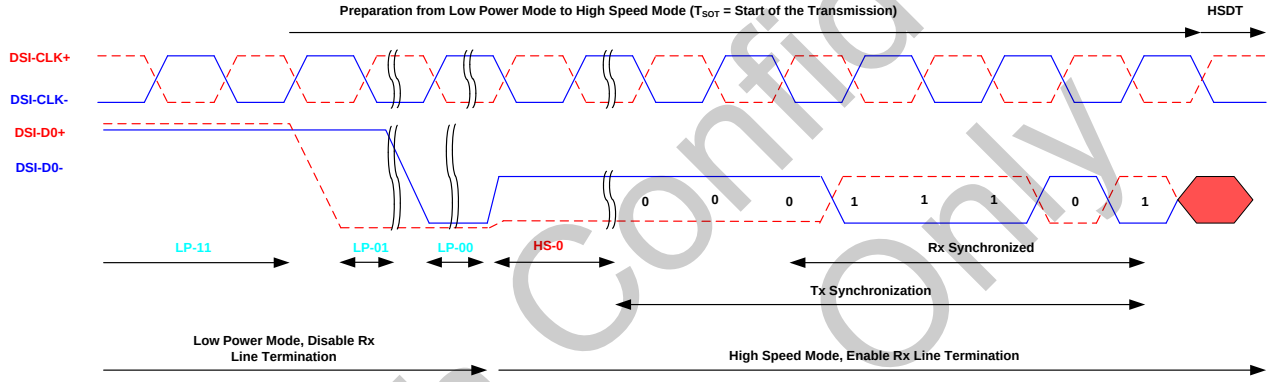

Figure: Tsot of HSDT

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Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI- CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes
DSI-D0+/- are in LP-11 mode. See more information on chapter “7.2.2 High-Speed Clock Mode (HSCM)”.
Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - MCU changes to HS-1, if the last load bit is HS-0
  - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

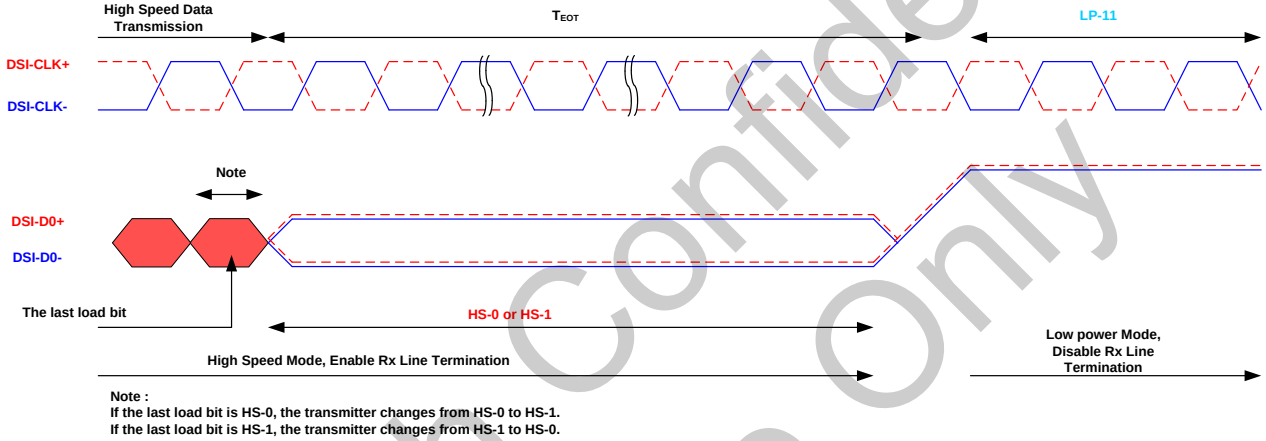

Figure: TEOT of HSDT

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets.
These data packets can be Long (Lpa) or Short (Spa) packets. These packets are defined on chapter “Short Packet (Spa) and Long Packet (Lpa) Structures“.
These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

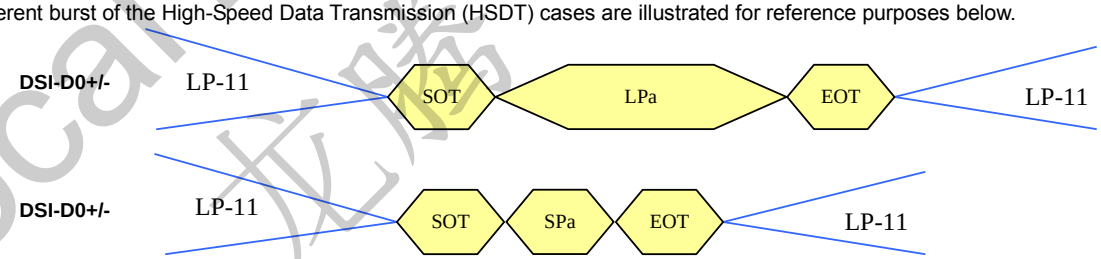

Figure: Single packet in HSDT

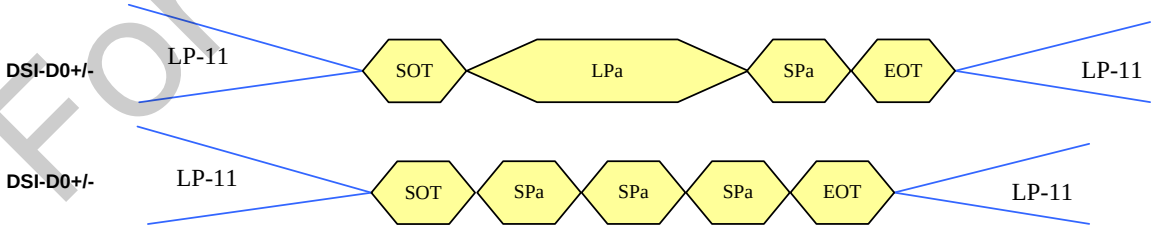

Figure: Multiple packets in HSDT

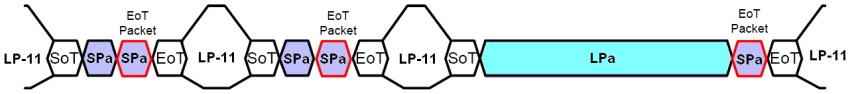

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Figure: Packets with EoT package in HSDT

Abbreviation	Explanation
LP-11	Low Power Mode, Data lanes are ‘1’s (Stop Mode)
SOT	Start of the Transmission
Lpa	Long Packet
Spa	Short Packet
EOT	End of the Transmission

Table: Abbreviations

6.3.3.4 Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU and display module are using the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follows.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00
- The MCU waits until the display module is starting to control DSI-D0+/- data lanes and the MCU stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

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6.4 MIPI-DSI Interface (C-option)

6.4.1 General description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface Level : Low level communication
- Packet level : High level communication

6.4.2 Interface level communication

6.4.2.1 General

The display module uses data and clock lane differential pairs for DSI .

Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode.

Data lane1 and Data lane2 can be driven High Speed mode only.

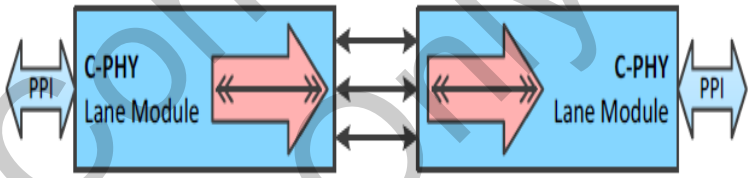
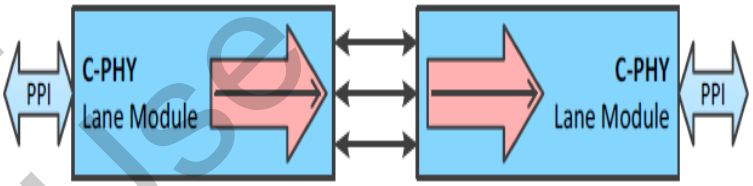
-	Lane support mode	MPU(Host) FT8722(Slave)
Data Lane0	Bi-directional lane • Forward high-speed only • Bi-directional Escape Mode • Bi-direction LPDT	
Data Lane1/2	Unidirectional lane • Forward high-speed only • Simplified Escape Mode (ULPS Only)	

Table: Lane types and support mode

Low Power mode means that each line of the three differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that three differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) three lanes are defined below.

State Code	Line DC Voltage Levels			High Speed (HS)	Low-Power (LP)	
	A Line	B Line	C Line	Burst Mode	Control Mode	Escape Mode
HS_+X	High (HS)	Low (HS)	Mid (HS)	+x state	Note 1	Note 1
HS_-X	Low (HS)	High (HS)	Mid (HS)	-x state	Note 1	Note 1
HS_+Y	Mid (HS)	High (HS)	Low (HS)	+y state	Note 1	Note 1
HS_-Y	Mid (HS)	Low (HS)	High (HS)	-y state	Note 1	Note 1
HS_+Z	Low (HS)	Mid (HS)	High (HS)	+z state	Note 1	Note 1
HS_-Z	High (HS)	Mid (HS)	Low (HS)	-z state	Note 1	Note 1
LP-000	Low (LP)	Low (LP)	Low (LP)	Not Defined	Bridge	Space

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LP-001	Low (LP)	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-100	High (LP)	Low (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-111	High (LP)	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table: High Speed and Low-Power Lane State Descriptions

6.4.2.2 DSI-CLK

CPHY doesn't have separated clock lane and clock will be recovered from each data trio.

6.4.3 DSI data lanes

6.4.3.1 General

DSI-Dn a/b/c data trios can be driven in different modes which are:

- Escape Mode (only support DSI_D0 data trio)
- High-Speed Data Transmission (support all data trios)
- Bus Turnaround Request (only support DSI_D0 data trio)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-111 =>LP-100 =>LP-000 =>LP-001 =>LP-000	LP-000 =>LP-100 =>LP-111 (Mark-1)
High-Speed Data Transmission	LP-111 =>LP-001 =>LP-000 =>HS-preamble	(HS-0 or HS-1) =>LP-111
Bus Turnaround Request	LP-111 =>LP-100 =>LP-000 =>LP-100 =>LP-000	High-Z, Note

Table: Entering and leaving sequences

6.4.3.2 Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and Reverse direction.

The basic sequence of the Escape Mode is as follow

- Start: LP-111
- Escape Mode Entry : LP-111 =>LP-100 =>LP-000 =>LP-001 =>LP-000
- Escape Command , which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit.
- A payload stream if it is needed
- Exit Escape (Mark-1) LP-000 =>LP-100 =>LP-111
- End: LP-111

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action.

All currently available Escape mode commands and actions are list below.

- Send or receive "Low-Power Data Transmission" (LPDT)
- Drive data lanes to "Ultra-Low Power State" (ULPS)
- Indicate "Remote Application Reset" (RAR), which is resetting the display module (same as S/W Reset function)
- Indicate "Tearing Effect" (TEE), which is used for a TE line event from the display module to the MCU,
- Indicate "Acknowledge" (ACK), which is used for a non-error event from the display module to the MCU.

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The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.

For data Lane1 and 2, only support ULPS Escape mode commands.

- Drive data lanes to "Ultra-Low Power State" (ULPS)

The basic construction is illustrated below:

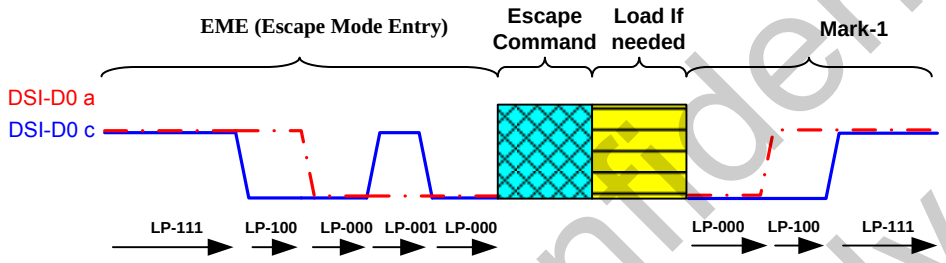

Figure: General Escape mode sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided 2 different groups: Mode or Trigger. Escape command groups are defined below.

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001bin
Ultra-Low Power Mode	Mode	0001 1110bin
Remote Application Reset	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin
Acknowledge	Trigger	0010 0001 bin

Table: Escape commands

The MCU is informing to the display module that it is controlling data lanes (DSI-D0 a/b/c) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode.

The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-111
- Escape Mode Entry : LP-111 =>LP-100 =>LP-000 =>LP-001 =>LP-000
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

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- Payload (Data):

  - One or more bytes

  - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

- Mark-1: LP-000 =>LP-100 =>LP-111
- End: LP-111

This sequence is illustrated for reference purposes below:

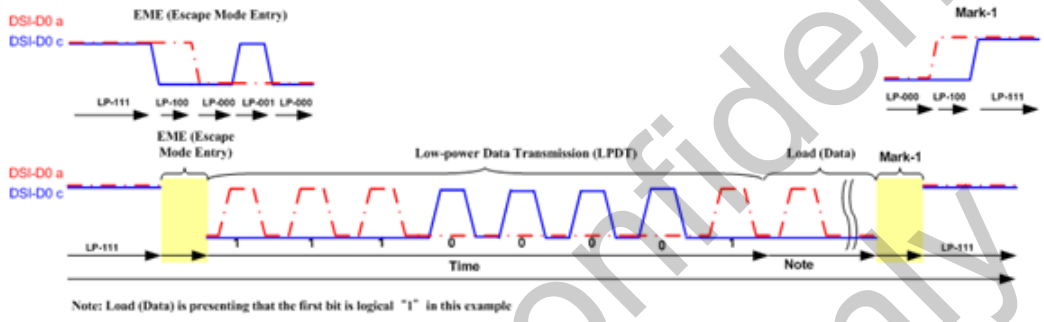

Figure: Low-power data transmission

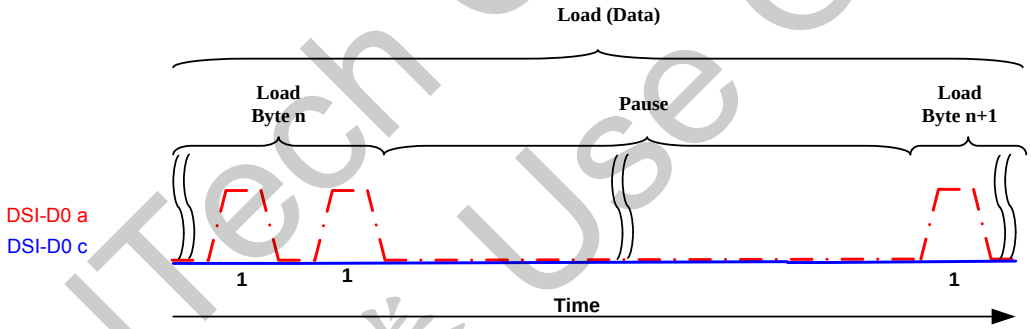

Figure: Pause (example)

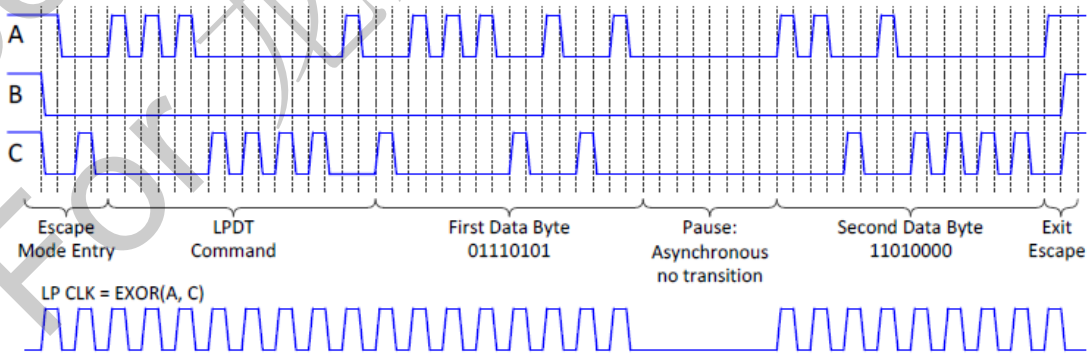

Figure: Two Data Byte Low-Power Data Transmission Example

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

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The Ultra-Low Power State (ULPS) is using a following sequence:

Start: LP-111

- Escape Mode Entry : LP-111 =>LP-100 =>LP-000 =>LP-001 =>LP-000
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-000 =>LP-100 =>LP-111
- End: LP-111

This sequence is illustrated for reference purposes below:

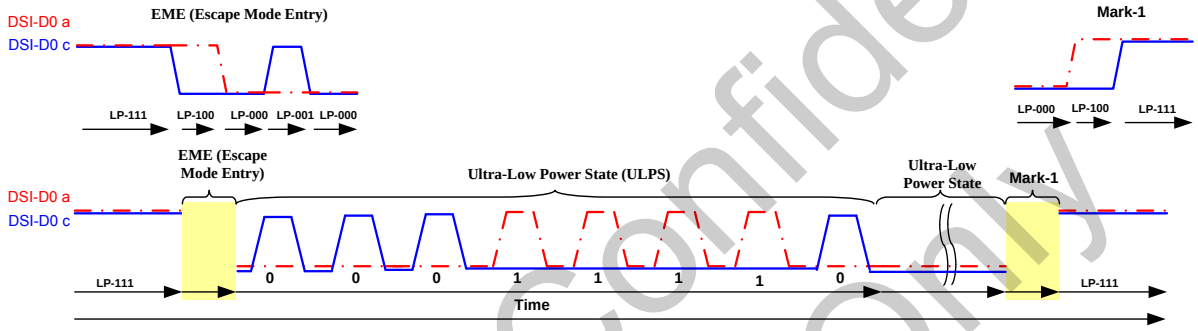

Figure: Ultra-low power state (ULPS)

Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset is using a following sequence:

- Start: LP-111
- Escape Mode Entry : LP-111 =>LP-100 =>LP-000 =>LP-001 =>LP-000
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-000 =>LP-100 =>LP-111
- End: LP-111

This sequence is illustrated for reference purposes below:

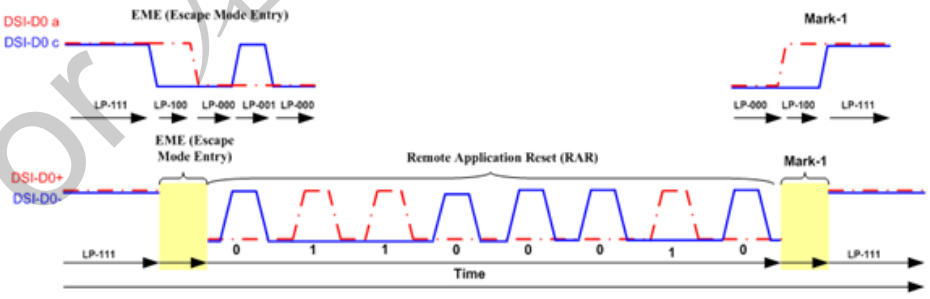

Figure: Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing

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Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-111
- Escape Mode Entry: LP-111 =>LP-100 =>LP-000 =>LP-001 =>LP-000
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-000 =>LP-100 =>LP-111
- End: LP-111

This sequence is illustrated for reference purposes below:

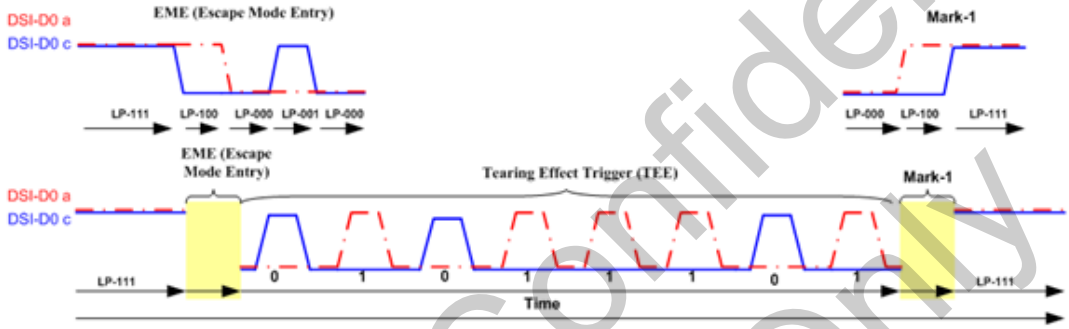

Figure: Tearing effect (TEE)

Acknowledgement (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-111
- Escape Mode Entry: LP-111 =>LP-100 =>LP-000 =>LP-001 =>LP-000
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-000 =>LP-100 =>LP-111
- End: LP-111

This sequence is illustrated for reference purposes below:

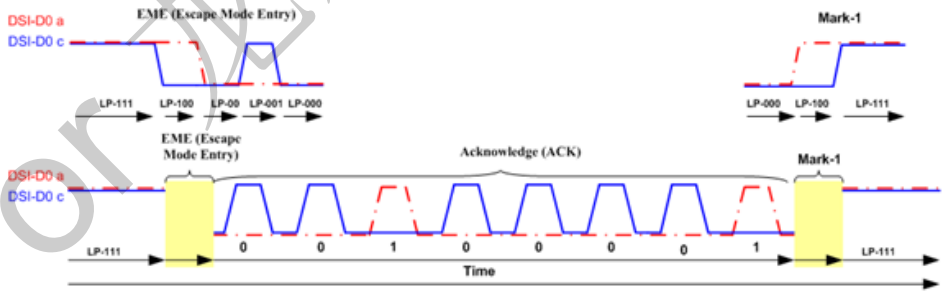

Figure: Acknowledgement (ACK)

6.4.3.3 High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (T_{sot} of HSDT)

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Data lanes DSI-D0 a/b/c of the display module are entering (TSOT) in the High-Speed Data Transmission(HSDT) as follows

- Start: LP-111
- HS-Request: LP-001
- HS-Settle: LP-000 => HS-preamble (Rx: Lane Termination Enable)
- Rx Synchronization: 3444443
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below.

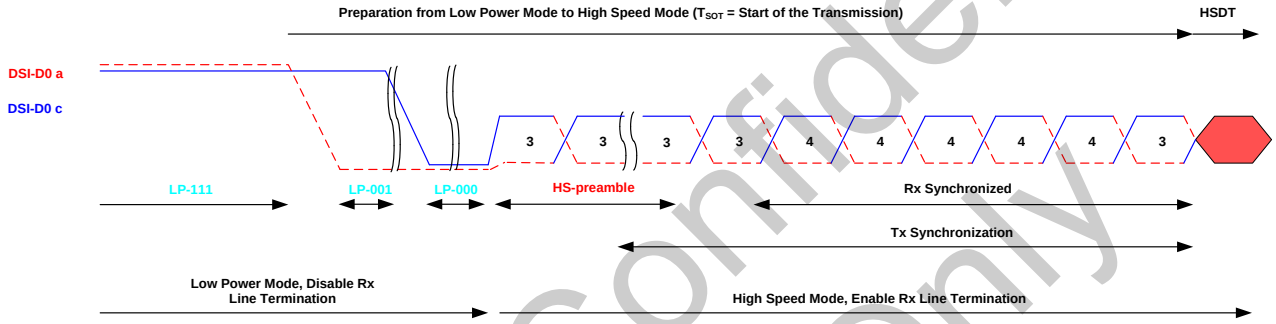

Figure: Tsot of HSDT

Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

Data lanes DSI-D0 a/b/c of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - MCU sends 49 symbols 4 for POST
- End: LP-111 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

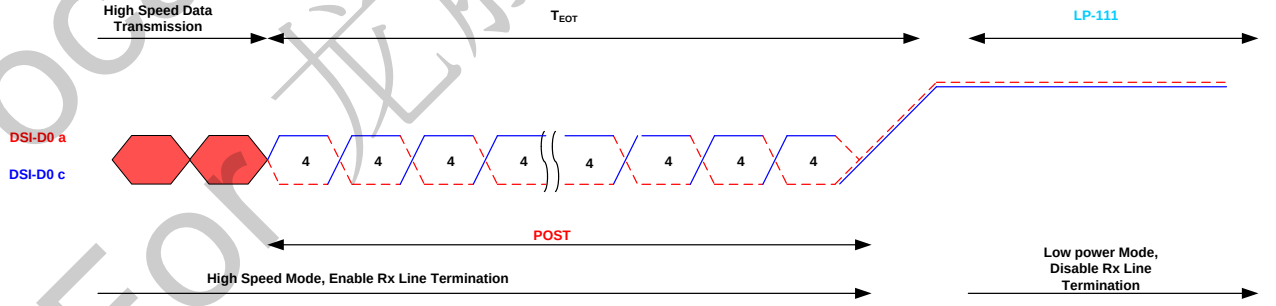

Figure: TEOT of HSDT

Burst of the High-Speed Data Transmission (HSDT)

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The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “Short Packet (SPa) and Long Packet (LPa) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

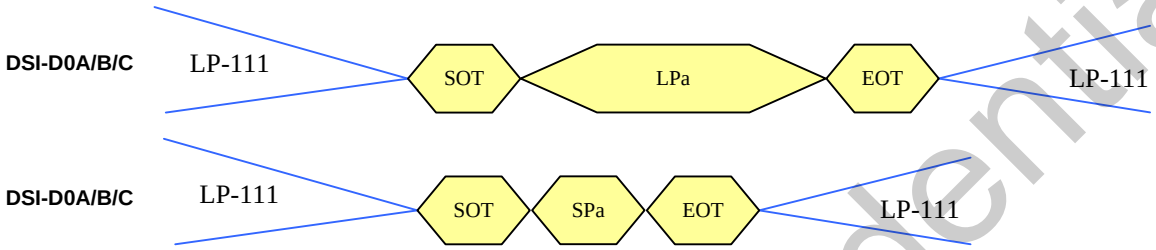

Figure: Single packet in HSDT

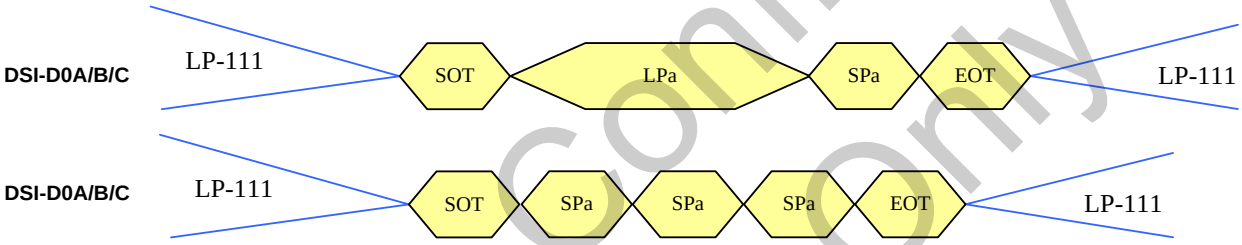

Figure: Multiple packets in HSDT

Figure: Packets with EoT package in HSDT

Abbreviation	Explanation
LP-111	Low Power Mode, Data lanes are ‘1’s (Stop Mode)
SOT	Start of the Transmission
LPa	Long Packet
SPa	Short Packet
EOT	End of the Transmission

Table: Abbreviations

6.4.3.4 Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU and display module are using the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follows.

- Start (MCU): LP-111
- Turnaround Request (MCU): LP-111 =>LP-100 =>LP-000

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- The MCU waits until the display module is starting to control DSI-D0+/- data lanes and the MCU stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-000 =>LP-100 =>LP-111

The same bus turnaround procedure (From the MCU to the display module) is illustrated below.

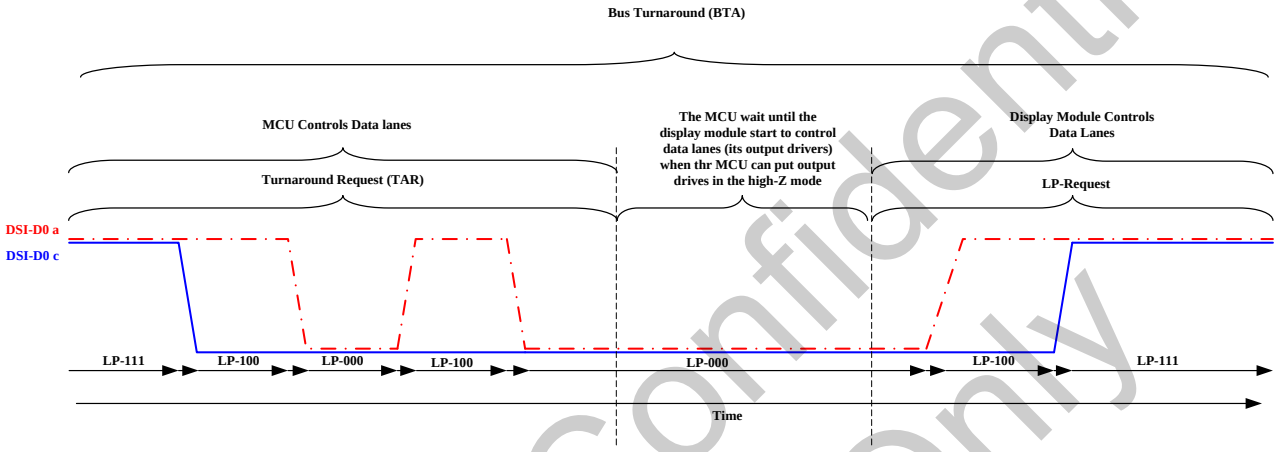

Figure: Bus turnaround procedure

6.4.3.5 Multi-lane High Speed Transmission

Since an HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of lanes, some lanes may run out of data before others. Therefore, the lane management layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for which there is no further data.

Although all lanes start simultaneously with parallel SoTs, each lane operates independently and may complete the HS transmission before the other lanes, sending an EoT one cycle (two bytes) earlier.

The N PHYs on the receiving end of the link collect bytes in parallel and feed them into the lane management layer. The lane management layer reconstructs the original sequence of bytes in the transmission.

The following figure shows ways an HS Transmission can terminate for two or three lanes HS transmission.

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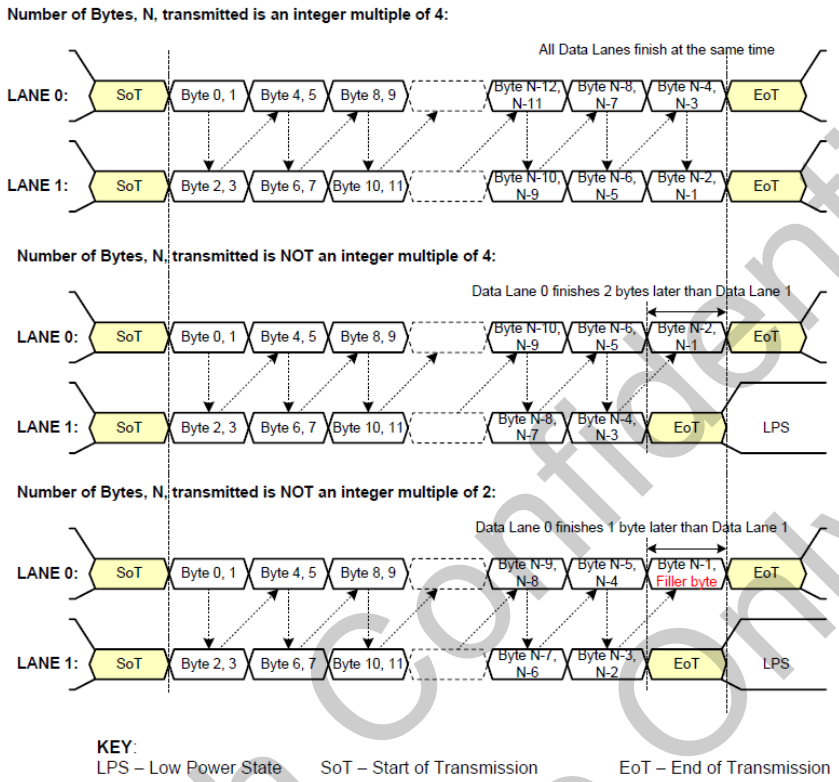
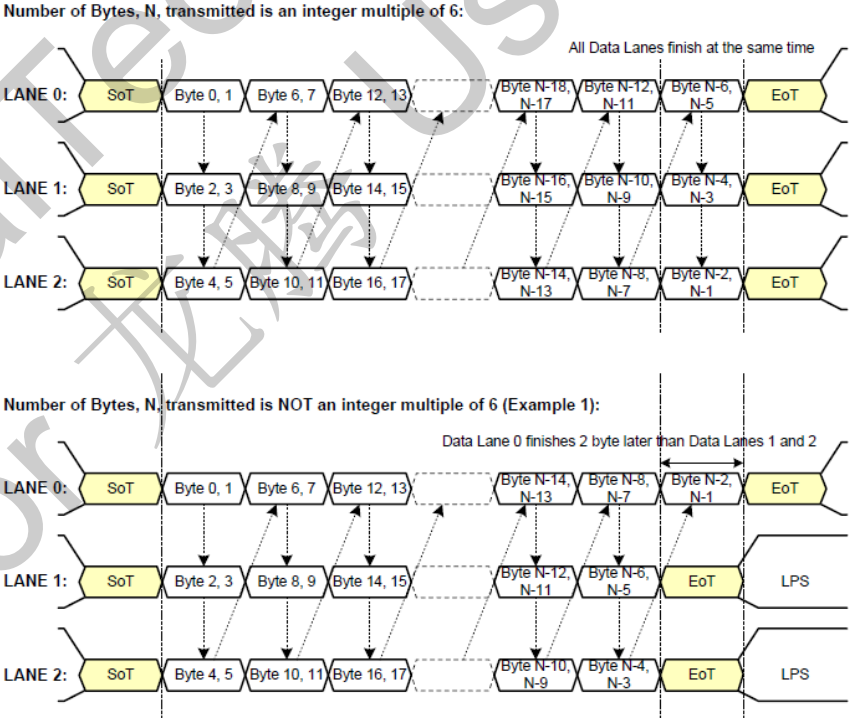


Figure: Two data-lane HS transmission example



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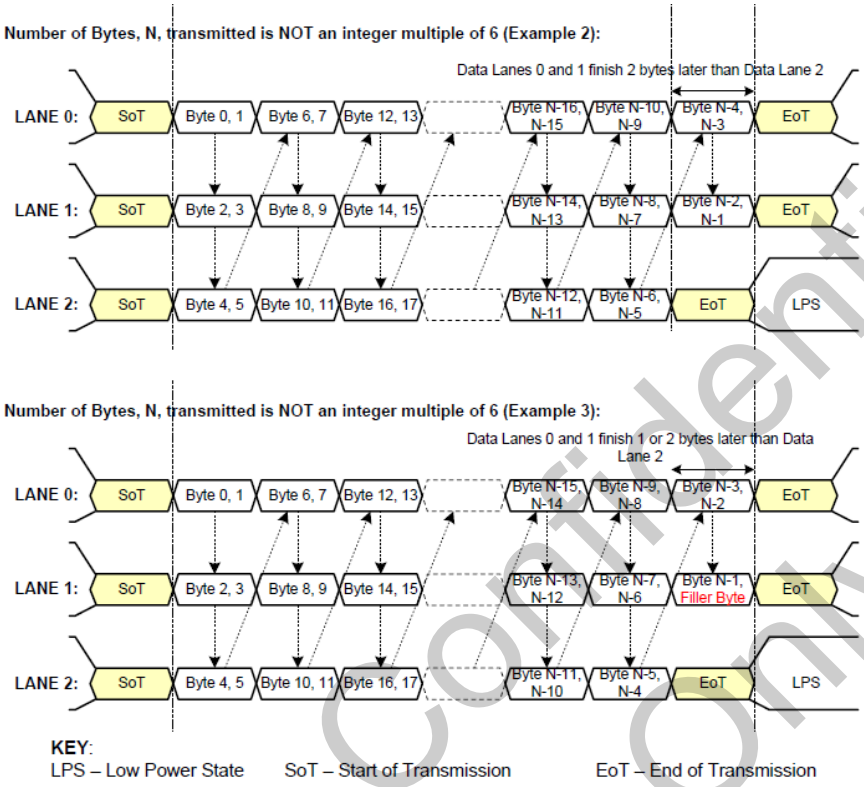

Figure: Three data-lane HS transmission example

6.4.4 Packet level communication

6.4.4.1 Short Packet (SPa) and Long Packet (LPa) structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The packet structure and length are both different between in LPDT and HSDT

LPDT:

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

HSDT:

- Short Packet (SPa): 12 bytes (6 bytes packet header replicate)
- Long Packet (LPa): From 14 to 65,549 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

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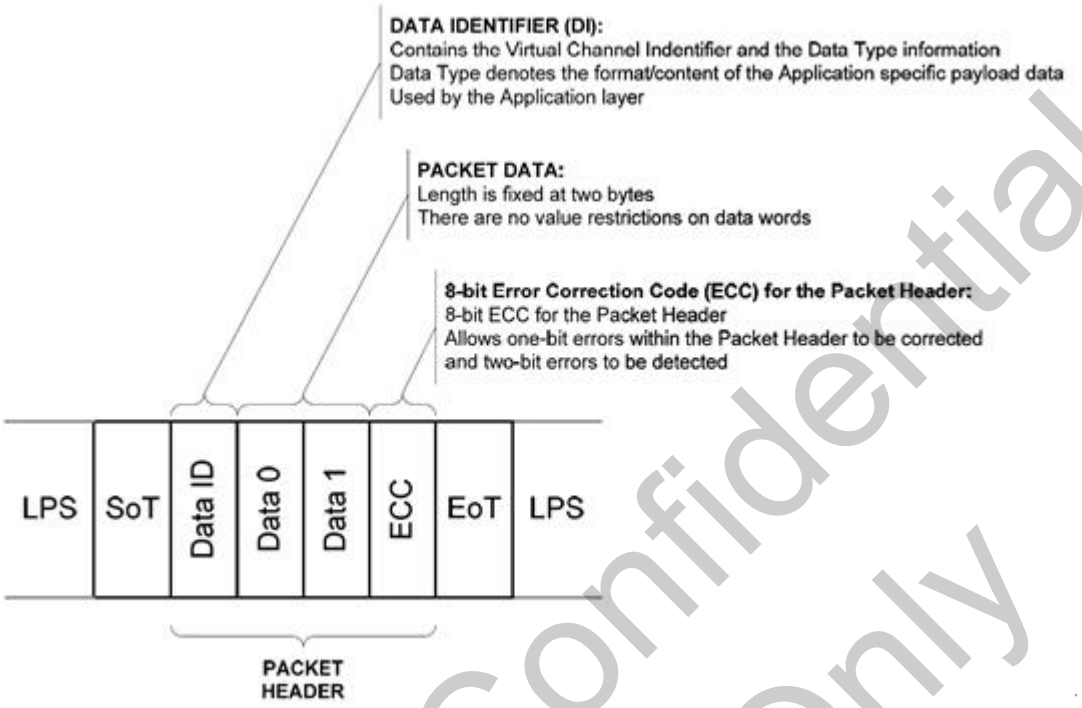

Figure: Short packet structure in LPDT

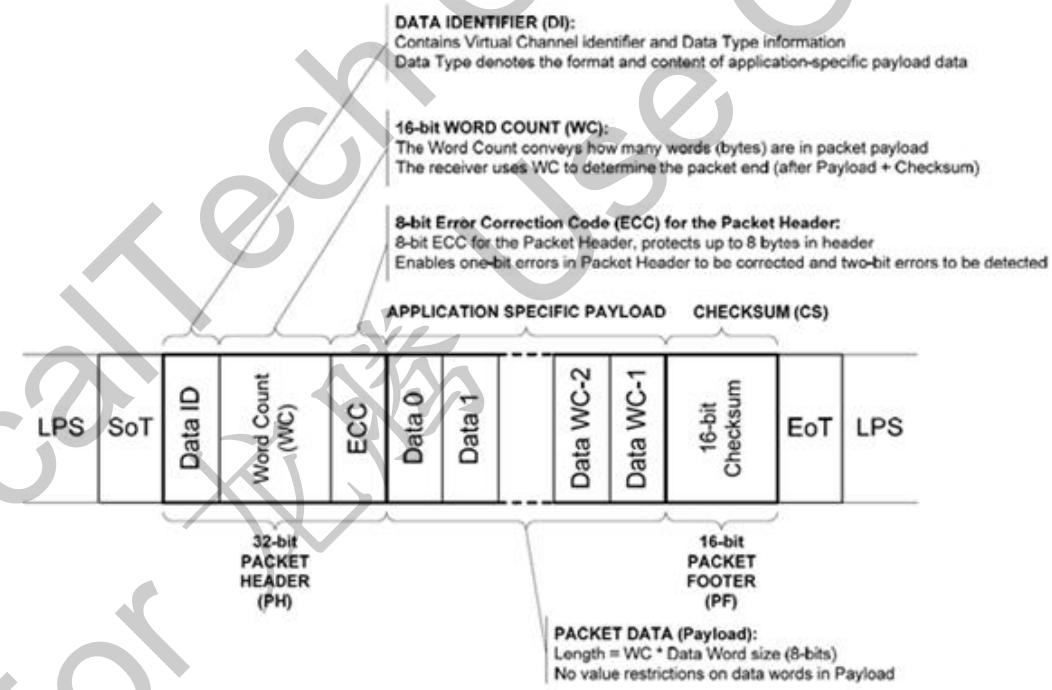

Figure: Long packet structure in LPDT

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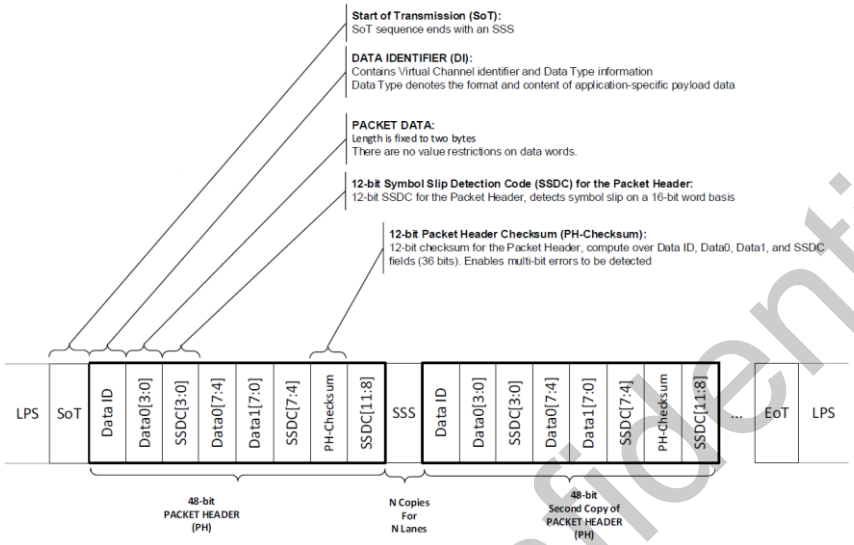

Figure: Short packet structure in HSDT

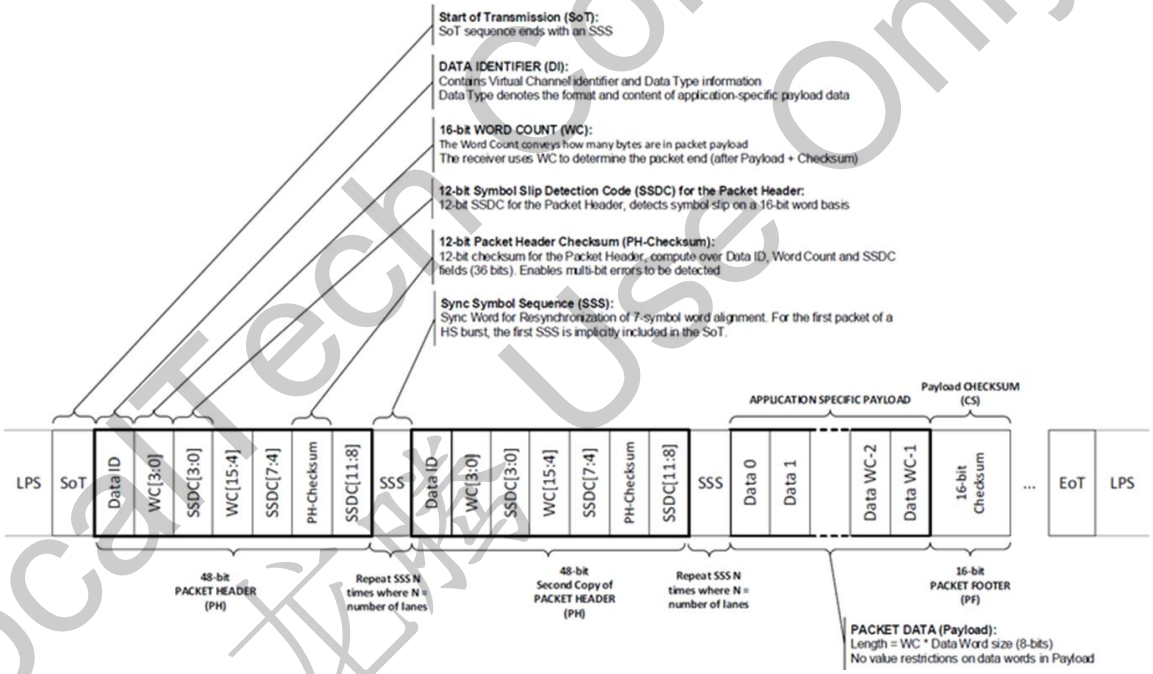

Figure: Long packet structure in HSDT

Note: Short Packet (SPa) Structure" and Long Packet (LPa) Structure" are presenting a single packet sending (= Includes LP-111, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-111 between packets if packets have sent in multiple packet format. e.g.:

- LP-111 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-111
- LP-111 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-111
- LP-111 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-111

Bit Order of the Byte on Packets

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte

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fields, the least significant byte shall be transmitted first unless otherwise specified.

The following figures shows complete long packet data transmission in escape mode operation and in high speed operation respectively. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

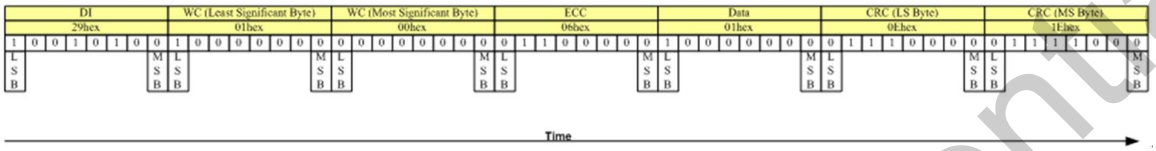

Figure: Bit order of the byte on packets in LPDT

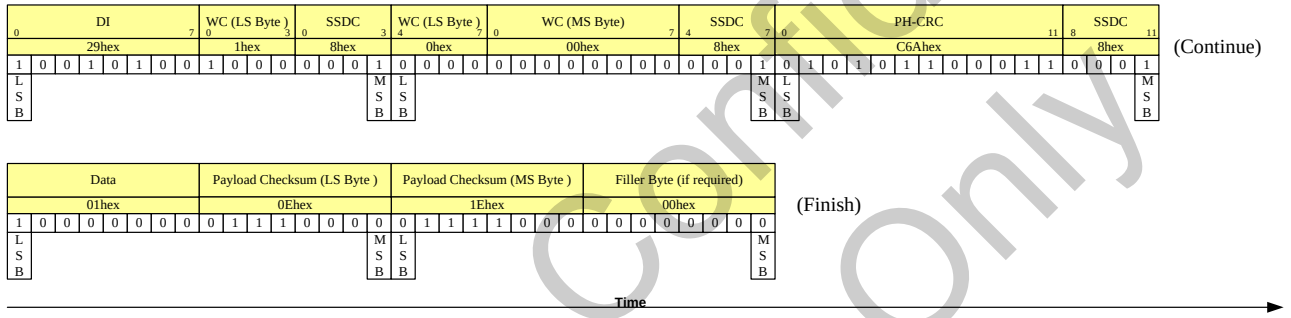

Figure: Bit order of the 2-byte on packets in HSDT

Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last.

e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

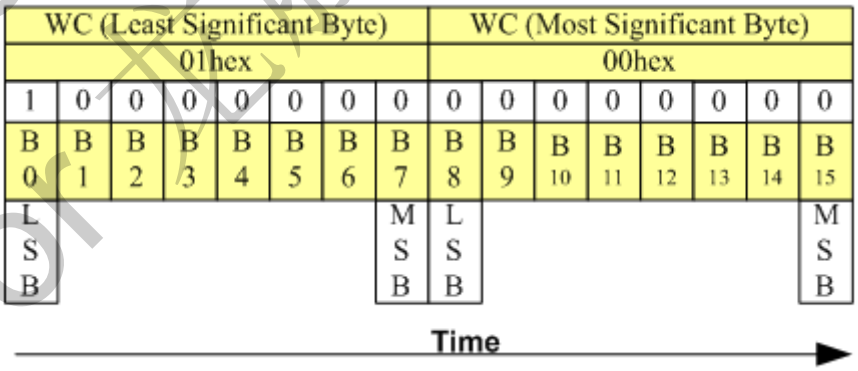

Figure: Byte order of the multiple byte information on packets

Packet Head (PH)

The packet header is always consisting of 4 bytes in LPDT (the same as D-option) and replicate 6 bytes in HSDT. The following sections only descript the content of packet header in HSDT.

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The content of packet header are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1st 16-bit word: Data Identification (DI), Packet Data0 and SSDC => DI[7:0], Data0[3:0] and SSDC[3:0]
- 2nd 16-bit word: Packet Data0, Data1 and SSDC => Data0[7:4], Data1[7:0] and SSDC[7:4]
- 3rd 16-bit word: Packet Header Checksum(PH-CRC) and SSDC => PH-CRC[11:0] and SSDC[11:8]

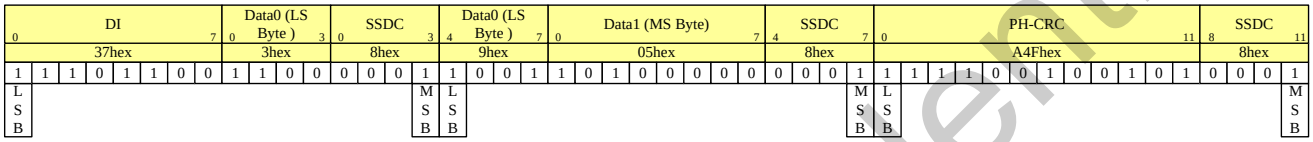

Figure: Packet head on short packet in HSDT

Long Packet (LPa):

- 1st 16-bit word: Data Identification (DI), Word Count 0 and SSDC => DI[7:0], WC0[3:0] and SSDC[3:0]
- 2nd 16-bit word: Packet Word Count 0, Word Count 1 and SSDC => WC0[7:4], WC1[7:0] and SSDC[7:4]
- 3rd 16-bit word: Packet Header Checksum(PH-CRC) and SSDC => PH-CRC[11:0] and SSDC[11:8]

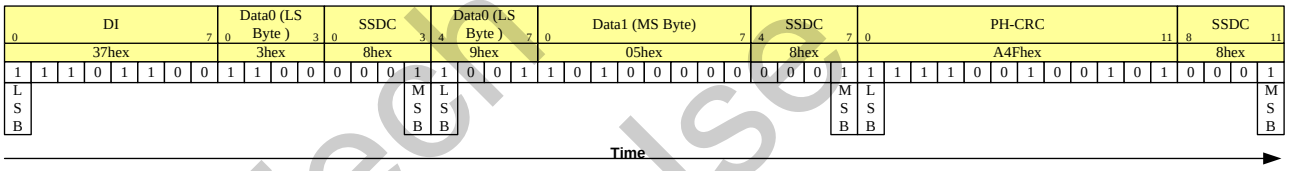

Figure: Packet head on long packet

Data Identification

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

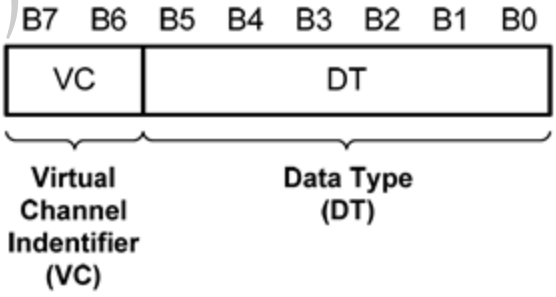

Table: Data identification structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

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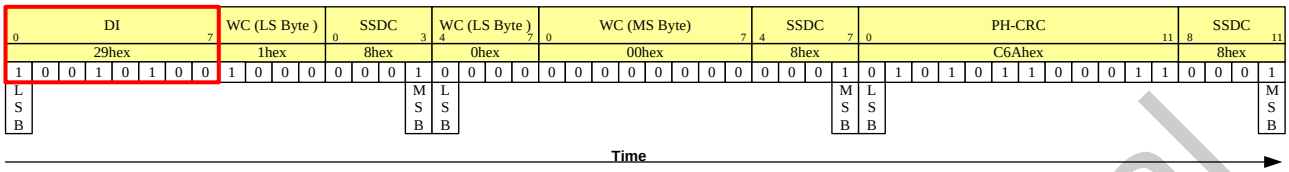

Figure: Data identification of the packet head

Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

FT8722 **only support VC code=00, package with other VC code(01/10/11) will be filter out.**

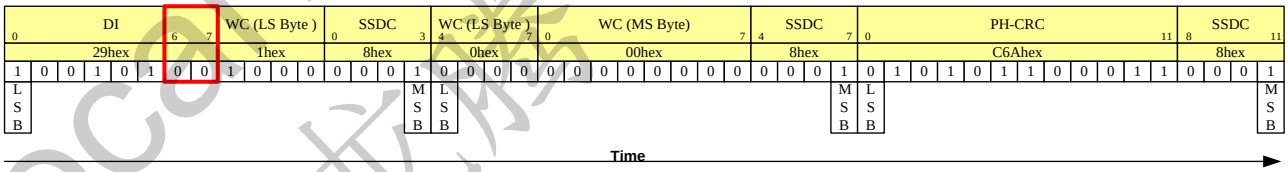

Figure: Virtual channel on the packet head

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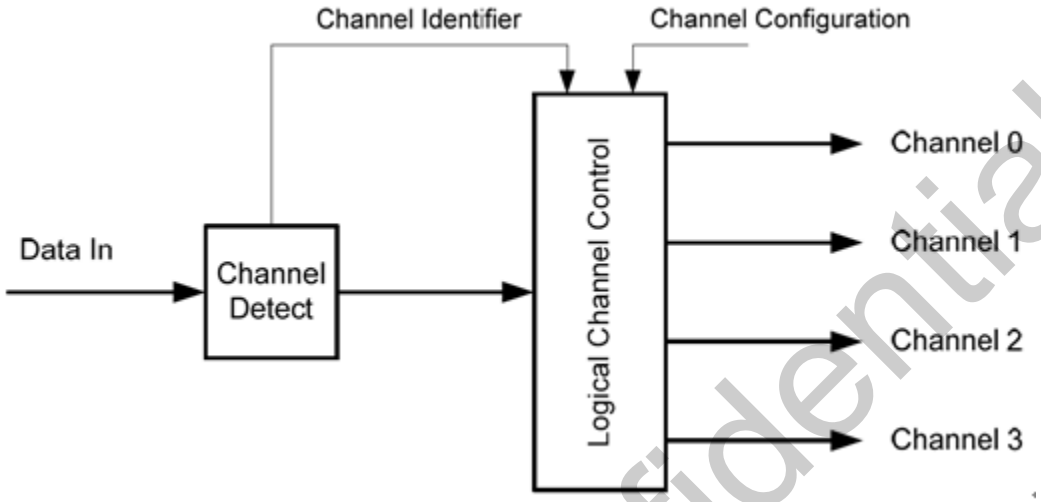

Figure: Virtual channel block diagram (receiver case)

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

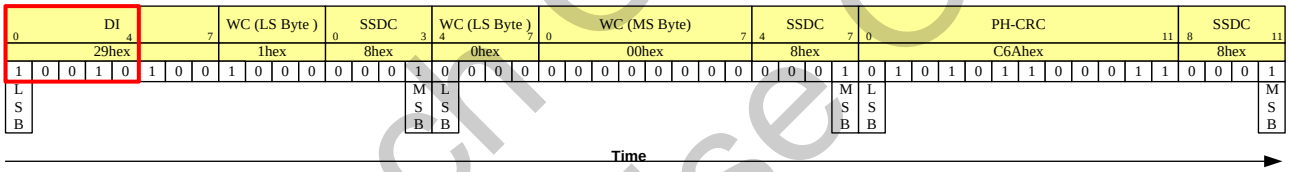

Figure: Data type on the packet head

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

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From the MCU to the Display module		
Data Type (HEX)	Data Type (Binary)	Description
01h	00 0001	Sync Event, V Sync Start
11h	01 0001	Sync Event, V Sync End
21h	10 0001	Sync Event, H Sync Start
31h	11 0001	Sync Event, H Sync End
07h	00 0111	Compression Mode Command
08h	00 1000	End of Transmission packet (EoTp, D-option only)
02h	00 0010	Color Mode (CM) Off Command
12h	01 0010	Color Mode (CM) On Command
22h	10 0010	Shut Down Peripheral Command
32h	11 0010	Turn On Peripheral Command
03h	00 0011	Generic Short WRITE, no parameters
13h	01 0011	Generic Short WRITE, 1 parameters
23h	10 0011	Generic Short WRITE, 2 parameters
04h	00 0100	Generic READ, no parameters
14h	01 0100	Generic READ, 1 parameters
24h	10 0100	Generic READ, 2 parameters
05h	00 0101	DCS WRITE, no parameters
15h	01 0101	DCS WRITE, 1 parameters
06h	00 0110	DCS READ, no parameters
16h	01 0110	Execute Queue
27h	10 0111	Scrambling Mode Command
37h	11 0111	Set Maximum Return Packet Size
09h	00 1001	Null Packet, no data
19h	01 1001	Blanking Packet, no data
29h	10 1001	Generic Long Write
39h	11 1001	DCS Long Write/Write_LUT Command packet
0Ah	00 1010	Picture Parameter Set
0Bh	00 1011	Compressed Pixel Stream
0Dh	00 1101	Packed Pixel Stream, 30-bit RGB, 10-10-10 Format
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format

Table: Data type from the MCU to the display module

From the Display Module to the MCU		
Data Type (HEX)	Data Type (Binary)	Description
02h	00 0010	Acknowledge & Error Report
1Ch	01 1100	DCS Long READ Response
21h	10 0001	DCS Short READ Response, 1 byte returned
22h	10 0010	DCS Short READ Response, 2 byte returned

Table: Data type from the display module to the MCU

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The receiver is ignored other Data Type (DT) if they are not defined on tables above. Host send “Generic Read” data type, FT8722 will return DCS Read package to Host.

Packet data on the short packet

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to 00h, if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 2 bytes are illustrated for reference purposes below.

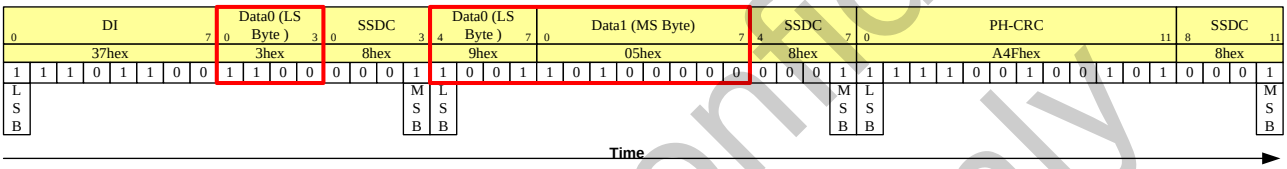

Figure: Packet data on the short packet, 2 bytes information

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Word count on the long packet

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI)has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

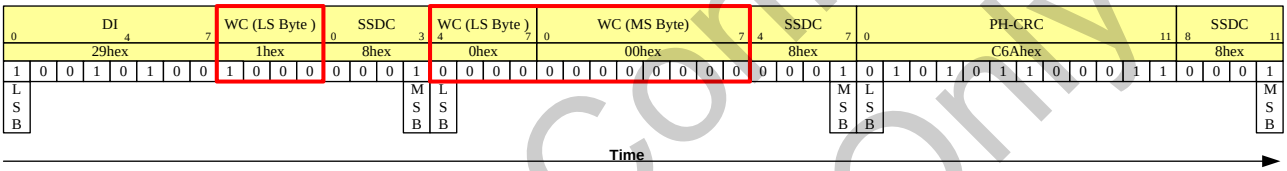

Figure: Word count on the long packet

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Symbol Slip Detection Code (SSDC)

The 12-bit Symbol Slip Detection Code (SSDC) allows detection of a symbol slip in each of the 16-bit words of the packet header. The MCU shall always transmit the SSDC for Packets transmitted in high speed mode and set the 12-bit SSDC of the packet header to the value 0x888.

SSDC[11:0] is illustrated for reference purposes below.

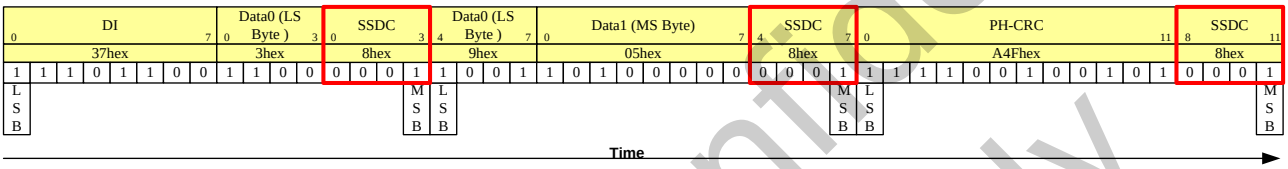

Figure: SSDC[11:0] on the short packet

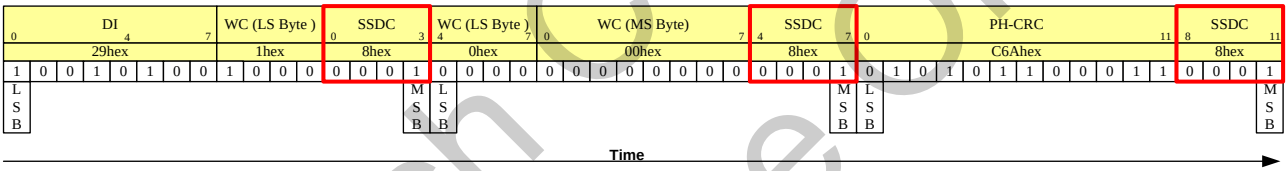

Figure: SSDC[11:0] on the long packet

Packet Header Checksum (PH-CRC)

The Packet Header Checksum(PH-CRC) allows single 3-phase encoded wire state error to be detected. The MCU shall always calculate and transmit the PH-CRC for packets transmitted in high speed mode.

The PH-CRC shall be realized as a 12-bit CRC with a generator polynomial of: $x^{12} + x^8 + x^7 + x^6 + x^5 + x^4 + x^0$

The CRC shift register shall be initialized to the value 0xFFF before the packet header enters. The packet header enters as a bitwise data stream from the left, least significant bit of the least significant byte first. The MCU and display module shall include the SSDC in the packet header checksum calculation.

PH-CRC[11:0] is illustrated for reference purposes below.

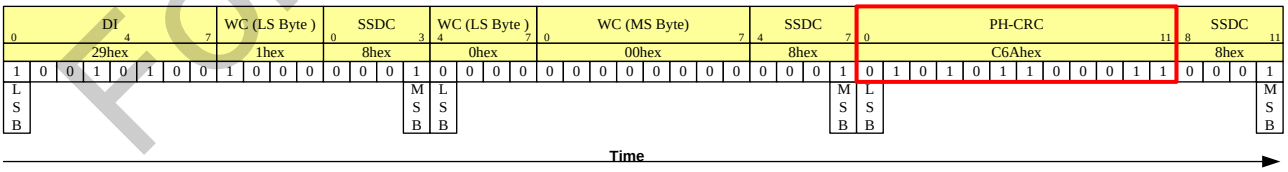

Figure: PH-CRC[11:0] on the short packet

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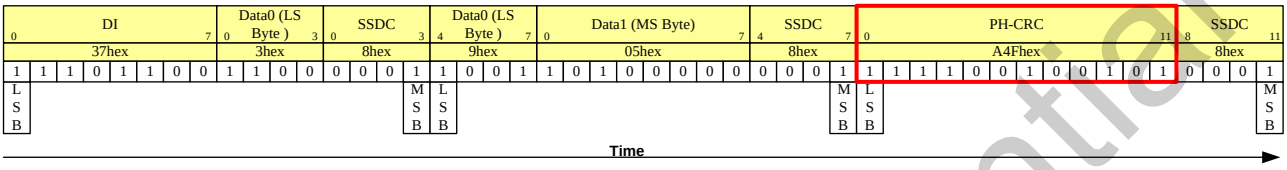

Figure: PH-CRC [11:0] on the long packet

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Packet footer on the long packet

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

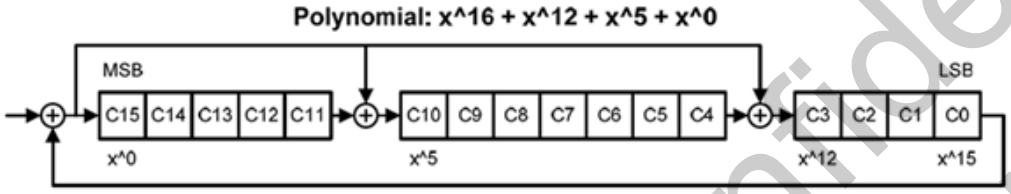

Figure: 16-bit cyclic redundancy check (CRC) calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

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6.4.4.2 Packet transmissions

Packet from the MCU to the display module

Display Command Set (DCS), which is defined on chapter “Instructions” is used from the MCU to the display module.

This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) in escape mode as these are illustrated below.

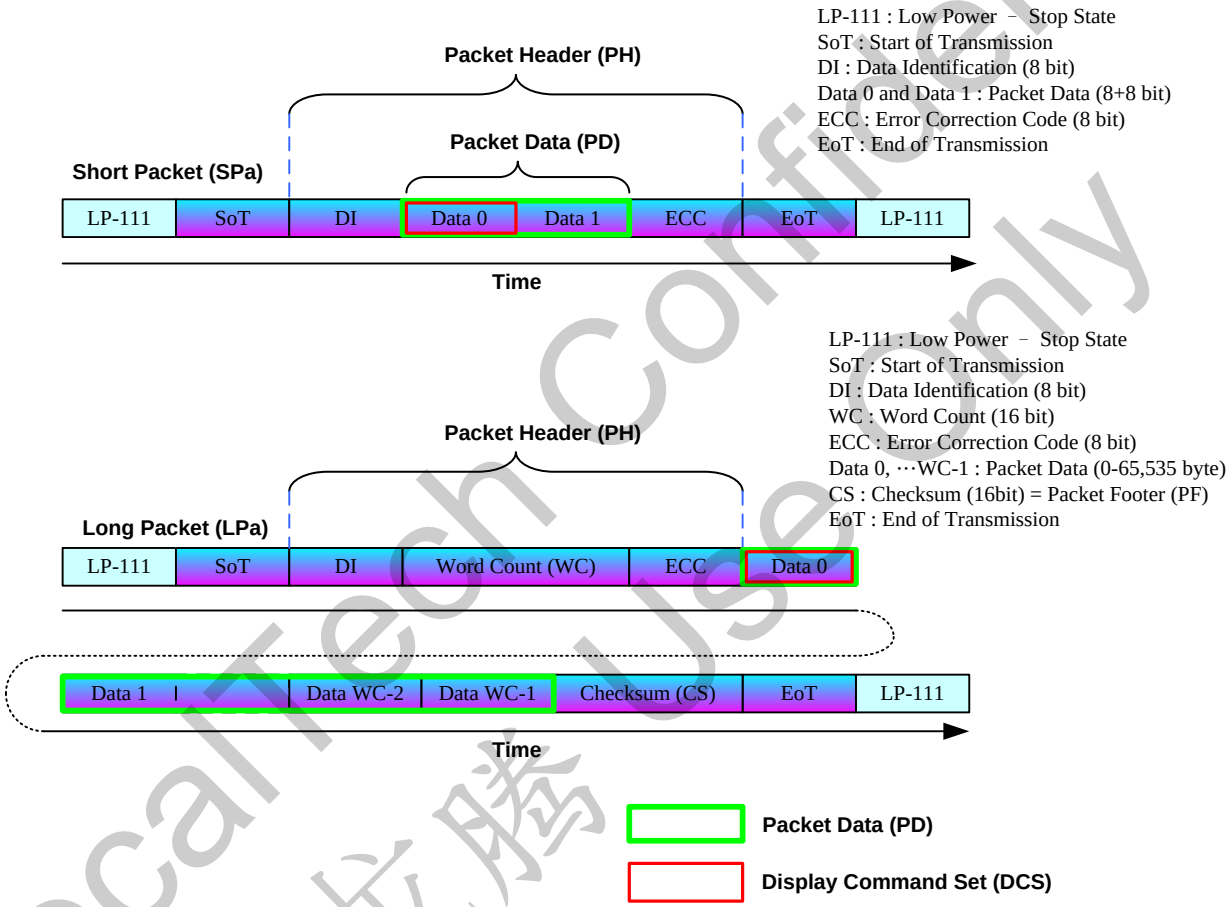

Figure: DCS on the short packet and long packet

Packet from the display module to the MCU

Used packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS).

The used packet type is defined on Data Type (DT).

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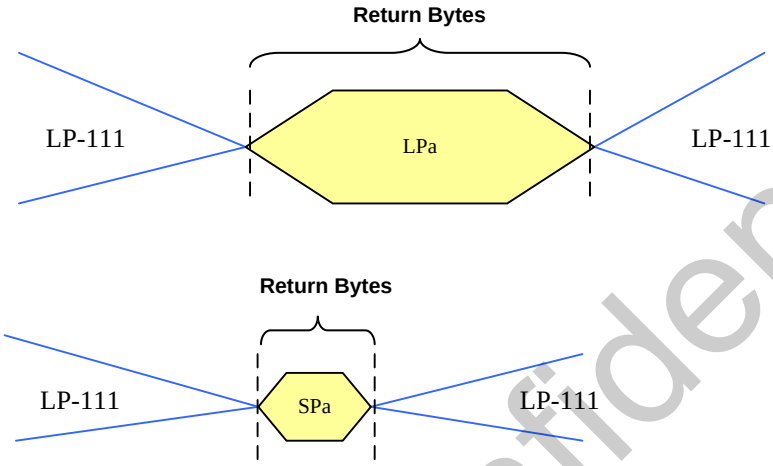

Figure: Return bytes on single packet

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Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to 1 , as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Protocol Timer Rime-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, signal-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum (CRC) Error (only for Long Packet(LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invaild
13	Invalid Transmission Length
14	Reserved, set to "0" internally
15	DSI Protocol violation

Figure: Acknowledge with error report for long packet response

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Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Protocol Timer Rime-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, signal-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	set to "0" internally
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invaild
13	Invalid Transmission Length
14	Reserved, set to "0" internally
15	DSI Protocol violation

Figure: Acknowledge with error report for short packet response

These errors are only included on the last packet, which has been received from the MCU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0010b
- Packet Data (PD)
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

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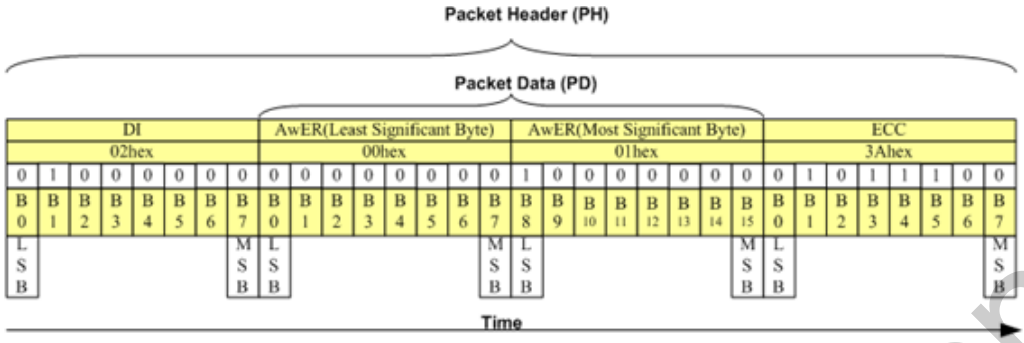

Figure: Acknowledge with error report – example

6.4.5 Customer-defined generic read data type format

The short packet of Data Type 24h (Generic READ, 2 parameters) specifies the register content for read and the Nth parameter that will begin reading. After Data Type 24h is received, BTA is executed. Then, the Nth parameter becomes the first data, and the number of data of WC (word count) value is output.

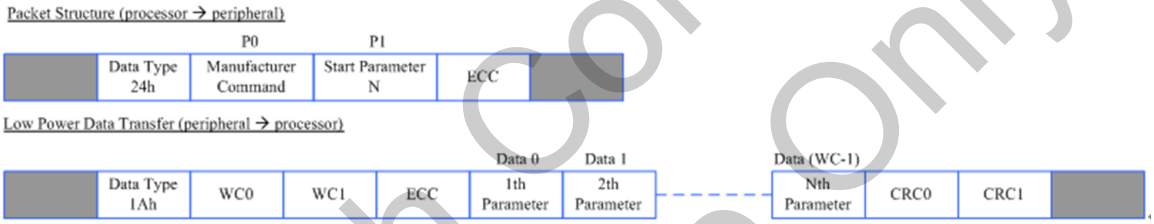

Figure: Generic read data type format

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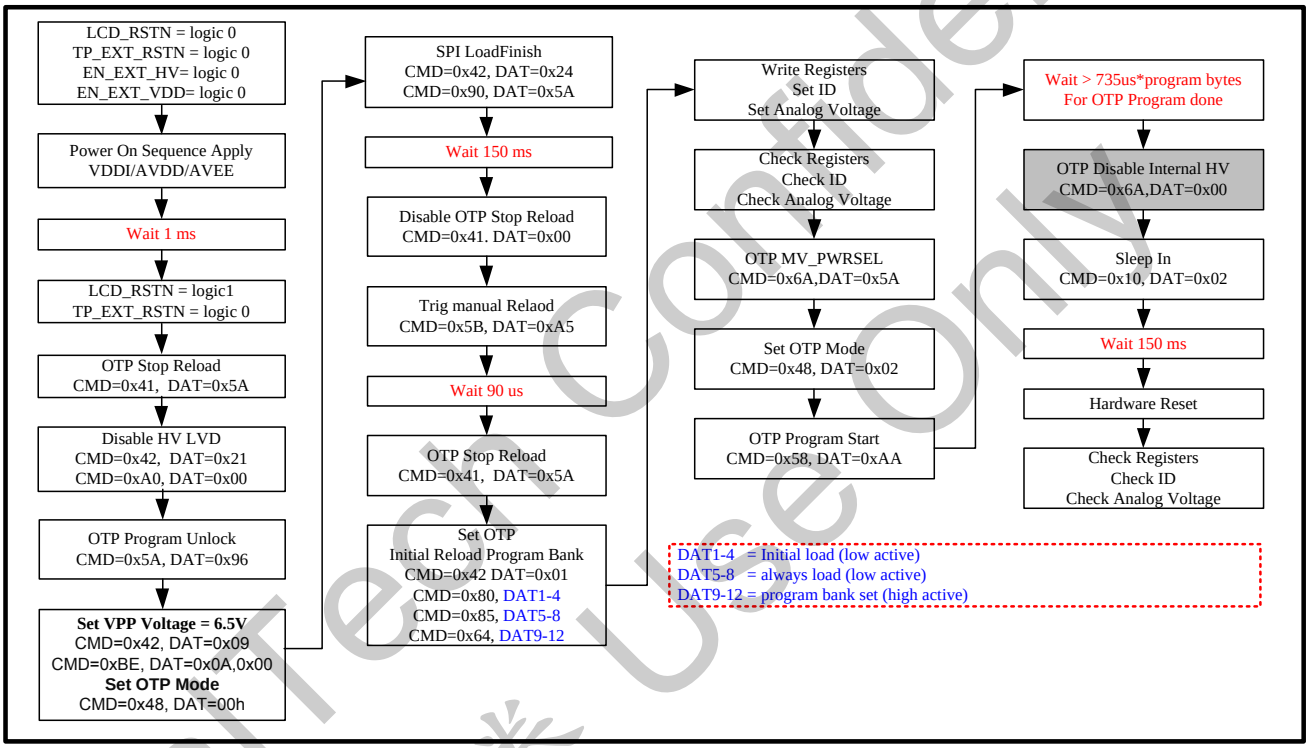
6.5 NVM Programming Procedure

6.5.1 NVM program flow chart with internal Power

1. TCON registers must include correct panel timing configurations to program NVM on panel.
2. TP_EXT_RSTN has to keep low during NVM program flow.

Here is an example of OTP program ID and VCOM with internal power:



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7 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

(AVDD = 4.5V ~ 6.5V, AVEE = -4.5V ~ -6.5V, VDDI = 1.65V ~ 1.95V, Ta = -30°C ~ 85°C)

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage 1	VDDI-VSS	-0.3 ~ +1.95	V	
Power Supply Voltage 2	VDD-VSS	-0.3 ~ +1.35	V	
Power Supply Voltage 3	AVDD-VSS	-0.3 ~ +6.5	V	
Power Supply Voltage 4	VSS-AVEE	-0.3 ~ +6.5	V	
Power Supply Voltage 5	VGH-VGL	-0.3 ~ +32	V	
Input Voltage	Vt	-0.3 ~ VDDI+0.3	V	
Operating Temperature	Topr	-30 ~ +85	°C	
Storage Temperature	Tstg	-55 ~ +110	°C	

Note1. The maximum applicable voltage on any pin with respect to 0V.

Note2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

7.2 DC Characteristics

7.2.1 Basic DC characteristic

(AVDD = 4.5V~6.5V,AVEE = -4.5V~-6.5V,VDDI = 1.65V~1.95V, Ta = -30°C ~ 85°C)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	AVDD	Operating Voltage	4.5	5.5	6.5	V	
Analog Operating voltage	AVEE	Operating Voltage	-6.5	-5.5	-4.5	V	
Logic Operating voltage	VDDI	I/O supply voltage	1.65	1.8	1.95	V	
Digital Operating voltage	VDD	Digital supply voltage	1.08	1.3	1.35	V	
MIPI Interface Operating voltage	LVDSVDD	MIPI supply voltage	1.08	1.3	1.35	V	
Touch Operating voltage	VDD_TP	Touch supply voltage	1.08	1.3	1.35	V	
Input / Output							
Logic High level input voltage	VIH	-	0.7VDDI	-	VDDI	V	
Logic Low level input voltage	VIL	-	VSS	-	0.3VDDI	V	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8VDDI	-	VDDI	V	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSS	-	0.2VDDI	V	
Logic High level input current	IIH	Vin = VDDI	-	-	1	uA	
Logic Low level input current	IIL	Vin = VDDI	-1	-	-	uA	
VCOM Operation							
VCOMDC output voltage	VCOM	AVDD=AVEE=+/-5V	-3.85	-	0.3	V	
Source Driver							
Gamma positive reference voltage	VGMP	VGMP<AVDD-0.2V	3.75	-	6.3	V	
Gamma negative reference voltage	VGMN	VGMN>AVEE-0.2V	-6.3	-	-3.75	V	
Source output voltage	VSD	-	VGMN	-	VGMP	-	
Output deviation voltage (Source positive output channel)	V,dev	Sout >=+4.2V, Sout<=+0.8V	-	-	30	mV	
		+4.2V>Sout>+0.8V	-	-	15	mV	

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Output deviation voltage (Source negative output channel)	V,dev	Sout <=-4.2V, Sout>=-0.8V	-	-	30	mV	
		-4.2V<Sout<-0.8V	-	-	15	mV	
Output offset voltage	V_{OFSET}	-	-	-	100	mv	
Reference Voltage							
Internal reference voltage	VREF_TP	-	3	3.5	4.4	V	
Internal reference voltage	VREF_ST	-	1	2	3	V	
Booster operation							
Pump output voltage	VGH	Range=(AVDD-AVEE) ~(2AVDD-2AVEE)	6.3	-	22.0	V	
Pump output voltage	VGL	Range=(AVEE-AVDD) ~(2AVEE-AVDD)	-18.0	-	-5.3	V	
Regulator output voltage	VCL	-	-5	-4	-3.5	V	

Note1. The maximum applicable voltage on any pin with respect to 0V.

Note2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

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7.2.2 MIPI D-PHY DC character

DC characteristics for MIPI-DSI

DC characteristics for MIPI-DSI

(AVDD = 5.0V~6.5V,AVEE = -5.0V~-6.5V,VDDI = 1.65V~1.95V, Ta = -30℃ ~ 85℃)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	LVDSVDD	-	1.08	1.3	1.35	V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	VGNDSH	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	-	-	550	mV
Logic 1 input threshold (D-PHY spec)	VIH	-	880	-		mV
Logic 1 input threshold (C-PHY spec)	VIH	-	740	-		mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV
Output high level (D-PHY spec)	VOH	-	1.1	1.2	1.3	V
Output high level (C-PHY spec)	VOH	-	0.95	1.2	1.3	V
Logic 0 contention threshold	VILCD,MAX	-	-	-	200	mV
Logic 1 contention threshold	VIHCD,MIN	-	450	-	-	mV
Output impedence of LPDT	ZOLP	-	110	-	-	Ω
Hi-speed Input/Output Characteristics (D-PHY)						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Single-end threshold for HS termination enable	VTERM-EN	-	-	-	450	mV
Differential input low threshold	VIDTL	-	-70	-	-	mV
Differential input high threshold	VIDTH	-	-	-	70	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Differential input impedence	ZID	-	80	100	125	Ω
Hi-speed Input/Output Characteristics (C-PHY)						
Common-Point voltage HS receive mode	VCPRX(DC)	-	95	-	390	mV
Differential input impedance	Z_{ID_AB} Z_{ID_BC} Z_{ID_CA}	-	80	100	120	Ω
Common-point interference beyond 450 MHz	$\Delta V_{CPRX(HF)}$	-	-	-	50	mV
Common-point interference 50MHz – 450MHz	$\Delta V_{CPRX(LF)}$	-	-25	-	25	mV
Differential input high threshold	V_{IDTH}	-	-	-	40	mV
Differential input low threshold	V_{IDTL}	-	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	-	535	mV
Single-ended input low voltage	V_{ILHS}		-40	-	-	mV
Single-ended threshold for HS termination enable	$V_{TERM-EN}$				450	mV
Common-point termination	C_{CP}				90	pF

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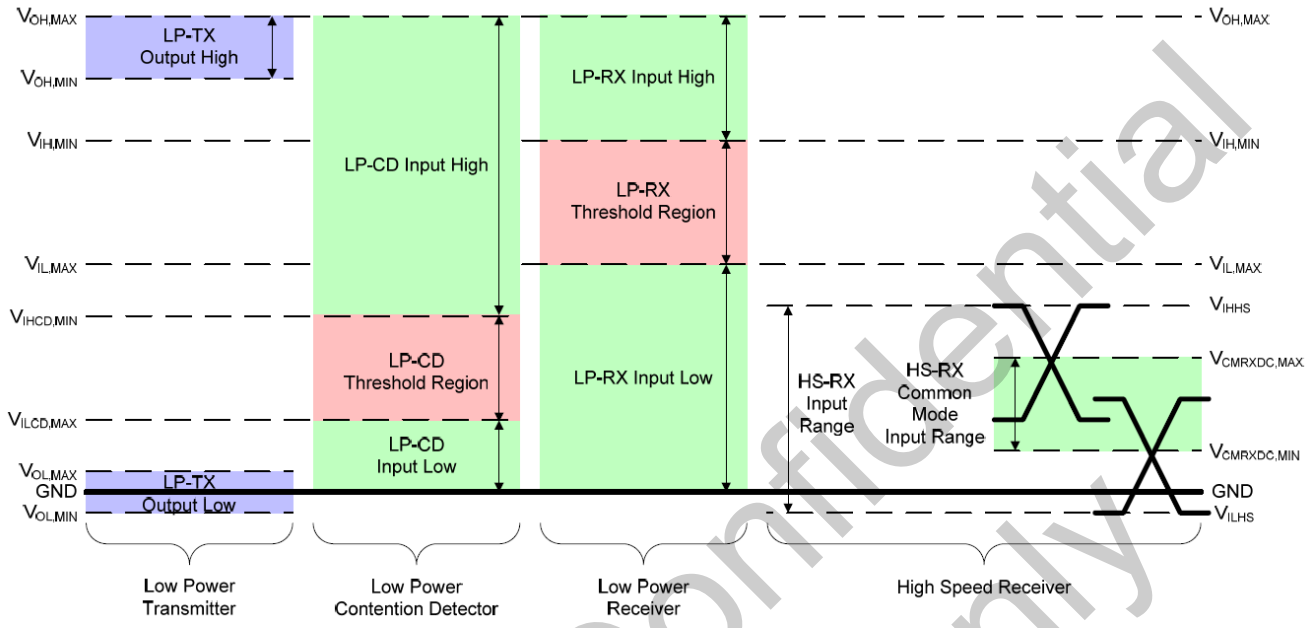

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7.2.3 MIPI C-PHY DC characteristics

C-PHY DC characteristics for MIPI-DSI

(Ta = -30ºC ~ 85ºC)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	LVDSVDD	-	1.08	1.3	1.35	V
Low Power Mode input Characteristics						
Pad signal voltage range	V_I	-	-50	-	1350	mV
Ground Shift	V_{GNDSH}	-	-50	-	50	mV
Logic 0 input threshold	V_{IL}	-	-	-	550	mV
Logic 1 input threshold	V_{IH}	-	740	-	-	mV
Input hysteresis	V_{HYST}	-	25	-	-	mV
LPDT Output Characteristics						
Output high level	V_{OH}	-	0.95	1.25	1.3	V
Output low level	V_{OL}	-	-50	-	50	mV
Logic 0 contention threshold	V_{ILCD}	-	0	-	200	mV
Logic 1 contention threshold	V_{IHCD}	-	450	-	LVDSVDD	mV
High-Speed Input/Output Characteristics						
Single-end input low voltage	V_{ILHS}	-	-40	-	-	mV
Single-end input high voltage	V_{IHHS}	-	-	-	535	mV
Single-end threshold for HS termination ebable	$V_{TERM-EN}$	-	-	-	450	mV
Common mode voltage	V_{CMRXDC}	-	95	250	390	mV
Differential input low threshold	V_{IDTL}	-	-70	-	-	mV
Differential input high threshold	V_{IDTH}	-	-	-	70	mV
Hi-speed transmit voltage	V_{OD}	-	140	200	250	mV
Differential input impedence	Z_{ID-AB} Z_{ID-BC} Z_{ID-CA}	-	80	100	120	ohm
Differential input impedence mismatch	$\triangle Z_{ID}$	Note1			10	%

Note1: $\triangle Z_{ID} = 3 * [max(Z_{ID-AB}, Z_{ID-BC}, Z_{ID-CA}) - min(Z_{ID-AB}, Z_{ID-BC}, Z_{ID-CA})] / (Z_{ID-AB} + Z_{ID-BC} + Z_{ID-CA})$

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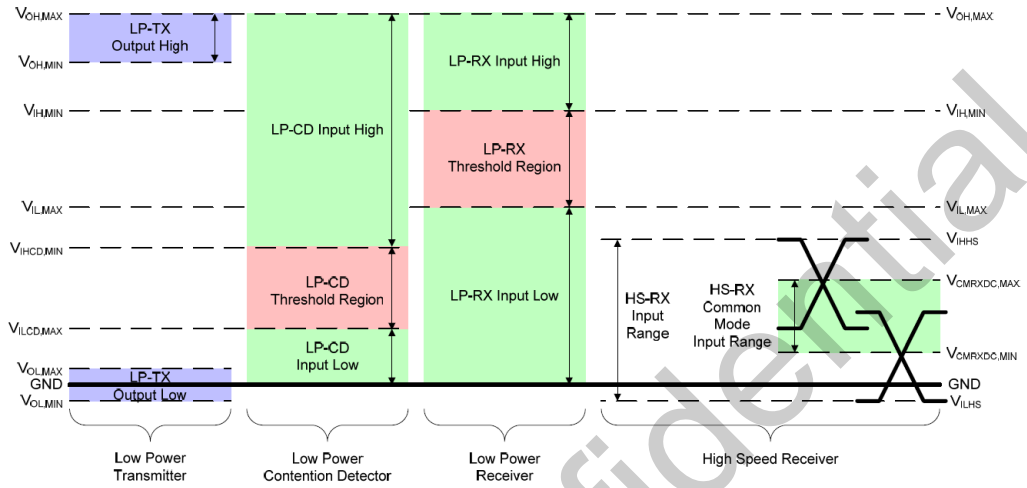

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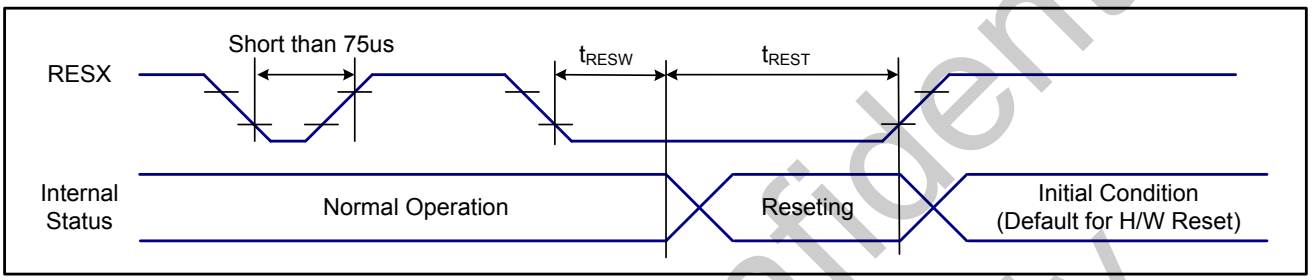
7.3 AC Characteristics

7.3.1 Reset timing characteristics

t_{RESW} shorter than 75us, Reset will be rejected.



VSS=0V, VDDI = 1.65V ~ 1.95V, Ta = -30ºC to 85ºC

Symbol	Parameter	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse minimum width	150	-	-	Reset signal recognized	us
t_{REST}	*2) Reset complete time	5	-	120	Reset action complete	ms

Table: Reset input timing

Note 1. RESX low pulse that is too short does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 75us	Reset Rejected
Longer than 150us	Reset Recognized
Between 75us and 150us	Reset sequence starts (It depends on voltage and temperature condition.)

Note 2. Once Reset low pulse is recognized, system requires RESX remaining low for another 5ms to complete H/W reset.

Note 3. During H/W Reset flow, ID0 ~ ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when H/W reset is complete ; The H/W reset sequence is complete when RESX is remaining low longer than tRESW + tREST.

Note 4. It is necessary to wait 15msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

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7.3.2 I²C interface characteristics

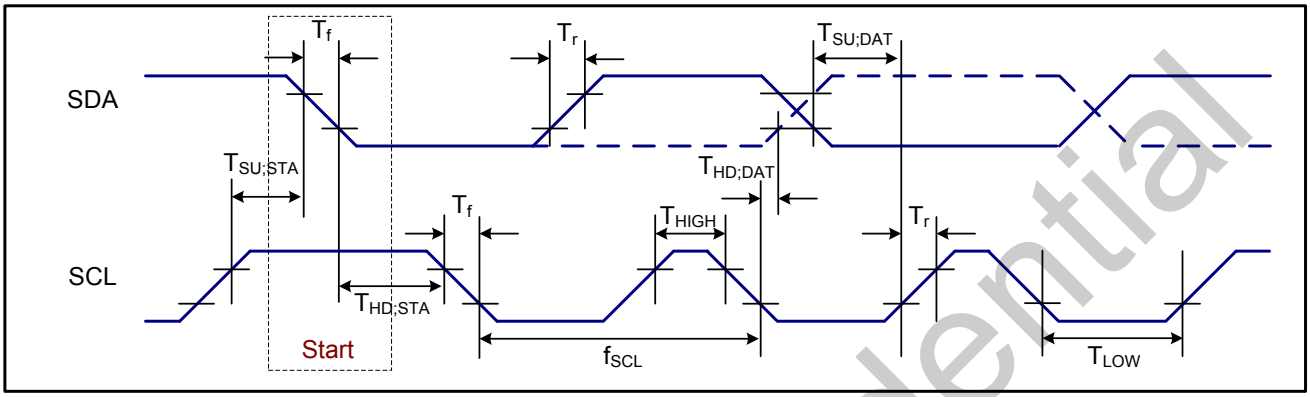

Table: I2C Interface Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCLK}	SCL clock frequency	-	10	-	400	kHz
T_{LOW}	SCL clock LOW period	-	1.2	-	-	us
T_{HIGH}	SCL clock HIGH period	-	0.6	-	-	us
$T_{SU;DATA}$	data set-up time	-	250	-	-	ns
$T_{HD;DATA}$	data hold time	-	0	-	0.9	us
T_r	SCL and SDA rise time	Note 2	$20+0.1C_b$	-	300	ns
T_f	SCL and SDA fall time	Note 2	$20+0.1C_b$	-	300	ns
T_f	SDA fall time for read out	-	$20+0.1C_b$	-	1000	ns
C_b	Capacitive load represented by each bus line	-	-	-	400	pF
$T_{SU;STA}$	Setup time for a repeated START condition	-	0.6	-	-	us
$T_{HD;STA}$	START condition hold time	-	0.6	-	-	us
$T_{SU;STO}$	Setup time for STOP condition	-	0.6	-	-	us
T_{SW}	Tolerable spike width on bus	Note 1	-	-	50	ns
T_{BUF}	BUS free time between a STOP and START condition	-	4.7	-	-	us

Note1: The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width $<t_{SW(max)}$.

Note2: The rise and fall times specified here refer to the driver device and are part of the general fast I²C-bus specification. C_b = capacitive load per bus line.

Note3: All timing values are valid within the operating supply voltage and ambient temperature ranges and are referenced to V_{IL} and V_{IH} with an input voltage swing of VSS to VDDI

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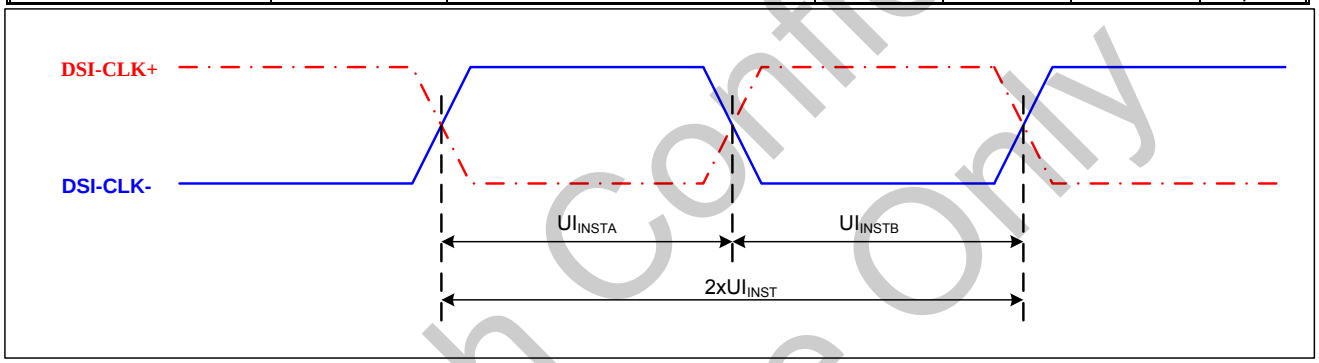
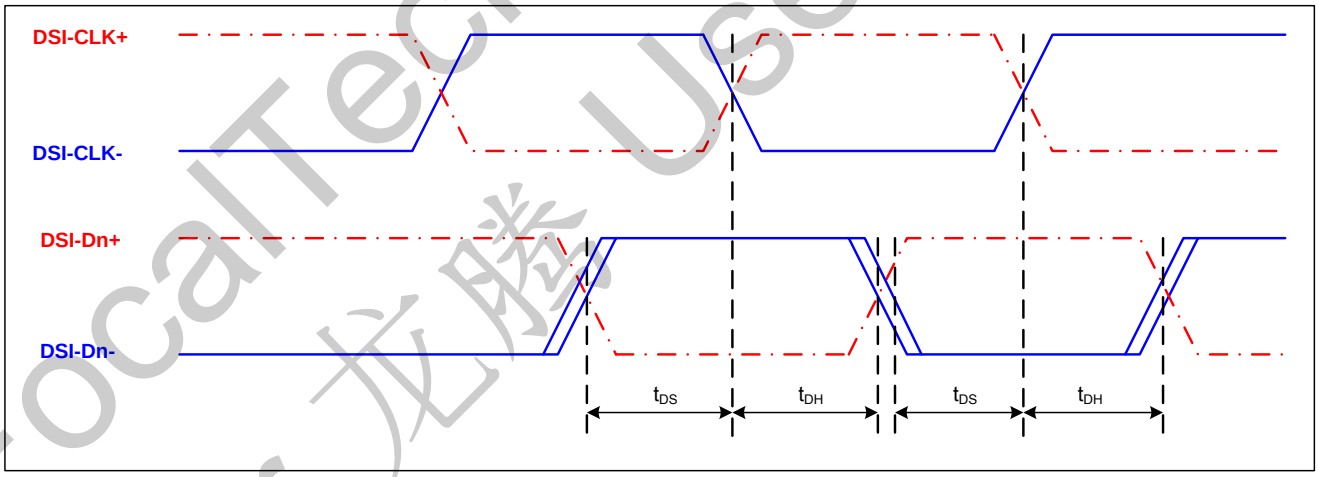
7.3.3 MIPI D-PHY AC characteristics

7.3.3.1 High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	1.54	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	0.77	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps





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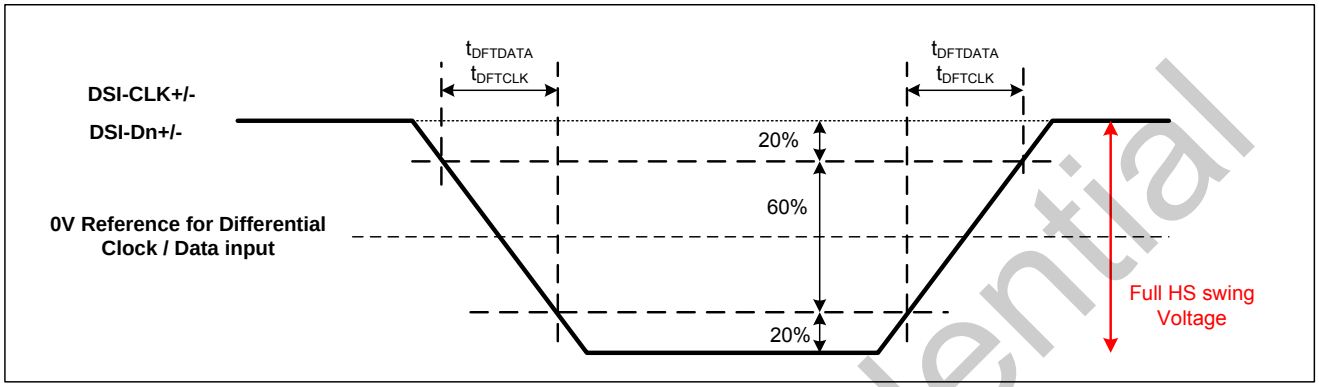

Figure: AC characteristics for MIPI-DSI High speed mode

7.3.3.2 Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2XT_{LPXD}$	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5XT_{LPXD}$	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4XT_{LPXD}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	-

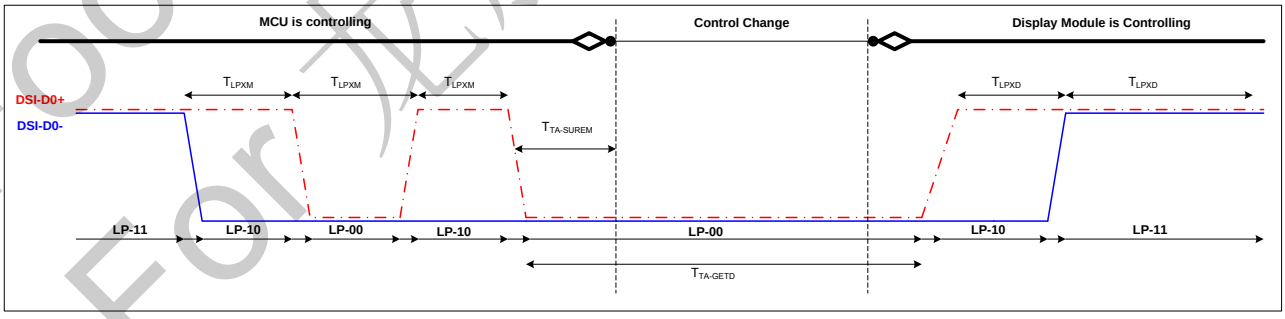

Figure: BTA from the MCU to the Display Module

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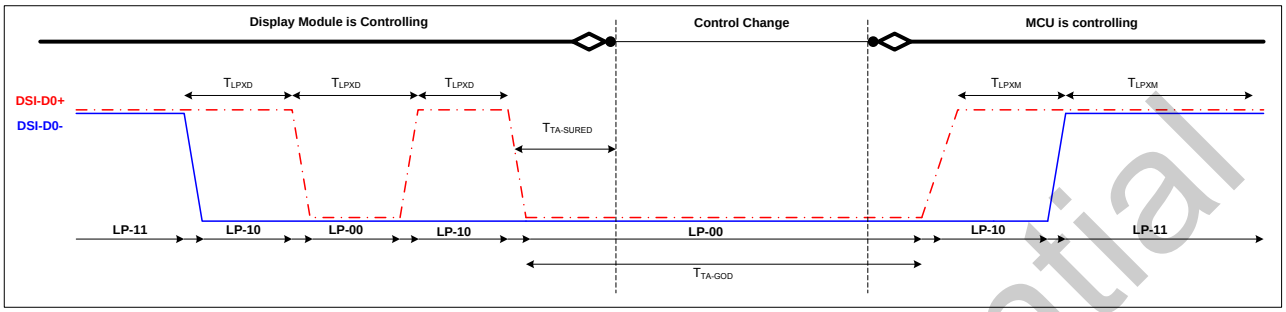

Figure: BTA from the Display Module to the MCU

7.3.3.3 Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

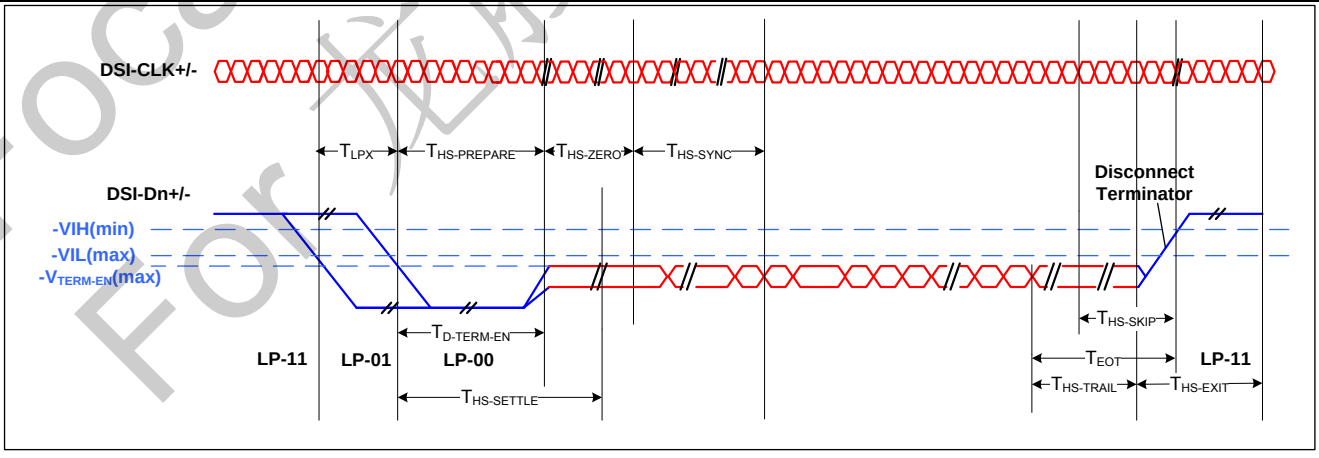

Figure: High Speed Data Transmission Bursts

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Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

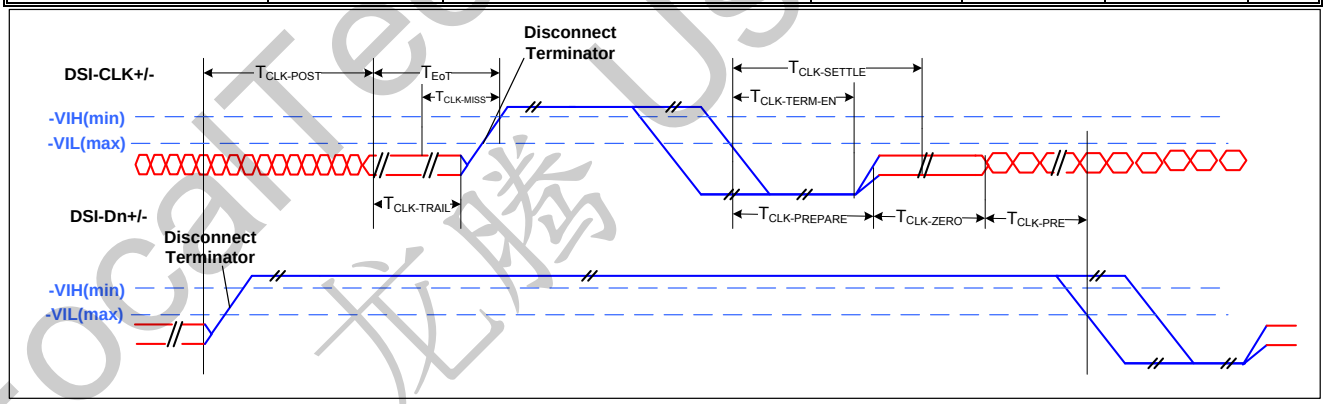

Figure: Switching the clock Lane between clock Transmission and Low Power Mode

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7.3.3.4 LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when 4 different combinations, what are listed below, are possible:

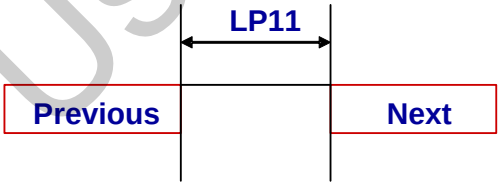
1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100 ns	-	100 ns	-	100 ns	-
HSDT	60ns + 52UI	-	60ns + 52UI	-	60ns + 52UI	-
BTA	100 ns	-	100 ns	-	100 ns	-



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7.3.4 MIPI C-PHY AC characteristics

7.3.4.1 C-PHY HS Mode

Symbol	Description	Notes	Specification			Unit
			MIN	TYP	MAX	
$t_{UI-AVERAGE}$	UI average	1	0.833	-	12.5	ns
t_{MID-RX}	Data rate ≦1Gsps	-	$t_{UI-AVERAGE}$ – 1000ps			ps
	Data rate ≧1Gsps	-	0			-
$T_{EYE-RAMP-RX-LR}$	Eye ramp time at th reference channel output	-	-	-	250	ps
$T_{EYE-WIDTH-RX-LR}$	Eye width at th reference channel output	-	-	-	500+t_{MID-RX}	ps

Note:

1. Date rate range: 80Msps ~ 1.2Gsps.

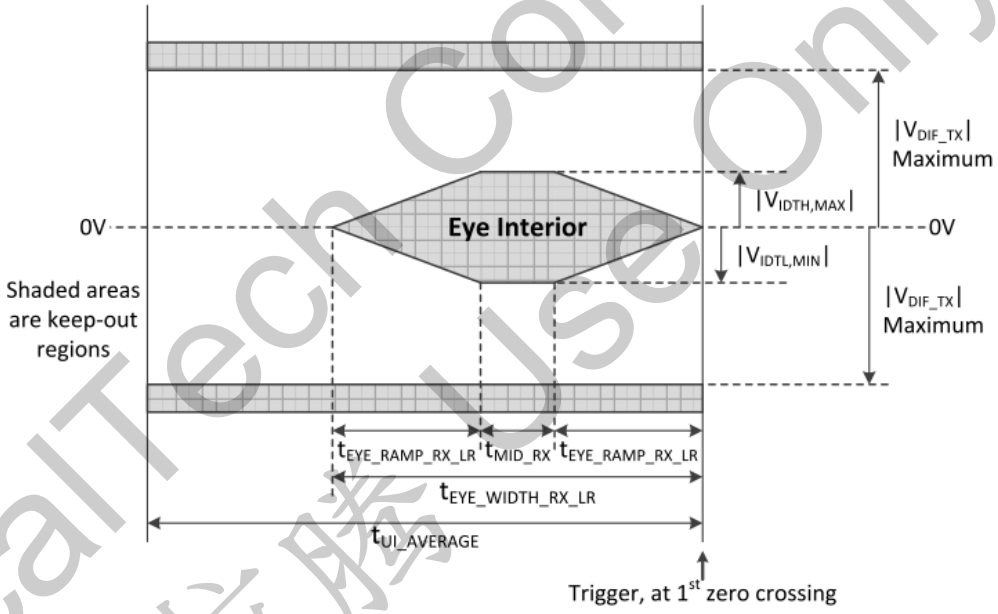

Figure: HS DATA Eye diagram at receiver

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7.3.4.1 C-PHY LP Mode

Symbol	Description	Notes	Specification			Unit
			MIN	TYP	MAX	
T_{LPX-M}	Transmitted length of any Low-Power state period (MCU)	-	50	-	-	ns
$T_{TA-SURE-M}$	The display module waits after the LP-10 before transmitting the LP-00 (MCU)	-	T_{LPX-M}	-	$2*T_{LPX-M}$	ns
$T_{TA-GO-M}$	The display module drives the LP-00 before releasing MCU control	-	$4*T_{LPX-M}$			ns
$T_{TA-GET-M}$	The display drives the LP-00 after accepting control	-	$5*T_{LPX-M}$			ns
Ratio T_{LPX}	Ratio of (T_{LPX-M}/T_{LPX-D}) for driving overlap	-	2/3	-	3/2	
T_{LPX-D}	Transmitted length of any Low-Power state period (Display)	-	58	-	-	ns
$T_{TA-SURE-D}$	The MCU waits after the LP-10 before transmitting the LP-00 (Display)	-	T_{LPX-D}	-	$2*T_{LPX-D}$	ns
$T_{TA-GO-D}$	The MCU drives the LP-00 before releasing Display control	-	$4*T_{LPX-D}$			ns
$T_{TA-GET-D}$	The MCU drives the LP-00 after accepting control	-	$5*T_{LPX-D}$			ns

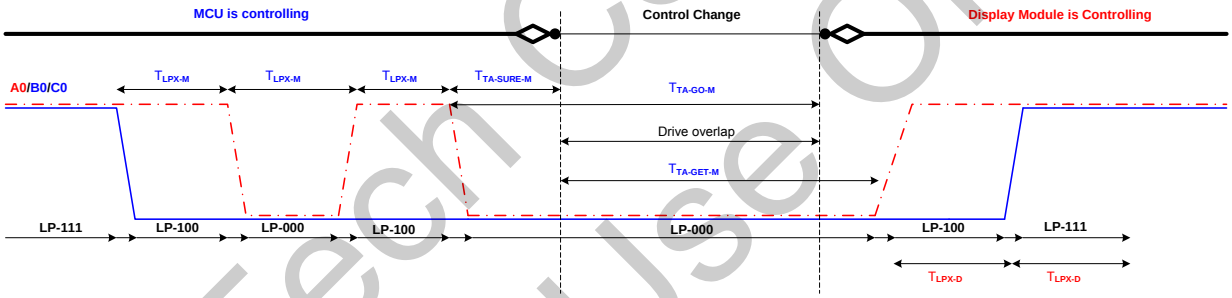

Figure: BTA from the MCU to the Display Module

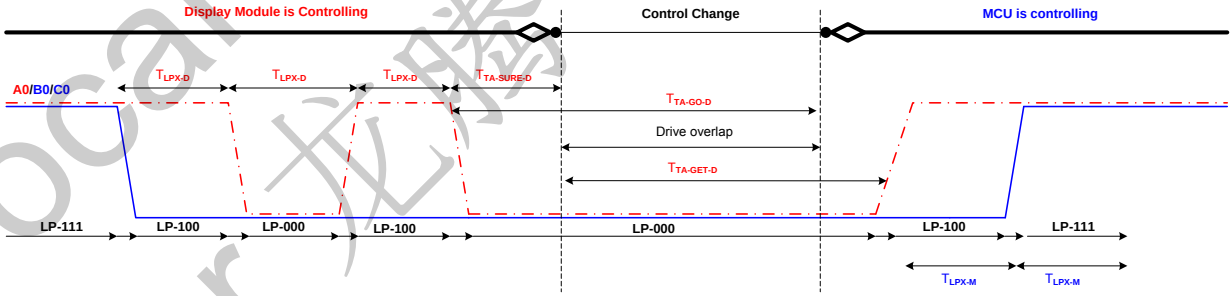

Figure: BTA from the Display Module to the MCU

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7.3.4.2 C-PHY HSDT Bursts

Symbol	Description	Notes	Specification			Unit
			MIN	TYP	MAX	
T_{LPX}	Length of any LP state period	2	50	-	-	ns
$T_{3\text{-TERM-EN}}$	Time for the receiver to enable the HS line termination, starting from the time point when the A,B,C wrie cross $V_{IL\text{-MAX}}$	1,3	-	-	38	ns
$T_{3\text{-PREPARE}}$	Time that the transmitter drives the 3-wire LP-000 Line state immediately before the start of the HS Transmission	2	38		95	ns
$T_{3\text{-SETTLE}}$	Time interval during whith the HS receiver should ignore any HS transitions on the lane,starting from the beginning of $T_{3\text{-PREPARE}}$	3,4	$T_{3\text{-PREPARE}}$ +6UI	-	$T_{3\text{-PREPARE}}$ +$T_{3\text{-PREBEGIN}}$	ns
$T_{3\text{-PREBEGIN}}$	The length of the first part of the preamble	2,5	7	-	448	UI
$T_{3\text{-PROGSEQ}}$	The length of the programmable sequence section of the Preamble	2	0 or 14			UI
$T_{3\text{-PREEND}}$	The length of the end of the preamble	2	7			UI
$T_{3\text{-PREAMBLE}}$	The length of the entire preamble including $T_{3\text{-PREBEGIN}}$, $T_{3\text{-PROGSEQ}}$ and $T_{3\text{-PREEND}}$	2	$T_{3\text{-PREBEGIN}}$ + $T_{3\text{-PROGSEQ}}$ + $T_{3\text{-PREEND}}$			UI
$T_{3\text{-sync}}$	The length of the Sync Word	2	7			UI
$T_{3\text{-POST}}$	The length of the post-sequence at the end of the Burst	2,6	7	-	224	UI
$T_{HS\text{-EXIT}}$	Time that the transmitter drives LP-111 following a HS burst	2	100	-	-	ns

Note:

1. The receiver termination impedances shall not be enabled until the single-ended voltages on all of A,B and C fall below V_{TERM_EN}
2. Transmitter-specific parameter.
3. Receiver-specific parameter.
4. $T_{3\text{-SETTLE}}$ should end before the end of $T_{3\text{-PREBEGIN}}$ so the receiver's internal clock can run for a sufficient time to be able to initialize the PHY and protocol circuitry in the receiver.
5. $T_{3\text{-PREBEGIN}}$ should be adjustable at the transmitter from 7UI to 448UI in increments of 7UI.
6. $T_{3\text{-POST}}$ should adjustable at the transmitter from 7UI to 224UI in increments of 7UI.

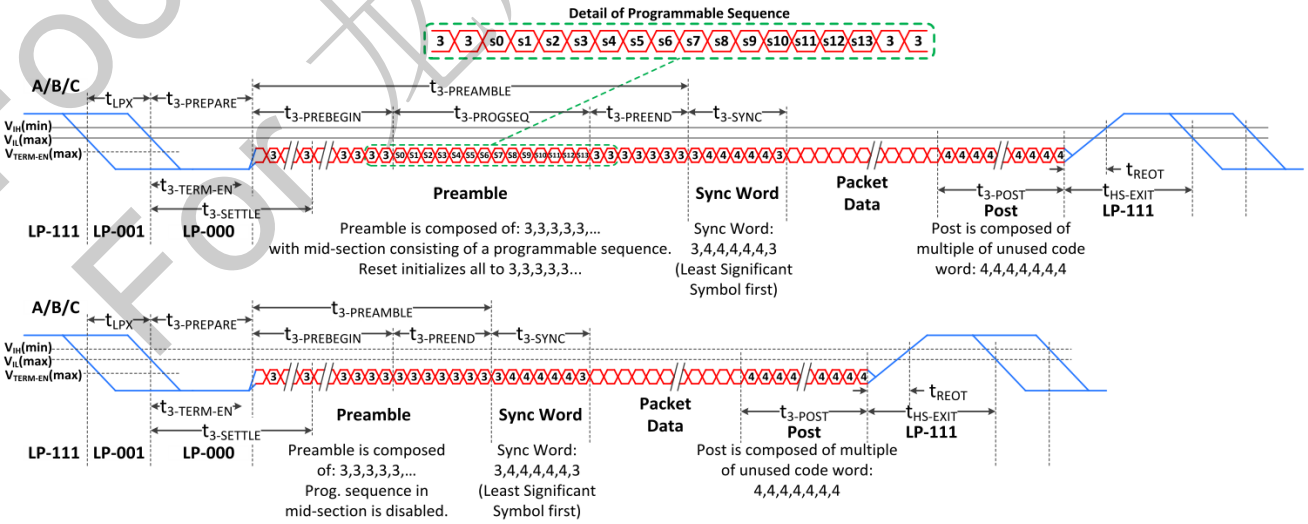

Figure: High Speed Data Transmission in Bursts

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7.3.4.3 CPHY: LP-111 between High Speed and Low Power Modes

High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-111) when 4 different combinations, what are listed below, are possible:

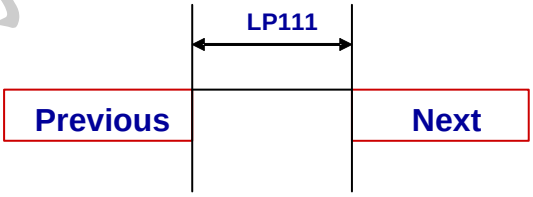
1. High Speed Mode => Stop State (SS, LP-111) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-111) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-111) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-111) => Low Power Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-111) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100 ns	-	400ns + 8UI	-	100 ns	-
HSDT	170ns + 52UI	-	520ns + 60UI	-	170ns + 52UI	-
BTA	100 ns	-	400ns + 8UI	-	100 ns	-



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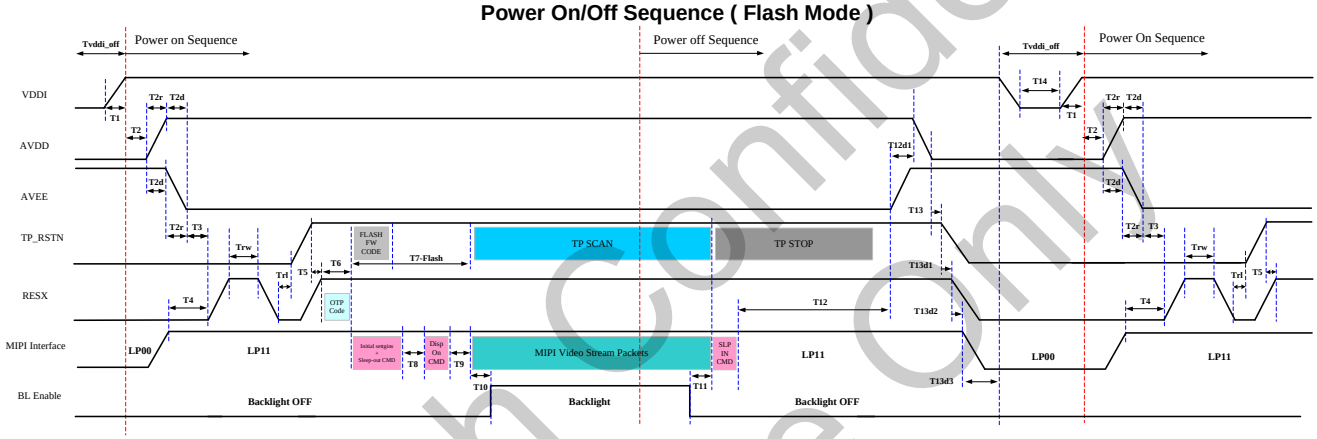
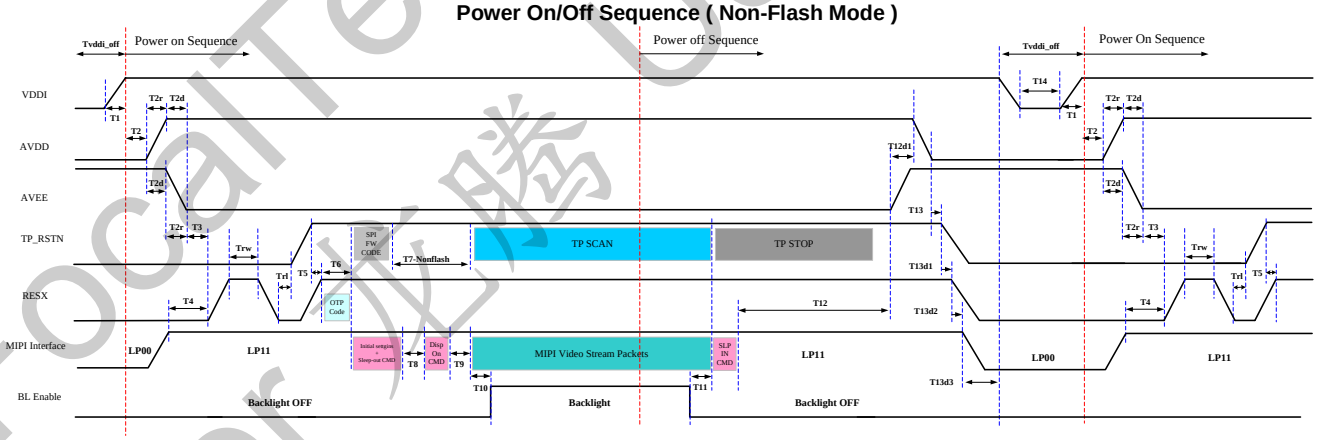
7.3.5 Power On/Off Sequence

1. There will be no hard-damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off sequences.
3. There will be no abnormal visible effects on the display between end of Power On sequence and before receiving Sleep-Out command. Also between receiving Sleep-In command and Power Off sequence.
4. RESX and TP_RSTN must be held stablely by host during Power On Sequence, otherwise function is not guaranteed.
5. During Abnormal power dropping, VDDI can start power down 3ms after AVDD/AVEE power down.
6. BL Enable timing is for reference only and not restricted (T10/T11).
7. 2nd reset timing is requested for RESX assertion and is optional for TP_RSTN assertion.
8. All input signals should be kept GND, floating or LP00 status during Tvddi_off.

Power On/Off Sequence (Flash Mode)



Power On/Off Sequence (Non-Flash Mode)



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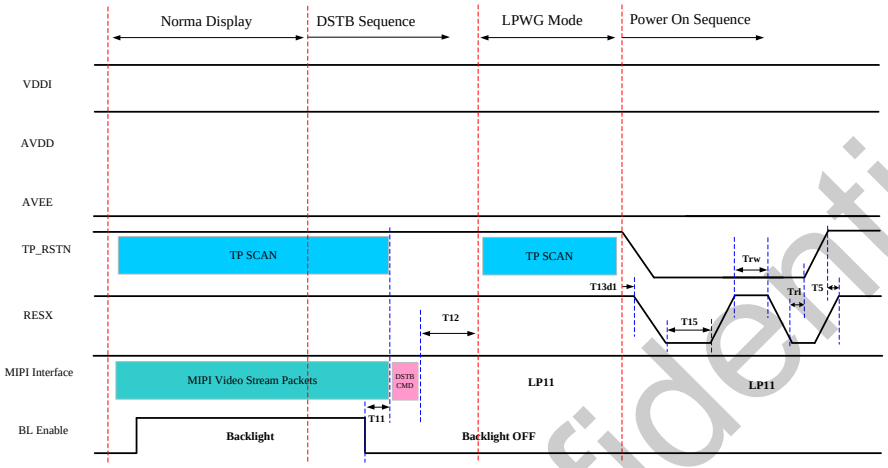
TP Gesture Mode Exit Sequence



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FT8206 Power On / Off Sequence Timing					
Parameter	Description	Min	Typ	Max	ms
T1	Rise time from 0.1*VDDI to 0.9*VDDI	0		5	ms
T2	AVDD power up after VDDI power on	3			ms
T2d	AVEE power up after AVDD power up	0			ms
T2r	Rise time from 0.1*AVDD to 0.9*AVDD Rise time from 0.1*AVEE to 0.9*AVEE	0.1		5	ms
T3	RESX reset release time after AVDD/AVEE power on	5			ms
T4	MIPI signals start (Hi-Z/GND to LP11) to RESX rising edge	0			ms
T5	TP Reset release to LCD Reset release	0			ms
T6	FLASH/OTP Settings download finished after RESX released MIPI may start to send Initial Settings + Sleep-out CMD SPI/Flash may start to send FW code			35	ms
T7-Nonflash	SPI FW Code download finish to TP SCAN Start (Non-flash mode)			200	ms
T7-Flash	Flash FW Code download start to TP SCAN Start (Flash mode)			280	ms
T8	Sleep-out CMD to Display-On CMD		120		ms
T9	Display-On CMD to MIPI Video Stream On time	10			ms
T10	MIPI Video Stream On time to Backlight On time	100			ms
T11	Backlight Off time to MIPI Video Stream Off time	100			ms
T12	AVEE power down after Sleep-In CMD	150			ms
T12d1	AVDD power down after AVEE power down	0			ms
T13	TP_RSTN falling edge after AVDD power down	0			ms
T13d1	In Power Off Sequence, TP_RSTN falling edge to RESX falling edge	0			ms
T13d2	In Power Off Sequence, RESX falling edge to MIPI interface power down	0			ms
T13d3	In Power Off Sequence, MIPI Interface power down to VDDI power down	3			ms
T14	VDDI rise again after VDDI power down (0.1*VDDI)	50			ms
T15	RESX falling edge (Exit from DSTB Mode) to RESX rising edge	5		120	ms
Trl	2nd RESX reset low width to TP_RSTN rising	5			ms
Trw	RESX high level width before 2nd RESX reset	5		10	ms

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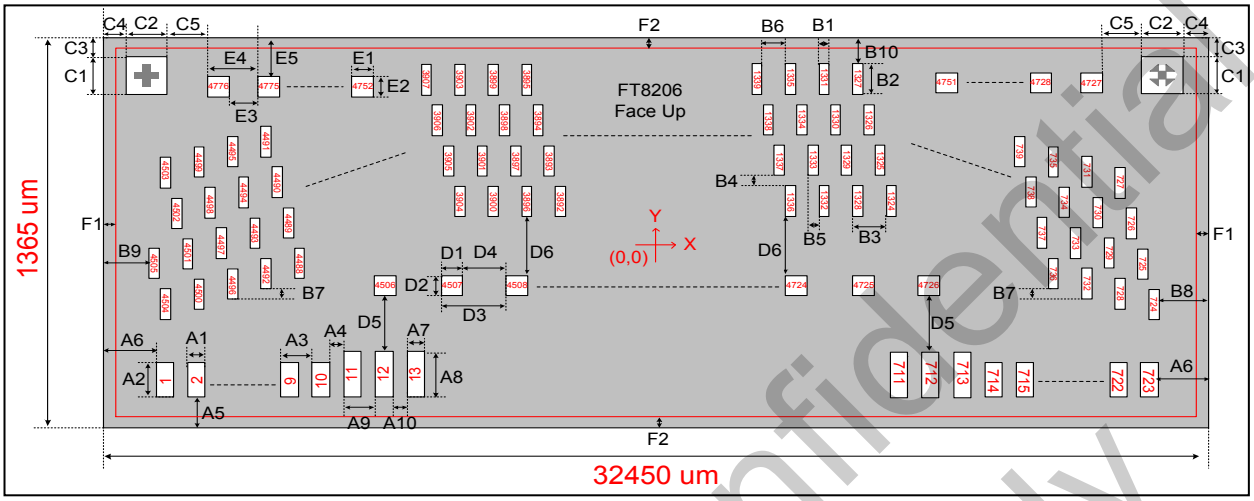
8 CHIP INFORMATION

8.1 PAD Assignment



Symbol	Size	Symbol	Size	Symbol	Size	Symbol	Size	Symbol	Size	Symbol	Size
A1	20	B1	13	C1	115	D1	40	E1	35	F1	30
A2	80	B2	80	C2	115	D2	40	E2	35	F2	30
A3	44	B3	34	C3	175	D3	100	E3	65		
A4	24	B4	28	C4	67.5	D4	60	E4	100		
A5	87.5	B5	8.5	C5	217.5	D5	287	E5	205		
A6	331	B6	21			D6	285				
A7	20	B7	2.8								
A8	115	B8	149.5								
A9	44	B9	149								
A10	24	B10	146.5							um	

Note : Chip Size and Bump space including scribe line

8.2 PAD Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip Size	--	32450	1365	um
Chip Thickness	--	170		
Pad Pitch	1~723	44	--	
	724~4505	34	--	
	DUMMY	100	--	
Pad Size	DUMMY	35	35	
	1~723	20	115	
	724~4505	13	80	

Note1: Chip size included scribe line

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8.3 PAD Locations

No.	PAD Name	X	Y
1	CGOUT_L[24]	-15884	-555
2	CGOUT_L[23]	-15840	-555
3	CGOUT_L[22]	-15796	-555
4	CGOUT_L[21]	-15752	-555
5	CGOUT_L[20]	-15708	-555
6	CGOUT_L[19]	-15664	-555
7	CGOUT_L[18]	-15620	-555
8	CGOUT_L[17]	-15576	-555
9	CGOUT_L[16]	-15532	-555
10	CGOUT_L[15]	-15488	-555
11	CGOUT_L[14]	-15444	-537.5
12	CGOUT_L[13]	-15400	-537.5
13	CGOUT_L[12]	-15356	-537.5
14	CGOUT_L[11]	-15312	-537.5
15	CGOUT_L[10]	-15268	-537.5
16	CGOUT_L[9]	-15224	-537.5
17	CGOUT_L[8]	-15180	-537.5
18	CGOUT_L[7]	-15136	-537.5
19	CGOUT_L[6]	-15092	-537.5
20	CGOUT_L[5]	-15048	-537.5
21	CGOUT_L[4]	-15004	-537.5
22	CGOUT_L[3]	-14960	-537.5
23	CGOUT_L[2]	-14916	-537.5
24	CGOUT_L[1]	-14872	-537.5
25	VGHO_L	-14828	-537.5
26	VGHO_L	-14784	-537.5
27	VGHO_L	-14740	-537.5
28	VGH1_L	-14696	-537.5
29	VGH1_L	-14652	-537.5
30	VGH1_L	-14608	-537.5
31	VGH2_L	-14564	-537.5
32	VGH2_L	-14520	-537.5
33	VGLO_L	-14476	-537.5
34	VGLO_L	-14432	-537.5
35	AVDD	-14388	-537.5
36	AVDD	-14344	-537.5
37	AVDD	-14300	-537.5
38	AVDD	-14256	-537.5
39	AVDD	-14212	-537.5
40	AVSS	-14168	-537.5
41	AVSS	-14124	-537.5
42	AVSS	-14080	-537.5
43	AVSS	-14036	-537.5
44	AVSS	-13992	-537.5
45	AVEE	-13948	-537.5
46	AVEE	-13904	-537.5
47	AVEE	-13860	-537.5
48	AVEE	-13816	-537.5
49	AVEE	-13772	-537.5
50	VGH_L	-13728	-537.5
51	VGH_L	-13684	-537.5
52	VGH_L	-13640	-537.5
53	VGH_L	-13596	-537.5
54	VGH_L	-13552	-537.5
55	C21P	-13508	-537.5
56	C21P	-13464	-537.5
57	C21P	-13420	-537.5
58	C21P	-13376	-537.5
59	C21P	-13332	-537.5
60	C21N	-13288	-537.5
61	C21N	-13244	-537.5
62	C21N	-13200	-537.5
63	C21N	-13156	-537.5
64	C21N	-13112	-537.5
65	AVSS	-13068	-537.5
66	AVSS	-13024	-537.5
67	AVSS	-12980	-537.5
68	AVSS	-12936	-537.5
69	AVSS	-12892	-537.5
70	C22P	-12848	-537.5
71	C22P	-12804	-537.5
72	C22P	-12760	-537.5
73	C22P	-12716	-537.5
74	C22P	-12672	-537.5
75	C22N	-12628	-537.5
76	C22N	-12584	-537.5
77	C22N	-12540	-537.5
78	C22N	-12496	-537.5
79	C22N	-12452	-537.5
80	VGL	-12408	-537.5
81	VGL	-12364	-537.5
82	VGL	-12320	-537.5
83	VGL	-12276	-537.5
84	VGL	-12232	-537.5
85	AVDD	-12188	-537.5
86	AVDD	-12144	-537.5
87	AVDD	-12100	-537.5
88	AVDD	-12056	-537.5
89	AVDD	-12012	-537.5
90	AVSS	-11968	-537.5
91	AVSS	-11924	-537.5
92	AVSS	-11880	-537.5
93	AVSS	-11836	-537.5
94	AVSS	-11792	-537.5
95	AVDD	-11748	-537.5
96	AVDD	-11704	-537.5
97	AVDD	-11660	-537.5
98	AVDD	-11616	-537.5
99	AVDD	-11572	-537.5
100	AVDD	-11528	-537.5
101	AVDD	-11484	-537.5
102	AVDD	-11440	-537.5
103	AVDD	-11396	-537.5
104	AVDD	-11352	-537.5
105	AVDD	-11308	-537.5
106	AVDD	-11264	-537.5
107	AVSS	-11220	-537.5
108	AVSS	-11176	-537.5
109	AVSS	-11132	-537.5
110	VSS	-11088	-537.5
111	VSS	-11044	-537.5
112	VSS	-11000	-537.5
113	VSS	-10956	-537.5
114	AVSS	-10912	-537.5
115	AVSS	-10868	-537.5
116	AVSS	-10824	-537.5
117	AVSS	-10780	-537.5
118	VDD_TP	-10736	-537.5
119	VDD_TP	-10692	-537.5
120	VDD_TP	-10648	-537.5
121	VDD_TP	-10604	-537.5
122	VGLOB	-10560	-537.5
123	VGLOB	-10516	-537.5
124	VGLOB	-10472	-537.5
125	VGHOB	-10428	-537.5
126	VGHOB	-10384	-537.5
127	VGHOB	-10340	-537.5
128	TAVDD_L	-10296	-537.5
129	TAVDD_L	-10252	-537.5
130	TAVDD_L	-10208	-537.5
131	TAVDD_L	-10164	-537.5
132	TAVSS_L	-10120	-537.5
133	TAVSS_L	-10076	-537.5
134	TAVSS_L	-10032	-537.5
135	TAVSS_L	-9988	-537.5
136	AFE_TEST_L	-9944	-537.5
137	AFE_TEST_L	-9900	-537.5
138	VCOM_L	-9856	-537.5
139	VCOM_L	-9812	-537.5
140	VCOM_L	-9768	-537.5
141	VCOM_L	-9724	-537.5
142	VCOM_L	-9680	-537.5
143	VCOM_L	-9636	-537.5
144	VCOM_L	-9592	-537.5
145	VCOM_L	-9548	-537.5
146	VCOM_L	-9504	-537.5
147	VCOM_L	-9460	-537.5
148	VREF_ST_L	-9416	-537.5
149	VREF_ST_L	-9372	-537.5
150	VREF_ST_L	-9328	-537.5
151	VREF_TP_L	-9284	-537.5
152	VREF_TP_L	-9240	-537.5
153	VREF_TP_L	-9196	-537.5
154	VDD	-9152	-537.5
155	VDD	-9108	-537.5
156	VDD	-9064	-537.5
157	VDD	-9020	-537.5
158	VDD	-8976	-537.5
159	VDD	-8932	-537.5
160	VDD	-8888	-537.5
161	DCHG2	-8844	-537.5
162	DCHG2	-8800	-537.5
163	DCHG1	-8756	-537.5
164	DCHG1	-8712	-537.5
165	AVEE_DC	-8668	-537.5
166	AVEE_DC	-8624	-537.5
167	AVEE_DC	-8580	-537.5
168	AVEE_DC	-8536	-537.5
169	AVEE_DC	-8492	-537.5
170	AVEE_DC	-8448	-537.5
171	AVSS_DC	-8404	-537.5
172	AVSS_DC	-8360	-537.5
173	AVSS_DC	-8316	-537.5
174	AVSS_DC	-8272	-537.5
175	AVSS_DC	-8228	-537.5
176	AVSS_DC	-8184	-537.5
177	AVSS_DC	-8140	-537.5
178	AVSS_DC	-8096	-537.5
179	AVDD_DC	-8052	-537.5
180	AVDD_DC	-8008	-537.5
181	AVDD_DC	-7964	-537.5
182	AVDD_DC	-7920	-537.5
183	AVDD_DC	-7876	-537.5
184	AVDD_DC	-7832	-537.5
185	AVDD_DC	-7788	-537.5
186	AVDD_DC	-7744	-537.5
187	AVDD_DC	-7700	-537.5
188	GVDDN	-7656	-537.5
189	GVDDN	-7612	-537.5
190	AVSS	-7568	-537.5
191	AVSS	-7524	-537.5
192	GVDDP	-7480	-537.5
193	GVDDP	-7436	-537.5
194	VSS	-7392	-537.5
195	VSS	-7348	-537.5
196	VSS	-7304	-537.5
197	VSS	-7260	-537.5
198	VSS	-7216	-537.5
199	VSS	-7172	-537.5
200	VSS	-7128	-537.5
201	VDD_TP	-7084	-537.5
202	VDD_TP	-7040	-537.5
203	VDD_TP	-6996	-537.5
204	VDD_TP	-6952	-537.5
205	VDD_TP	-6908	-537.5
206	VDD_TP	-6864	-537.5
207	VDD_TP	-6820	-537.5
208	VDD_TP	-6776	-537.5
209	VDDI	-6732	-537.5
210	VDDI	-6688	-537.5
211	VDDI	-6644	-537.5
212	VDDI	-6600	-537.5
213	VDDI	-6556	-537.5
214	VDDI	-6512	-537.5
215	VDDI	-6468	-537.5
216	VDDI	-6424	-537.5

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No.	PAD Name	X	Y
217	CYSTAL_SEL[0]	-6380	-537.5
218	CYSTAL_SEL[1]	-6336	-537.5
219	SYNC_LS_L[0]	-6292	-537.5
220	SYNC_LS_L[1]	-6248	-537.5
221	SYNC_LS_L[2]	-6204	-537.5
222	SYNC_LS_L[3]	-6160	-537.5
223	SYNC_LS_L[4]	-6116	-537.5
224	SYNC_LS_L[5]	-6072	-537.5
225	SYNC_LS_L[6]	-6028	-537.5
226	SYNC_LS_L[7]	-5984	-537.5
227	SYNC_LS_L[8]	-5940	-537.5
228	SYNC_LS_L[9]	-5896	-537.5
229	SYNC_LS_L[10]	-5852	-537.5
230	SYNC_LS_L[11]	-5808	-537.5
231	SYNC_LS_L[12]	-5764	-537.5
232	SYNC_LS_L[13]	-5720	-537.5
233	EN_EXT_VCOM	-5676	-537.5
234	AFE_TEST_L[0]	-5632	-537.5
235	AFE_TEST_L[0]	-5588	-537.5
236	TP_EXT_RSTN	-5544	-537.5
237	TP_EXT_RSTN	-5500	-537.5
238	TP_INT	-5456	-537.5
239	TP_INT	-5412	-537.5
240	TP_I2C_SDA	-5368	-537.5
241	TP_I2C_SDA	-5324	-537.5
242	TP_I2C_SCL	-5280	-537.5
243	TP_I2C_SCL	-5236	-537.5
244	TP_SPI_SS	-5192	-537.5
245	TP_SPI_SS	-5148	-537.5
246	TP_SPI_MISO	-5104	-537.5
247	TP_SPI_MISO	-5060	-537.5
248	TP_SPI_MOSI	-5016	-537.5
249	TP_SPI_MOSI	-4972	-537.5
250	TP_SPI_SCL	-4928	-537.5
251	TP_SPI_SCL	-4884	-537.5
252	TP_BUS_SEL	-4840	-537.5
253	TEST[0]	-4796	-537.5
254	LCD_GPIO[0]	-4752	-537.5
255	TP_WAKE	-4708	-537.5
256	TP_BOOT_DEVICE	-4664	-537.5
257	EN_EXT_HV	-4620	-537.5
258	VSS	-4576	-537.5
259	VSS	-4532	-537.5
260	VDDI	-4488	-537.5
261	VDDI	-4444	-537.5
262	VDDI	-4400	-537.5
263	VDDI	-4356	-537.5
264	VDDI	-4312	-537.5
265	VSS	-4268	-537.5
266	VSS	-4224	-537.5
267	VSS	-4180	-537.5
268	VSS	-4136	-537.5
269	BIST_EN	-4092	-537.5
270	IM	-4048	-537.5
271	EN_EXT_VDD	-4004	-537.5
272	VSS	-3960	-537.5
273	VSS	-3916	-537.5
274	VSS	-3872	-537.5
275	VSS	-3828	-537.5
276	VSS	-3784	-537.5
277	VDDI	-3740	-537.5
278	VDDI	-3696	-537.5
279	DSWAP[0]	-3652	-537.5
280	DSWAP[1]	-3608	-537.5
281	PNSWAP	-3564	-537.5
282	LED_PWM	-3520	-537.5
283	RESX	-3476	-537.5
284	TP_GPIO[0]	-3432	-537.5
285	TP_GPIO[1]	-3388	-537.5
286	POR12	-3344	-537.5
287	POR18	-3300	-537.5
288	LANSEL[0]	-3256	-537.5
289	LANSEL[1]	-3212	-537.5
290	SYNC_HS[0]	-3168	-537.5

No.	PAD Name	X	Y
291	LCD_EXT_OSC	-3124	-537.5
292	TEST[1]	-3080	-537.5
293	TEST[2]	-3036	-537.5
294	SYNC_HS[1]	-2992	-537.5
295	SYNC_HS[1]	-2948	-537.5
296	SYNC_HS[2]	-2904	-537.5
297	SYNC_HS[2]	-2860	-537.5
298	SYNC_HS[3]	-2816	-537.5
299	SYNC_HS[4]	-2772	-537.5
300	SYNC_HS[5]	-2728	-537.5
301	SYNC_HS[6]	-2684	-537.5
302	SYNC_HS[7]	-2640	-537.5
303	SYNC_HS[8]	-2596	-537.5
304	SYNC_HS[9]	-2552	-537.5
305	SYNC_HS[10]	-2508	-537.5
306	SYNC_HS[11]	-2464	-537.5
307	SYNC_HS[12]	-2420	-537.5
308	SYNC_HS[13]	-2376	-537.5
309	SYNC_HS[14]	-2332	-537.5
310	SYNC_HS[15]	-2288	-537.5
311	TP_FLASH_SS	-2244	-537.5
312	TP_FLASH_MISO	-2200	-537.5
313	TP_FLASH_MOSI	-2156	-537.5
314	TP_FLASH_SCL	-2112	-537.5
315	VDDI	-2068	-537.5
316	VDDI	-2024	-537.5
317	VDDI	-1980	-537.5
318	VDDI	-1936	-537.5
319	VSS	-1892	-537.5
320	VSS	-1848	-537.5
321	VSS	-1804	-537.5
322	VSS	-1760	-537.5
323	VDD_TP	-1716	-537.5
324	VDD_TP	-1672	-537.5
325	VDD_TP	-1628	-537.5
326	ENB_CASCADE	-1584	-537.5
327	TP_MS	-1540	-537.5
328	TP_FLASH_HOLD	-1496	-537.5
329	TP_FLASH_WP	-1452	-537.5
330	LCD_GPIO[1]	-1408	-537.5
331	LCD_SDA	-1364	-537.5
332	LCD_SCL	-1320	-537.5
333	SYNC_HS[16]	-1276	-537.5
334	CRYSTAL_OUT	-1232	-537.5
335	CRYSTAL_OUT	-1188	-537.5
336	CRYSTAL_OUT	-1144	-537.5
337	CRYSTAL_IN	-1100	-537.5
338	CRYSTAL_IN	-1056	-537.5
339	CRYSTAL_IN	-1012	-537.5
340	VSS_TP_OSC	-968	-537.5
341	VSS_TP_OSC	-924	-537.5
342	VDD_TP_OSC	-880	-537.5
343	VDD_TP_OSC	-836	-537.5
344	VDD_TP_OSC	-792	-537.5
345	VDD_TP	-748	-537.5
346	VDD_TP	-704	-537.5
347	VDD_TP	-660	-537.5
348	VDD_TP	-616	-537.5
349	VDD_TP	-572	-537.5
350	VDD_TP	-528	-537.5
351	VDD_TP	-484	-537.5
352	VDD_TP	-440	-537.5
353	VSS	-396	-537.5
354	VSS	-352	-537.5
355	VSS	-308	-537.5
356	VSS	-264	-537.5
357	VSS	-220	-537.5
358	VSS	-176	-537.5
359	VSS	-132	-537.5
360	VSS	-88	-537.5
361	VDD	-44	-537.5
362	VDD	0	-537.5
363	VDD	44	-537.5
364	VDD	88	-537.5

No.	PAD Name	X	Y
365	VDD	132	-537.5
366	VDD	176	-537.5
367	VDD	220	-537.5
368	AVEE	264	-537.5
369	AVEE	308	-537.5
370	AVEE	352	-537.5
371	AVEE	396	-537.5
372	AVEE	440	-537.5
373	AVEE	484	-537.5
374	VCL	528	-537.5
375	VCL	572	-537.5
376	VCL	616	-537.5
377	VCOMDC	660	-537.5
378	VCOMDC	704	-537.5
379	VCOMDC	748	-537.5
380	VCOMDC	792	-537.5
381	VCOMDC	836	-537.5
382	VCOMDC	880	-537.5
383	VCOMDC	924	-537.5
384	VCOM_FB	968	-537.5
385	VDDI	1012	-537.5
386	VDDI	1056	-537.5
387	VDDI	1100	-537.5
388	VDDI	1144	-537.5
389	VDDI	1188	-537.5
390	VDDI	1232	-537.5
391	VDDI	1276	-537.5
392	AVSS	1320	-537.5
393	AVSS	1364	-537.5
394	AVSS	1408	-537.5
395	AVSS	1452	-537.5
396	AVSS	1496	-537.5
397	AVSS	1540	-537.5
398	AVSS	1584	-537.5
399	AVSS	1628	-537.5
400	AVDD	1672	-537.5
401	AVDD	1716	-537.5
402	AVDD	1760	-537.5
403	AVDD	1804	-537.5
404	AVDD	1848	-537.5
405	AVDD	1892	-537.5
406	AVDD	1936	-537.5
407	AVDD	1980	-537.5
408	VSS	2024	-537.5
409	VSS	2068	-537.5
410	VSS	2112	-537.5
411	VSS	2156	-537.5
412	VDD	2200	-537.5
413	VDD	2244	-537.5
414	VDD	2288	-537.5
415	VDD	2332	-537.5
416	VDD	2376	-537.5
417	VDD	2420	-537.5
418	VDD	2464	-537.5
419	VDD	2508	-537.5
420	VDD	2552	-537.5
421	VDD	2596	-537.5
422	VDDI	2640	-537.5
423	VDDI	2684	-537.5
424	VDDI	2728	-537.5
425	VDDI	2772	-537.5
426	VDDI	2816	-537.5
427	VDDI	2860	-537.5
428	VDDI	2904	-537.5
429	LVDSVSS	2948	-537.5
430	LVDSVSS	2992	-537.5
431	LVDSVSS	3036	-537.5
432	LVDSVDD	3080	-537.5
433	LVDSVDD	3124	-537.5
434	LVDSVDD	3168	-537.5
435	LVDSVDD	3212	-537.5
436	LVDSVDD	3256	-537.5
437	DATAP[2]	3300	-537.5
438	DATAP[2]	3344	-537.5

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No.	PAD Name	X	Y
439	DATAP[2]	3388	-537.5
440	DATAP[2]	3432	-537.5
441	LVDSVSS	3476	-537.5
442	DATAN[2]	3520	-537.5
443	DATAN[2]	3564	-537.5
444	DATAN[2]	3608	-537.5
445	DATAN[2]	3652	-537.5
446	LVDSVSS	3696	-537.5
447	DATAP[1]	3740	-537.5
448	DATAP[1]	3784	-537.5
449	DATAP[1]	3828	-537.5
450	DATAP[1]	3872	-537.5
451	LVDSVSS	3916	-537.5
452	DATAN[1]	3960	-537.5
453	DATAN[1]	4004	-537.5
454	DATAN[1]	4048	-537.5
455	DATAN[1]	4092	-537.5
456	LVDSVSS	4136	-537.5
457	CLKP	4180	-537.5
458	CLKP	4224	-537.5
459	CLKP	4268	-537.5
460	CLKP	4312	-537.5
461	LVDSVSS	4356	-537.5
462	CLKN	4400	-537.5
463	CLKN	4444	-537.5
464	CLKN	4488	-537.5
465	CLKN	4532	-537.5
466	LVDSVSS	4576	-537.5
467	DATAP[0]	4620	-537.5
468	DATAP[0]	4664	-537.5
469	DATAP[0]	4708	-537.5
470	DATAP[0]	4752	-537.5
471	LVDSVSS	4796	-537.5
472	DATAN[0]	4840	-537.5
473	DATAN[0]	4884	-537.5
474	DATAN[0]	4928	-537.5
475	DATAN[0]	4972	-537.5
476	LVDSVSS	5016	-537.5
477	DATAP[3]	5060	-537.5
478	DATAP[3]	5104	-537.5
479	DATAP[3]	5148	-537.5
480	DATAP[3]	5192	-537.5
481	LVDSVSS	5236	-537.5
482	DATAN[3]	5280	-537.5
483	DATAN[3]	5324	-537.5
484	DATAN[3]	5368	-537.5
485	DATAN[3]	5412	-537.5
486	LVDSVSS	5456	-537.5
487	LVDSVSS	5500	-537.5
488	LVDSVSS	5544	-537.5
489	LVDSVSS	5588	-537.5
490	LVDSVDD	5632	-537.5
491	LVDSVDD	5676	-537.5
492	LVDSVDD	5720	-537.5
493	LVDSVDD	5764	-537.5
494	LVDSVDD	5808	-537.5
495	LVDSVDD	5852	-537.5
496	VDD	5896	-537.5
497	VDD	5940	-537.5
498	VDD	5984	-537.5
499	VDD	6028	-537.5
500	VSS	6072	-537.5
501	VSS	6116	-537.5
502	VSS	6160	-537.5
503	VSS	6204	-537.5
504	AVSS	6248	-537.5
505	AVSS	6292	-537.5
506	AVSS	6336	-537.5
507	AVSS	6380	-537.5
508	AVSS	6424	-537.5
509	AVSS	6468	-537.5
510	AVSS	6512	-537.5
511	AVSS	6556	-537.5
512	AVSS	6600	-537.5

No.	PAD Name	X	Y
513	AVSS	6644	-537.5
514	AVDD	6688	-537.5
515	AVDD	6732	-537.5
516	AVDD	6776	-537.5
517	AVDD	6820	-537.5
518	AVDD	6864	-537.5
519	AVDD	6908	-537.5
520	AVDD	6952	-537.5
521	AVEE	6996	-537.5
522	AVEE	7040	-537.5
523	AVEE	7084	-537.5
524	AVEE	7128	-537.5
525	AVEE	7172	-537.5
526	AVEE	7216	-537.5
527	VCOM_R	7260	-537.5
528	VCOM_R	7304	-537.5
529	VCOM_R	7348	-537.5
530	VCOM_R	7392	-537.5
531	VCOM_R	7436	-537.5
532	VCOM_R	7480	-537.5
533	VCOM_R	7524	-537.5
534	VCOM_R	7568	-537.5
535	VCOM_R	7612	-537.5
536	VCOM_R	7656	-537.5
537	VDD_TP	7700	-537.5
538	VDD_TP	7744	-537.5
539	VDD_TP	7788	-537.5
540	VDD_TP	7832	-537.5
541	VDD_TP	7876	-537.5
542	VDD_TP	7920	-537.5
543	VDD_TP	7964	-537.5
544	VDD_TP	8008	-537.5
545	VDDI	8052	-537.5
546	VDDI	8096	-537.5
547	VDDI	8140	-537.5
548	VDDI	8184	-537.5
549	VDDI	8228	-537.5
550	VDDI	8272	-537.5
551	VSS	8316	-537.5
552	VSS	8360	-537.5
553	VSS	8404	-537.5
554	VSS	8448	-537.5
555	VSS	8492	-537.5
556	VREF_TP_R	8536	-537.5
557	VREF_TP_R	8580	-537.5
558	VREF_TP_R	8624	-537.5
559	VREF_ST_R	8668	-537.5
560	VREF_ST_R	8712	-537.5
561	VREF_ST_R	8756	-537.5
562	VDDI	8800	-537.5
563	VDDI	8844	-537.5
564	VDDI	8888	-537.5
565	VDDI	8932	-537.5
566	VDD	8976	-537.5
567	VDD	9020	-537.5
568	VDD	9064	-537.5
569	VDD	9108	-537.5
570	VDD	9152	-537.5
571	VDD	9196	-537.5
572	VDD	9240	-537.5
573	VDD	9284	-537.5
574	TAVSS_R	9328	-537.5
575	TAVSS_R	9372	-537.5
576	TAVSS_R	9416	-537.5
577	TAVSS_R	9460	-537.5
578	TAVSS_R	9504	-537.5
579	TAVSS_R	9548	-537.5
580	TAVDD_R	9592	-537.5
581	TAVDD_R	9636	-537.5
582	TAVDD_R	9680	-537.5
583	TAVDD_R	9724	-537.5
584	TAVDD_R	9768	-537.5
585	TAVDD_R	9812	-537.5
586	VSS	9856	-537.5

No.	PAD Name	X	Y
587	VSS	9900	-537.5
588	VSS	9944	-537.5
589	VSS	9988	-537.5
590	VSS	10032	-537.5
591	VSS	10076	-537.5
592	VGHB	10120	-537.5
593	VGHB	10164	-537.5
594	VGHB	10208	-537.5
595	VGHB	10252	-537.5
596	VGHB	10296	-537.5
597	VGHB	10340	-537.5
598	VDD_TP	10384	-537.5
599	VDD_TP	10428	-537.5
600	VDD_TP	10472	-537.5
601	VDD_TP	10516	-537.5
602	VDD_TP	10560	-537.5
603	VDD_TP	10604	-537.5
604	VSS	10648	-537.5
605	VSS	10692	-537.5
606	VSS	10736	-537.5
607	VSS	10780	-537.5
608	VSS	10824	-537.5
609	VSS	10868	-537.5
610	AVSS	10912	-537.5
611	AVSS	10956	-537.5
612	AVSS	11000	-537.5
613	AVSS	11044	-537.5
614	DUMMY	11088	-537.5
615	DUMMY	11132	-537.5
616	AVDD	11176	-537.5
617	AVDD	11220	-537.5
618	AVDD	11264	-537.5
619	AVDD	11308	-537.5
620	AVDD	11352	-537.5
621	AVDD	11396	-537.5
622	AVDD	11440	-537.5
623	AVDD	11484	-537.5
624	AVDD	11528	-537.5
625	AVDD	11572	-537.5
626	AVDD	11616	-537.5
627	AVDD	11660	-537.5
628	AVDD	11704	-537.5
629	AVDD	11748	-537.5
630	AVDD	11792	-537.5
631	AVDD	11836	-537.5
632	AVSS	11880	-537.5
633	AVSS	11924	-537.5
634	AVSS	11968	-537.5
635	AVSS	12012	-537.5
636	AVSS	12056	-537.5
637	TP_AFE_SCAN_MODE	12100	-537.5
638	TEST[3]	12144	-537.5
639	TEST[4]	12188	-537.5
640	TEST[5]	12232	-537.5
641	TEST[6]	12276	-537.5
642	TEST[7]	12320	-537.5
643	TEST[8]	12364	-537.5
644	TEST[9]	12408	-537.5
645	TEST[10]	12452	-537.5
646	TEST[11]	12496	-537.5
647	TEST[12]	12540	-537.5
648	TEST[13]	12584	-537.5
649	TEST[14]	12628	-537.5
650	TEST[15]	12672	-537.5
651	TEST[16]	12716	-537.5
652	AFE_TEST_R[0]	12760	-537.5
653	AFE_TEST_R[1]	12804	-537.5
654	AFE_TEST_R[1]	12848	-537.5
655	C31N	12892	-537.5
656	C31N	12936	-537.5
657	C31N	12980	-537.5
658	C31N	13024	-537.5
659	C31N	13068	-537.5
660	VGH_R	13112	-537.5

No.	PAD Name	X	Y
661	VGH_R	13156	-537.5
662	VGH_R	13200	-537.5
663	VGH_R	13244	-537.5
664	VGH_R	13288	-537.5
665	C31P	13332	-537.5
666	C31P	13376	-537.5
667	C31P	13420	-537.5
668	C31P	13464	-537.5
669	C31P	13508	-537.5
670	VGL	13552	-537.5
671	VGL	13596	-537.5
672	VGL	13640	-537.5
673	VGL	13684	-537.5
674	VGL	13728	-537.5
675	AVEE	13772	-537.5
676	AVEE	13816	-537.5
677	AVEE	13860	-537.5
678	AVEE	13904	-537.5
679	AVEE	13948	-537.5
680	AVSS	13992	-537.5
681	AVSS	14036	-537.5
682	AVSS	14080	-537.5
683	AVSS	14124	-537.5
684	AVSS	14168	-537.5
685	AVDD	14212	-537.5
686	AVDD	14256	-537.5
687	AVDD	14300	-537.5
688	AVDD	14344	-537.5
689	AVDD	14388	-537.5
690	VGLO_R	14432	-537.5
691	VGLO_R	14476	-537.5
692	VGH2_R	14520	-537.5
693	VGH2_R	14564	-537.5
694	VGH1_R	14608	-537.5
695	VGH1_R	14652	-537.5
696	VGH1_R	14696	-537.5
697	VGHO_R	14740	-537.5
698	VGHO_R	14784	-537.5
699	VGHO_R	14828	-537.5
700	CGOUT_R[1]	14872	-537.5
701	CGOUT_R[2]	14916	-537.5
702	CGOUT_R[3]	14960	-537.5
703	CGOUT_R[4]	15004	-537.5
704	CGOUT_R[5]	15048	-537.5
705	CGOUT_R[6]	15092	-537.5
706	CGOUT_R[7]	15136	-537.5
707	CGOUT_R[8]	15180	-537.5
708	CGOUT_R[9]	15224	-537.5
709	CGOUT_R[10]	15268	-537.5
710	CGOUT_R[11]	15312	-537.5
711	CGOUT_R[12]	15356	-537.5
712	CGOUT_R[13]	15400	-537.5
713	CGOUT_R[14]	15444	-537.5
714	CGOUT_R[15]	15488	-555
715	CGOUT_R[16]	15532	-555
716	CGOUT_R[17]	15576	-555
717	CGOUT_R[18]	15620	-555
718	CGOUT_R[19]	15664	-555
719	CGOUT_R[20]	15708	-555
720	CGOUT_R[21]	15752	-555
721	CGOUT_R[22]	15796	-555
722	CGOUT_R[23]	15840	-555
723	CGOUT_R[24]	15884	-555
724	GAMMA_N_R[7]	16069	-248
725	GAMMA_N_R[6]	16060.5	-140
726	GAMMA_N_R[5]	16052	-32
727	GAMMA_N_R[4]	16043.5	76
728	GAMMA_N_R[3]	16035	-245.2
729	GAMMA_N_R[2]	16026.5	-137.2
730	GAMMA_N_R[1]	16018	-29.2
731	GAMMA_N_R[0]	16009.5	78.8
732	GAMMA_P_R[0]	16001	-242.4
733	GAMMA_P_R[1]	15992.5	-134.4
734	GAMMA_P_R[2]	15984	-26.4

No.	PAD Name	X	Y
735	GAMMA_P_R[3]	15975.5	81.6
736	GAMMA_P_R[4]	15967	-239.6
737	GAMMA_P_R[5]	15958.5	-131.6
738	GAMMA_P_R[6]	15950	-23.6
739	GAMMA_P_R[7]	15941.5	84.4
740	VCOM	15933	-236.8
741	VCOM	15924.5	-128.8
742	VCOM_OPT_R	15916	-20.8
743	VCOM_OPT_R	15907.5	87.2
744	S[0]	15899	-234
745	S[1]	15890.5	-126
746	RX[1]	15882	-18
747	S[2]	15873.5	90
748	S[3]	15865	-231.2
749	RX[2]	15856.5	-123.2
750	S[4]	15848	-15.2
751	S[5]	15839.5	92.8
752	RX[3]	15831	-228.4
753	S[6]	15822.5	-120.4
754	S[7]	15814	-12.4
755	RX[4]	15805.5	95.6
756	S[8]	15797	-225.6
757	S[9]	15788.5	-117.6
758	RX[5]	15780	-9.6
759	S[10]	15771.5	98.4
760	S[11]	15763	-222.8
761	RX[6]	15754.5	-114.8
762	S[12]	15746	-6.8
763	S[13]	15737.5	101.2
764	RX[7]	15729	-220
765	S[14]	15720.5	-112
766	S[15]	15712	-4
767	RX[8]	15703.5	104
768	S[16]	15695	-217.2
769	S[17]	15686.5	-109.2
770	RX[9]	15678	-1.2
771	S[18]	15669.5	106.8
772	S[19]	15661	-214.4
773	RX[10]	15652.5	-106.4
774	S[20]	15644	1.6
775	S[21]	15635.5	109.6
776	RX[11]	15627	-211.6
777	S[22]	15618.5	-103.6
778	S[23]	15610	4.4
779	RX[12]	15601.5	112.4
780	S[24]	15593	-208.8
781	S[25]	15584.5	-100.8
782	RX[13]	15576	7.2
783	S[26]	15567.5	115.2
784	S[27]	15559	-206
785	RX[14]	15550.5	-98
786	S[28]	15542	10
787	S[29]	15533.5	118
788	RX[15]	15525	-203.2
789	S[30]	15516.5	-95.2
790	S[31]	15508	12.8
791	RX[16]	15499.5	120.8
792	S[32]	15491	-200.4
793	S[33]	15482.5	-92.4
794	RX[17]	15474	15.6
795	S[34]	15465.5	123.6
796	S[35]	15457	-197.6
797	RX[18]	15448.5	-89.6
798	S[36]	15440	18.4
799	S[37]	15431.5	126.4
800	RX[19]	15423	-194.8
801	S[38]	15414.5	-86.8
802	S[39]	15406	21.2
803	RX[20]	15397.5	129.2
804	S[40]	15389	-192
805	S[41]	15380.5	-84
806	RX[21]	15372	24
807	S[42]	15363.5	132
808	S[43]	15355	-189.2

No.	PAD Name	X	Y
809	RX[22]	15346.5	-81.2
810	S[44]	15338	26.8
811	S[45]	15329.5	134.8
812	RX[23]	15321	-186.4
813	S[46]	15312.5	-78.4
814	S[47]	15304	29.6
815	RX[24]	15295.5	137.6
816	S[48]	15287	-183.6
817	S[49]	15278.5	-75.6
818	RX[25]	15270	32.4
819	S[50]	15261.5	140.4
820	S[51]	15253	-180.8
821	RX[26]	15244.5	-72.8
822	S[52]	15236	35.2
823	S[53]	15227.5	143.2
824	RX[27]	15219	-178
825	S[54]	15210.5	-70
826	S[55]	15202	38
827	RX[28]	15193.5	146
828	S[56]	15185	-175.2
829	S[57]	15176.5	-67.2
830	RX[29]	15168	40.8
831	S[58]	15159.5	148.8
832	S[59]	15151	-172.4
833	RX[30]	15142.5	-64.4
834	S[60]	15134	43.6
835	S[61]	15125.5	151.6
836	RX[31]	15117	-169.6
837	S[62]	15108.5	-61.6
838	S[63]	15100	46.4
839	RX[32]	15091.5	154.4
840	S[64]	15083	-166.8
841	S[65]	15074.5	-58.8
842	RX[33]	15066	49.2
843	S[66]	15057.5	157.2
844	S[67]	15049	-164
845	RX[34]	15040.5	-56
846	S[68]	15032	52
847	S[69]	15023.5	160
848	RX[35]	15015	-161.2
849	S[70]	15006.5	-53.2
850	S[71]	14998	54.8
851	RX[36]	14989.5	162.8
852	S[72]	14981	-158.4
853	S[73]	14972.5	-50.4
854	RX[37]	14964	57.6
855	S[74]	14955.5	165.6
856	S[75]	14947	-155.6
857	RX[38]	14938.5	-47.6
858	S[76]	14930	60.4
859	S[77]	14921.5	168.4
860	RX[39]	14913	-152.8
861	S[78]	14904.5	-44.8
862	S[79]	14896	63.2
863	RX[40]	14887.5	171.2
864	S[80]	14879	-150
865	S[81]	14870.5	-42
866	RX[41]	14862	66
867	S[82]	14853.5	174
868	S[83]	14845	-147.2
869	RX[42]	14836.5	-39.2
870	S[84]	14828	68.8
871	S[85]	14819.5	176.8
872	RX[43]	14811	-144.4
873	S[86]	14802.5	-36.4
874	S[87]	14794	71.6
875	RX[44]	14785.5	179.6
876	S[88]	14777	-141.6
877	S[89]	14768.5	-33.6
878	RX[45]	14760	74.4
879	S[90]	14751.5	182.4
880	S[91]	14743	-138.8
881	RX[46]	14734.5	-30.8
882	S[92]	14726	77.2

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No.	PAD Name	X	Y
883	S[93]	14717.5	185.2
884	RX[47]	14709	-136
885	S[94]	14700.5	-28
886	S[95]	14692	80
887	RX[48]	14683.5	188
888	S[96]	14675	-133.2
889	S[97]	14666.5	-25.2
890	RX[49]	14658	82.8
891	S[98]	14649.5	190.8
892	S[99]	14641	-130.4
893	RX[50]	14632.5	-22.4
894	S[100]	14624	85.6
895	S[101]	14615.5	193.6
896	RX[51]	14607	-127.6
897	S[102]	14598.5	-19.6
898	S[103]	14590	88.4
899	RX[52]	14581.5	196.4
900	S[104]	14573	-124.8
901	S[105]	14564.5	-16.8
902	RX[53]	14556	91.2
903	S[106]	14547.5	199.2
904	S[107]	14539	-122
905	RX[54]	14530.5	-14
906	S[108]	14522	94
907	S[109]	14513.5	202
908	RX[55]	14505	-119.2
909	S[110]	14496.5	-11.2
910	S[111]	14488	96.8
911	RX[56]	14479.5	204.8
912	S[112]	14471	-116.4
913	S[113]	14462.5	-8.4
914	RX[57]	14454	99.6
915	S[114]	14445.5	207.6
916	S[115]	14437	-113.6
917	RX[58]	14428.5	-5.6
918	S[116]	14420	102.4
919	S[117]	14411.5	210.4
920	RX[59]	14403	-110.8
921	S[118]	14394.5	-2.8
922	S[119]	14386	105.2
923	RX[60]	14377.5	213.2
924	S[120]	14369	-108
925	S[121]	14360.5	0
926	RX[61]	14352	108
927	S[122]	14343.5	216
928	S[123]	14335	-105.2
929	RX[62]	14326.5	2.8
930	S[124]	14318	110.8
931	S[125]	14309.5	218.8
932	RX[63]	14301	-102.4
933	S[126]	14292.5	5.6
934	S[127]	14284	113.6
935	RX[64]	14275.5	221.6
936	S[128]	14267	-99.6
937	S[129]	14258.5	8.4
938	RX[65]	14250	116.4
939	S[130]	14241.5	224.4
940	S[131]	14233	-96.8
941	RX[66]	14224.5	11.2
942	S[132]	14216	119.2
943	S[133]	14207.5	227.2
944	RX[67]	14199	-94
945	S[134]	14190.5	14
946	S[135]	14182	122
947	RX[68]	14173.5	230
948	S[136]	14165	-91.2
949	S[137]	14156.5	16.8
950	RX[69]	14148	124.8
951	S[138]	14139.5	232.8
952	S[139]	14131	-88.4
953	RX[70]	14122.5	19.6
954	S[140]	14114	127.6
955	S[141]	14105.5	235.6
956	RX[71]	14097	-85.6

No.	PAD Name	X	Y
957	S[142]	14088.5	22.4
958	S[143]	14080	130.4
959	RX[72]	14071.5	238.4
960	S[144]	14063	-82.8
961	S[145]	14054.5	25.2
962	RX[73]	14046	133.2
963	S[146]	14037.5	241.2
964	S[147]	14029	-80
965	RX[74]	14020.5	28
966	S[148]	14012	136
967	S[149]	14003.5	244
968	RX[75]	13995	-77.2
969	S[150]	13986.5	30.8
970	S[151]	13978	138.8
971	RX[76]	13969.5	246.8
972	S[152]	13961	-74.4
973	S[153]	13952.5	33.6
974	RX[77]	13944	141.6
975	S[154]	13935.5	249.6
976	S[155]	13927	-71.6
977	RX[78]	13918.5	36.4
978	S[156]	13910	144.4
979	S[157]	13901.5	252.4
980	RX[79]	13893	-68.8
981	S[158]	13884.5	39.2
982	S[159]	13876	147.2
983	RX[80]	13867.5	255.2
984	S[160]	13859	-66
985	S[161]	13850.5	42
986	RX[81]	13842	150
987	S[162]	13833.5	258
988	S[163]	13825	-63.2
989	RX[82]	13816.5	44.8
990	S[164]	13808	152.8
991	S[165]	13799.5	260.8
992	RX[83]	13791	-60.4
993	S[166]	13782.5	47.6
994	S[167]	13774	155.6
995	RX[84]	13765.5	263.6
996	S[168]	13757	-57.6
997	S[169]	13748.5	50.4
998	RX[85]	13740	158.4
999	S[170]	13731.5	266.4
1000	S[171]	13723	-54.8
1001	RX[86]	13714.5	53.2
1002	S[172]	13706	161.2
1003	S[173]	13697.5	269.2
1004	RX[87]	13689	-52
1005	S[174]	13680.5	56
1006	S[175]	13672	164
1007	RX[88]	13663.5	272
1008	S[176]	13655	-49.2
1009	S[177]	13646.5	58.8
1010	RX[89]	13638	166.8
1011	S[178]	13629.5	274.8
1012	S[179]	13621	-46.4
1013	RX[90]	13612.5	61.6
1014	S[180]	13604	169.6
1015	S[181]	13595.5	277.6
1016	RX[91]	13587	-43.6
1017	S[182]	13578.5	64.4
1018	S[183]	13570	172.4
1019	RX[92]	13561.5	280.4
1020	S[184]	13553	-40.8
1021	S[185]	13544.5	67.2
1022	RX[93]	13536	175.2
1023	S[186]	13527.5	283.2
1024	S[187]	13519	-38
1025	RX[94]	13510.5	70
1026	S[188]	13502	178
1027	S[189]	13493.5	286
1028	RX[95]	13485	-35.2
1029	S[190]	13476.5	72.8
1030	S[191]	13468	180.8

No.	PAD Name	X	Y
1031	RX[96]	13459.5	288.8
1032	S[192]	13451	-32.4
1033	S[193]	13442.5	75.6
1034	RX[97]	13434	183.6
1035	S[194]	13425.5	291.6
1036	S[195]	13417	-29.6
1037	RX[98]	13408.5	78.4
1038	S[196]	13400	186.4
1039	S[197]	13391.5	294.4
1040	RX[99]	13383	-26.8
1041	S[198]	13374.5	81.2
1042	S[199]	13366	189.2
1043	RX[100]	13357.5	297.2
1044	S[200]	13349	-24
1045	S[201]	13340.5	84
1046	RX[101]	13332	192
1047	S[202]	13323.5	300
1048	S[203]	13315	-21.2
1049	RX[102]	13306.5	86.8
1050	S[204]	13298	194.8
1051	S[205]	13289.5	302.8
1052	RX[103]	13281	-18.4
1053	S[206]	13272.5	89.6
1054	S[207]	13264	197.6
1055	RX[104]	13255.5	305.6
1056	S[208]	13247	-15.6
1057	S[209]	13238.5	92.4
1058	RX[105]	13230	200.4
1059	S[210]	13221.5	308.4
1060	S[211]	13213	-12.8
1061	RX[106]	13204.5	95.2
1062	S[212]	13196	203.2
1063	S[213]	13187.5	311.2
1064	RX[107]	13179	-10
1065	S[214]	13170.5	98
1066	S[215]	13162	206
1067	RX[108]	13153.5	314
1068	S[216]	13145	-7.2
1069	S[217]	13136.5	100.8
1070	RX[109]	13128	208.8
1071	S[218]	13119.5	316.8
1072	S[219]	13111	-4.4
1073	RX[110]	13102.5	103.6
1074	S[220]	13094	211.6
1075	S[221]	13085.5	319.6
1076	RX[111]	13077	-1.6
1077	S[222]	13068.5	106.4
1078	S[223]	13060	214.4
1079	RX[112]	13051.5	322.4
1080	S[224]	13043	1.2
1081	S[225]	13034.5	109.2
1082	RX[113]	13026	217.2
1083	S[226]	13017.5	325.2
1084	S[227]	13009	4
1085	RX[114]	13000.5	112
1086	S[228]	12992	220
1087	S[229]	12983.5	328
1088	RX[115]	12975	6.8
1089	S[230]	12966.5	114.8
1090	S[231]	12958	222.8
1091	RX[116]	12949.5	330.8
1092	S[232]	12941	9.6
1093	S[233]	12932.5	117.6
1094	RX[117]	12924	225.6
1095	S[234]	12915.5	333.6
1096	S[235]	12907	12.4
1097	RX[118]	12898.5	120.4
1098	S[236]	12890	228.4
1099	S[237]	12881.5	336.4
1100	RX[119]	12873	15.2
1101	S[238]	12864.5	123.2
1102	S[239]	12856	231.2
1103	RX[120]	12847.5	339.2
1104	S[240]	12839	18

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No.	PAD Name	X	Y
1105	S[241]	12830.5	126
1106	RX[121]	12822	234
1107	S[242]	12813.5	342
1108	S[243]	12805	20.8
1109	RX[122]	12796.5	128.8
1110	S[244]	12788	236.8
1111	S[245]	12779.5	344.8
1112	RX[123]	12771	23.6
1113	S[246]	12762.5	131.6
1114	S[247]	12754	239.6
1115	RX[124]	12745.5	347.6
1116	S[248]	12737	26.4
1117	S[249]	12728.5	134.4
1118	RX[125]	12720	242.4
1119	S[250]	12711.5	350.4
1120	S[251]	12703	29.2
1121	RX[126]	12694.5	137.2
1122	S[252]	12686	245.2
1123	S[253]	12677.5	353.2
1124	RX[127]	12669	32
1125	S[254]	12660.5	140
1126	S[255]	12652	248
1127	RX[128]	12643.5	356
1128	S[256]	12635	34.8
1129	S[257]	12626.5	142.8
1130	RX[129]	12618	250.8
1131	S[258]	12609.5	358.8
1132	S[259]	12601	37.6
1133	RX[130]	12592.5	145.6
1134	S[260]	12584	253.6
1135	S[261]	12575.5	361.6
1136	RX[131]	12567	40.4
1137	S[262]	12558.5	148.4
1138	S[263]	12550	256.4
1139	RX[132]	12541.5	364.4
1140	S[264]	12533	43.2
1141	S[265]	12524.5	151.2
1142	RX[133]	12516	259.2
1143	S[266]	12507.5	367.2
1144	S[267]	12499	46
1145	RX[134]	12490.5	154
1146	S[268]	12482	262
1147	S[269]	12473.5	370
1148	RX[135]	12465	48.8
1149	S[270]	12456.5	156.8
1150	S[271]	12448	264.8
1151	RX[136]	12439.5	372.8
1152	S[272]	12431	51.6
1153	S[273]	12422.5	159.6
1154	RX[137]	12414	267.6
1155	S[274]	12405.5	375.6
1156	S[275]	12397	54.4
1157	RX[138]	12388.5	162.4
1158	S[276]	12380	270.4
1159	S[277]	12371.5	378.4
1160	RX[139]	12363	57.2
1161	S[278]	12354.5	165.2
1162	S[279]	12346	273.2
1163	RX[140]	12337.5	381.2
1164	S[280]	12329	60
1165	S[281]	12320.5	168
1166	RX[141]	12312	276
1167	S[282]	12303.5	384
1168	S[283]	12295	62.8
1169	RX[142]	12286.5	170.8
1170	S[284]	12278	278.8
1171	S[285]	12269.5	386.8
1172	RX[143]	12261	65.6
1173	S[286]	12252.5	173.6
1174	S[287]	12244	281.6
1175	RX[144]	12235.5	389.6
1176	S[288]	12227	68.4
1177	S[289]	12218.5	176.4
1178	RX[145]	12210	284.4
1179	S[290]	12201.5	392.4
1180	S[291]	12193	71.2
1181	RX[146]	12184.5	179.2
1182	S[292]	12176	287.2
1183	S[293]	12167.5	395.2
1184	RX[147]	12159	74
1185	S[294]	12150.5	182
1186	S[295]	12142	290
1187	RX[148]	12133.5	398
1188	S[296]	12125	76.8
1189	S[297]	12116.5	184.8
1190	RX[149]	12108	292.8
1191	S[298]	12099.5	400.8
1192	S[299]	12091	79.6
1193	RX[150]	12082.5	187.6
1194	S[300]	12074	295.6
1195	S[301]	12065.5	403.6
1196	RX[151]	12057	82.4
1197	S[302]	12048.5	190.4
1198	S[303]	12040	298.4
1199	RX[152]	12031.5	406.4
1200	S[304]	12023	85.2
1201	S[305]	12014.5	193.2
1202	RX[153]	12006	301.2
1203	S[306]	11997.5	409.2
1204	S[307]	11989	88
1205	RX[154]	11980.5	196
1206	S[308]	11972	304
1207	S[309]	11963.5	412
1208	RX[155]	11955	90.8
1209	S[310]	11946.5	198.8
1210	S[311]	11938	306.8
1211	RX[156]	11929.5	414.8
1212	S[312]	11921	93.6
1213	S[313]	11912.5	201.6
1214	RX[157]	11904	309.6
1215	S[314]	11895.5	417.6
1216	S[315]	11887	96.4
1217	RX[158]	11878.5	204.4
1218	S[316]	11870	312.4
1219	S[317]	11861.5	420.4
1220	RX[159]	11853	99.2
1221	S[318]	11844.5	207.2
1222	S[319]	11836	315.2
1223	RX[160]	11827.5	423.2
1224	S[320]	11819	102
1225	S[321]	11810.5	210
1226	RX[161]	11802	318
1227	S[322]	11793.5	426
1228	S[323]	11785	104.8
1229	RX[162]	11776.5	212.8
1230	S[324]	11768	320.8
1231	S[325]	11759.5	428.8
1232	RX[163]	11751	107.6
1233	S[326]	11742.5	215.6
1234	S[327]	11734	323.6
1235	RX[164]	11725.5	431.6
1236	S[328]	11717	110.4
1237	S[329]	11708.5	218.4
1238	RX[165]	11700	326.4
1239	S[330]	11691.5	434.4
1240	S[331]	11683	113.2
1241	RX[166]	11674.5	221.2
1242	S[332]	11666	329.2
1243	S[333]	11657.5	437.2
1244	RX[167]	11649	116
1245	S[334]	11640.5	224
1246	S[335]	11632	332
1247	RX[168]	11623.5	440
1248	S[336]	11615	118.8
1249	S[337]	11606.5	226.8
1250	RX[169]	11598	334.8
1251	S[338]	11589.5	442.8
1252	S[339]	11581	121.6
1253	RX[170]	11572.5	229.6
1254	S[340]	11564	337.6
1255	S[341]	11555.5	445.6
1256	RX[171]	11547	124.4
1257	S[342]	11538.5	232.4
1258	S[343]	11530	340.4
1259	RX[172]	11521.5	448.4
1260	S[344]	11513	127.2
1261	S[345]	11504.5	235.2
1262	RX[173]	11496	343.2
1263	S[346]	11487.5	451.2
1264	S[347]	11479	130
1265	RX[174]	11470.5	238
1266	S[348]	11462	346
1267	S[349]	11453.5	454
1268	RX[175]	11445	132.8
1269	S[350]	11436.5	240.8
1270	S[351]	11428	348.8
1271	RX[176]	11419.5	456.8
1272	S[352]	11411	135.6
1273	S[353]	11402.5	243.6
1274	RX[177]	11394	351.6
1275	S[354]	11385.5	459.6
1276	S[355]	11377	138.4
1277	RX[178]	11368.5	246.4
1278	S[356]	11360	354.4
1279	S[357]	11351.5	462.4
1280	RX[179]	11343	141.2
1281	S[358]	11334.5	249.2
1282	S[359]	11326	357.2
1283	RX[180]	11317.5	465.2
1284	S[360]	11309	144
1285	S[361]	11300.5	252
1286	RX[181]	11292	360
1287	S[362]	11283.5	468
1288	S[363]	11275	146.8
1289	RX[182]	11266.5	254.8
1290	S[364]	11258	362.8
1291	S[365]	11249.5	470.8
1292	RX[183]	11241	149.6
1293	S[366]	11232.5	257.6
1294	S[367]	11224	365.6
1295	RX[184]	11215.5	473.6
1296	S[368]	11207	152.4
1297	S[369]	11198.5	260.4
1298	RX[185]	11190	368.4
1299	S[370]	11181.5	476.4
1300	S[371]	11173	155.2
1301	RX[186]	11164.5	263.2
1302	S[372]	11156	371.2
1303	S[373]	11147.5	479.2
1304	RX[187]	11139	158
1305	S[374]	11130.5	266
1306	S[375]	11122	374
1307	RX[188]	11113.5	482
1308	S[376]	11105	160.8
1309	S[377]	11096.5	268.8
1310	RX[189]	11088	376.8
1311	S[378]	11079.5	484.8
1312	S[379]	11071	163.6
1313	RX[190]	11062.5	271.6
1314	S[380]	11054	379.6
1315	S[381]	11045.5	487.6
1316	RX[191]	11037	166.4
1317	S[382]	11028.5	274.4
1318	S[383]	11020	382.4
1319	RX[192]	11011.5	490.4
1320	S[384]	11003	169.2
1321	S[385]	10994.5	277.2
1322	RX[193]	10986	385.2
1323	S[386]	10977.5	493.2
1324	S[387]	10969	172
1325	RX[194]	10960.5	280
1326	S[388]	10952	388

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No.	PAD Name	X	Y
1327	S[389]	10943.5	496
1328	RX[195]	10935	172
1329	S[390]	10926.5	280
1330	S[391]	10918	388
1331	RX[196]	10909.5	496
1332	S[392]	10901	172
1333	S[393]	10892.5	280
1334	RX[197]	10884	388
1335	S[394]	10875.5	496
1336	S[395]	10867	172
1337	RX[198]	10858.5	280
1338	S[396]	10850	388
1339	S[397]	10841.5	496
1340	RX[199]	10833	172
1341	S[398]	10824.5	280
1342	S[399]	10816	388
1343	RX[200]	10807.5	496
1344	S[400]	10799	172
1345	S[401]	10790.5	280
1346	RX[201]	10782	388
1347	S[402]	10773.5	496
1348	S[403]	10765	172
1349	RX[202]	10756.5	280
1350	S[404]	10748	388
1351	S[405]	10739.5	496
1352	RX[203]	10731	172
1353	S[406]	10722.5	280
1354	S[407]	10714	388
1355	RX[204]	10705.5	496
1356	S[408]	10697	172
1357	S[409]	10688.5	280
1358	RX[205]	10680	388
1359	S[410]	10671.5	496
1360	S[411]	10663	172
1361	RX[206]	10654.5	280
1362	S[412]	10646	388
1363	S[413]	10637.5	496
1364	RX[207]	10629	172
1365	S[414]	10620.5	280
1366	S[415]	10612	388
1367	RX[208]	10603.5	496
1368	S[416]	10595	172
1369	S[417]	10586.5	280
1370	RX[209]	10578	388
1371	S[418]	10569.5	496
1372	S[419]	10561	172
1373	RX[210]	10552.5	280
1374	S[420]	10544	388
1375	S[421]	10535.5	496
1376	RX[211]	10527	172
1377	S[422]	10518.5	280
1378	S[423]	10510	388
1379	RX[212]	10501.5	496
1380	S[424]	10493	172
1381	S[425]	10484.5	280
1382	RX[213]	10476	388
1383	S[426]	10467.5	496
1384	S[427]	10459	172
1385	RX[214]	10450.5	280
1386	S[428]	10442	388
1387	S[429]	10433.5	496
1388	RX[215]	10425	172
1389	S[430]	10416.5	280
1390	S[431]	10408	388
1391	RX[216]	10399.5	496
1392	S[432]	10391	172
1393	S[433]	10382.5	280
1394	RX[217]	10374	388
1395	S[434]	10365.5	496
1396	S[435]	10357	172
1397	RX[218]	10348.5	280
1398	S[436]	10340	388
1399	S[437]	10331.5	496
1400	RX[219]	10323	172

No.	PAD Name	X	Y
1401	S[438]	10314.5	280
1402	S[439]	10306	388
1403	RX[220]	10297.5	496
1404	S[440]	10289	172
1405	S[441]	10280.5	280
1406	RX[221]	10272	388
1407	S[442]	10263.5	496
1408	S[443]	10255	172
1409	RX[222]	10246.5	280
1410	S[444]	10238	388
1411	S[445]	10229.5	496
1412	RX[223]	10221	172
1413	S[446]	10212.5	280
1414	S[447]	10204	388
1415	RX[224]	10195.5	496
1416	S[448]	10187	172
1417	S[449]	10178.5	280
1418	RX[225]	10170	388
1419	S[450]	10161.5	496
1420	S[451]	10153	172
1421	RX[226]	10144.5	280
1422	S[452]	10136	388
1423	S[453]	10127.5	496
1424	RX[227]	10119	172
1425	S[454]	10110.5	280
1426	S[455]	10102	388
1427	RX[228]	10093.5	496
1428	S[456]	10085	172
1429	S[457]	10076.5	280
1430	RX[229]	10068	388
1431	S[458]	10059.5	496
1432	S[459]	10051	172
1433	RX[230]	10042.5	280
1434	S[460]	10034	388
1435	S[461]	10025.5	496
1436	RX[231]	10017	172
1437	S[462]	10008.5	280
1438	S[463]	10000	388
1439	RX[232]	9991.5	496
1440	S[464]	9983	172
1441	S[465]	9974.5	280
1442	RX[233]	9966	388
1443	S[466]	9957.5	496
1444	S[467]	9949	172
1445	RX[234]	9940.5	280
1446	S[468]	9932	388
1447	S[469]	9923.5	496
1448	RX[235]	9915	172
1449	S[470]	9906.5	280
1450	S[471]	9898	388
1451	RX[236]	9889.5	496
1452	S[472]	9881	172
1453	S[473]	9872.5	280
1454	RX[237]	9864	388
1455	S[474]	9855.5	496
1456	S[475]	9847	172
1457	RX[238]	9838.5	280
1458	S[476]	9830	388
1459	S[477]	9821.5	496
1460	RX[239]	9813	172
1461	S[478]	9804.5	280
1462	S[479]	9796	388
1463	RX[240]	9787.5	496
1464	S[480]	9779	172
1465	S[481]	9770.5	280
1466	RX[241]	9762	388
1467	S[482]	9753.5	496
1468	S[483]	9745	172
1469	RX[242]	9736.5	280
1470	S[484]	9728	388
1471	S[485]	9719.5	496
1472	RX[243]	9711	172
1473	S[486]	9702.5	280
1474	S[487]	9694	388

No.	PAD Name	X	Y
1475	RX[244]	9685.5	496
1476	S[488]	9677	172
1477	S[489]	9668.5	280
1478	RX[245]	9660	388
1479	S[490]	9651.5	496
1480	S[491]	9643	172
1481	RX[246]	9634.5	280
1482	S[492]	9626	388
1483	S[493]	9617.5	496
1484	RX[247]	9609	172
1485	S[494]	9600.5	280
1486	S[495]	9592	388
1487	RX[248]	9583.5	496
1488	S[496]	9575	172
1489	S[497]	9566.5	280
1490	RX[249]	9558	388
1491	S[498]	9549.5	496
1492	S[499]	9541	172
1493	RX[250]	9532.5	280
1494	S[500]	9524	388
1495	S[501]	9515.5	496
1496	RX[251]	9507	172
1497	S[502]	9498.5	280
1498	S[503]	9490	388
1499	RX[252]	9481.5	496
1500	S[504]	9473	172
1501	S[505]	9464.5	280
1502	RX[253]	9456	388
1503	S[506]	9447.5	496
1504	S[507]	9439	172
1505	RX[254]	9430.5	280
1506	S[508]	9422	388
1507	S[509]	9413.5	496
1508	RX[255]	9405	172
1509	S[510]	9396.5	280
1510	S[511]	9388	388
1511	RX[256]	9379.5	496
1512	S[512]	9371	172
1513	S[513]	9362.5	280
1514	RX[257]	9354	388
1515	S[514]	9345.5	496
1516	S[515]	9337	172
1517	RX[258]	9328.5	280
1518	S[516]	9320	388
1519	S[517]	9311.5	496
1520	RX[259]	9303	172
1521	S[518]	9294.5	280
1522	S[519]	9286	388
1523	RX[260]	9277.5	496
1524	S[520]	9269	172
1525	S[521]	9260.5	280
1526	RX[261]	9252	388
1527	S[522]	9243.5	496
1528	S[523]	9235	172
1529	RX[262]	9226.5	280
1530	S[524]	9218	388
1531	S[525]	9209.5	496
1532	RX[263]	9201	172
1533	S[526]	9192.5	280
1534	S[527]	9184	388
1535	RX[264]	9175.5	496
1536	S[528]	9167	172
1537	S[529]	9158.5	280
1538	RX[265]	9150	388
1539	S[530]	9141.5	496
1540	S[531]	9133	172
1541	RX[266]	9124.5	280
1542	S[532]	9116	388
1543	S[533]	9107.5	496
1544	RX[267]	9099	172
1545	S[534]	9090.5	280
1546	S[535]	9082	388
1547	RX[268]	9073.5	496
1548	S[536]	9065	172

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No.	PAD Name	X	Y
1549	S[537]	9056.5	280
1550	RX[269]	9048	388
1551	S[538]	9039.5	496
1552	S[539]	9031	172
1553	RX[270]	9022.5	280
1554	S[540]	9014	388
1555	S[541]	9005.5	496
1556	RX[271]	8997	172
1557	S[542]	8988.5	280
1558	S[543]	8980	388
1559	RX[272]	8971.5	496
1560	S[544]	8963	172
1561	S[545]	8954.5	280
1562	RX[273]	8946	388
1563	S[546]	8937.5	496
1564	S[547]	8929	172
1565	RX[274]	8920.5	280
1566	S[548]	8912	388
1567	S[549]	8903.5	496
1568	RX[275]	8895	172
1569	S[550]	8886.5	280
1570	S[551]	8878	388
1571	RX[276]	8869.5	496
1572	S[552]	8861	172
1573	S[553]	8852.5	280
1574	RX[277]	8844	388
1575	S[554]	8835.5	496
1576	S[555]	8827	172
1577	RX[278]	8818.5	280
1578	S[556]	8810	388
1579	S[557]	8801.5	496
1580	RX[279]	8793	172
1581	S[558]	8784.5	280
1582	S[559]	8776	388
1583	RX[280]	8767.5	496
1584	S[560]	8759	172
1585	S[561]	8750.5	280
1586	RX[281]	8742	388
1587	S[562]	8733.5	496
1588	S[563]	8725	172
1589	RX[282]	8716.5	280
1590	S[564]	8708	388
1591	S[565]	8699.5	496
1592	RX[283]	8691	172
1593	S[566]	8682.5	280
1594	S[567]	8674	388
1595	RX[284]	8665.5	496
1596	S[568]	8657	172
1597	S[569]	8648.5	280
1598	RX[285]	8640	388
1599	S[570]	8631.5	496
1600	S[571]	8623	172
1601	RX[286]	8614.5	280
1602	S[572]	8606	388
1603	S[573]	8597.5	496
1604	RX[287]	8589	172
1605	S[574]	8580.5	280
1606	S[575]	8572	388
1607	RX[288]	8563.5	496
1608	S[576]	8555	172
1609	S[577]	8546.5	280
1610	RX[289]	8538	388
1611	S[578]	8529.5	496
1612	S[579]	8521	172
1613	RX[290]	8512.5	280
1614	S[580]	8504	388
1615	S[581]	8495.5	496
1616	RX[291]	8487	172
1617	S[582]	8478.5	280
1618	S[583]	8470	388
1619	RX[292]	8461.5	496
1620	S[584]	8453	172
1621	S[585]	8444.5	280
1622	RX[293]	8436	388
1623	S[586]	8427.5	496
1624	S[587]	8419	172
1625	RX[294]	8410.5	280
1626	S[588]	8402	388
1627	S[589]	8393.5	496
1628	RX[295]	8385	172
1629	S[590]	8376.5	280
1630	S[591]	8368	388
1631	RX[296]	8359.5	496
1632	S[592]	8351	172
1633	S[593]	8342.5	280
1634	RX[297]	8334	388
1635	S[594]	8325.5	496
1636	S[595]	8317	172
1637	RX[298]	8308.5	280
1638	S[596]	8300	388
1639	S[597]	8291.5	496
1640	RX[299]	8283	172
1641	S[598]	8274.5	280
1642	S[599]	8266	388
1643	RX[300]	8257.5	496
1644	S[600]	8249	172
1645	S[601]	8240.5	280
1646	RX[301]	8232	388
1647	S[602]	8223.5	496
1648	S[603]	8215	172
1649	RX[302]	8206.5	280
1650	S[604]	8198	388
1651	S[605]	8189.5	496
1652	RX[303]	8181	172
1653	S[606]	8172.5	280
1654	S[607]	8164	388
1655	RX[304]	8155.5	496
1656	S[608]	8147	172
1657	S[609]	8138.5	280
1658	RX[305]	8130	388
1659	S[610]	8121.5	496
1660	S[611]	8113	172
1661	RX[306]	8104.5	280
1662	S[612]	8096	388
1663	S[613]	8087.5	496
1664	RX[307]	8079	172
1665	S[614]	8070.5	280
1666	S[615]	8062	388
1667	RX[308]	8053.5	496
1668	S[616]	8045	172
1669	S[617]	8036.5	280
1670	RX[309]	8028	388
1671	S[618]	8019.5	496
1672	S[619]	8011	172
1673	RX[310]	8002.5	280
1674	S[620]	7994	388
1675	S[621]	7985.5	496
1676	RX[311]	7977	172
1677	S[622]	7968.5	280
1678	S[623]	7960	388
1679	RX[312]	7951.5	496
1680	S[624]	7943	172
1681	S[625]	7934.5	280
1682	RX[313]	7926	388
1683	S[626]	7917.5	496
1684	S[627]	7909	172
1685	RX[314]	7900.5	280
1686	S[628]	7892	388
1687	S[629]	7883.5	496
1688	RX[315]	7875	172
1689	S[630]	7866.5	280
1690	S[631]	7858	388
1691	RX[316]	7849.5	496
1692	S[632]	7841	172
1693	S[633]	7832.5	280
1694	RX[317]	7824	388
1695	S[634]	7815.5	496
1696	S[635]	7807	172
1697	RX[318]	7798.5	280
1698	S[636]	7790	388
1699	S[637]	7781.5	496
1700	RX[319]	7773	172
1701	S[638]	7764.5	280
1702	S[639]	7756	388
1703	RX[320]	7747.5	496
1704	S[640]	7739	172
1705	S[641]	7730.5	280
1706	RX[321]	7722	388
1707	S[642]	7713.5	496
1708	S[643]	7705	172
1709	RX[322]	7696.5	280
1710	S[644]	7688	388
1711	S[645]	7679.5	496
1712	RX[323]	7671	172
1713	S[646]	7662.5	280
1714	S[647]	7654	388
1715	RX[324]	7645.5	496
1716	S[648]	7637	172
1717	S[649]	7628.5	280
1718	RX[325]	7620	388
1719	S[650]	7611.5	496
1720	S[651]	7603	172
1721	RX[326]	7594.5	280
1722	S[652]	7586	388
1723	S[653]	7577.5	496
1724	RX[327]	7569	172
1725	S[654]	7560.5	280
1726	S[655]	7552	388
1727	RX[328]	7543.5	496
1728	S[656]	7535	172
1729	S[657]	7526.5	280
1730	RX[329]	7518	388
1731	S[658]	7509.5	496
1732	S[659]	7501	172
1733	RX[330]	7492.5	280
1734	S[660]	7484	388
1735	S[661]	7475.5	496
1736	RX[331]	7467	172
1737	S[662]	7458.5	280
1738	S[663]	7450	388
1739	RX[332]	7441.5	496
1740	S[664]	7433	172
1741	S[665]	7424.5	280
1742	RX[333]	7416	388
1743	S[666]	7407.5	496
1744	S[667]	7399	172
1745	RX[334]	7390.5	280
1746	S[668]	7382	388
1747	S[669]	7373.5	496
1748	RX[335]	7365	172
1749	S[670]	7356.5	280
1750	S[671]	7348	388
1751	RX[336]	7339.5	496
1752	S[672]	7331	172
1753	S[673]	7322.5	280
1754	RX[337]	7314	388
1755	S[674]	7305.5	496
1756	S[675]	7297	172
1757	RX[338]	7288.5	280
1758	S[676]	7280	388
1759	S[677]	7271.5	496
1760	RX[339]	7263	172
1761	S[678]	7254.5	280
1762	S[679]	7246	388
1763	RX[340]	7237.5	496
1764	S[680]	7229	172
1765	S[681]	7220.5	280
1766	RX[341]	7212	388
1767	S[682]	7203.5	496
1768	S[683]	7195	172
1769	RX[342]	7186.5	280
1770	S[684]	7178	388

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No.	PAD Name	X	Y
1771	S[685]	7169.5	496
1772	RX[343]	7161	172
1773	S[686]	7152.5	280
1774	S[687]	7144	388
1775	RX[344]	7135.5	496
1776	S[688]	7127	172
1777	S[689]	7118.5	280
1778	RX[345]	7110	388
1779	S[690]	7101.5	496
1780	S[691]	7093	172
1781	RX[346]	7084.5	280
1782	S[692]	7076	388
1783	S[693]	7067.5	496
1784	RX[347]	7059	172
1785	S[694]	7050.5	280
1786	S[695]	7042	388
1787	RX[348]	7033.5	496
1788	S[696]	7025	172
1789	S[697]	7016.5	280
1790	RX[349]	7008	388
1791	S[698]	6999.5	496
1792	S[699]	6991	172
1793	RX[350]	6982.5	280
1794	S[700]	6974	388
1795	S[701]	6965.5	496
1796	RX[351]	6957	172
1797	S[702]	6948.5	280
1798	S[703]	6940	388
1799	RX[352]	6931.5	496
1800	S[704]	6923	172
1801	S[705]	6914.5	280
1802	RX[353]	6906	388
1803	S[706]	6897.5	496
1804	S[707]	6889	172
1805	RX[354]	6880.5	280
1806	S[708]	6872	388
1807	S[709]	6863.5	496
1808	RX[355]	6855	172
1809	S[710]	6846.5	280
1810	S[711]	6838	388
1811	RX[356]	6829.5	496
1812	S[712]	6821	172
1813	S[713]	6812.5	280
1814	RX[357]	6804	388
1815	S[714]	6795.5	496
1816	S[715]	6787	172
1817	RX[358]	6778.5	280
1818	S[716]	6770	388
1819	S[717]	6761.5	496
1820	RX[359]	6753	172
1821	S[718]	6744.5	280
1822	S[719]	6736	388
1823	RX[360]	6727.5	496
1824	S[720]	6719	172
1825	S[721]	6710.5	280
1826	RX[361]	6702	388
1827	S[722]	6693.5	496
1828	S[723]	6685	172
1829	RX[362]	6676.5	280
1830	S[724]	6668	388
1831	S[725]	6659.5	496
1832	RX[363]	6651	172
1833	S[726]	6642.5	280
1834	S[727]	6634	388
1835	RX[364]	6625.5	496
1836	S[728]	6617	172
1837	S[729]	6608.5	280
1838	RX[365]	6600	388
1839	S[730]	6591.5	496
1840	S[731]	6583	172
1841	RX[366]	6574.5	280
1842	S[732]	6566	388
1843	S[733]	6557.5	496
1844	RX[367]	6549	172
1845	S[734]	6540.5	280
1846	S[735]	6532	388
1847	RX[368]	6523.5	496
1848	S[736]	6515	172
1849	S[737]	6506.5	280
1850	RX[369]	6498	388
1851	S[738]	6489.5	496
1852	S[739]	6481	172
1853	RX[370]	6472.5	280
1854	S[740]	6464	388
1855	S[741]	6455.5	496
1856	RX[371]	6447	172
1857	S[742]	6438.5	280
1858	S[743]	6430	388
1859	RX[372]	6421.5	496
1860	S[744]	6413	172
1861	S[745]	6404.5	280
1862	RX[373]	6396	388
1863	S[746]	6387.5	496
1864	S[747]	6379	172
1865	RX[374]	6370.5	280
1866	S[748]	6362	388
1867	S[749]	6353.5	496
1868	RX[375]	6345	172
1869	S[750]	6336.5	280
1870	S[751]	6328	388
1871	RX[376]	6319.5	496
1872	S[752]	6311	172
1873	S[753]	6302.5	280
1874	RX[377]	6294	388
1875	S[754]	6285.5	496
1876	S[755]	6277	172
1877	RX[378]	6268.5	280
1878	S[756]	6260	388
1879	S[757]	6251.5	496
1880	RX[379]	6243	172
1881	S[758]	6234.5	280
1882	S[759]	6226	388
1883	RX[380]	6217.5	496
1884	S[760]	6209	172
1885	S[761]	6200.5	280
1886	RX[381]	6192	388
1887	S[762]	6183.5	496
1888	S[763]	6175	172
1889	RX[382]	6166.5	280
1890	S[764]	6158	388
1891	S[765]	6149.5	496
1892	RX[383]	6141	172
1893	S[766]	6132.5	280
1894	S[767]	6124	388
1895	RX[384]	6115.5	496
1896	S[768]	6107	172
1897	S[769]	6098.5	280
1898	RX[385]	6090	388
1899	S[770]	6081.5	496
1900	S[771]	6073	172
1901	RX[386]	6064.5	280
1902	S[772]	6056	388
1903	S[773]	6047.5	496
1904	RX[387]	6039	172
1905	S[774]	6030.5	280
1906	S[775]	6022	388
1907	RX[388]	6013.5	496
1908	S[776]	6005	172
1909	S[777]	5996.5	280
1910	RX[389]	5988	388
1911	S[778]	5979.5	496
1912	S[779]	5971	172
1913	RX[390]	5962.5	280
1914	S[780]	5954	388
1915	S[781]	5945.5	496
1916	RX[391]	5937	172
1917	S[782]	5928.5	280
1918	S[783]	5920	388
1919	RX[392]	5911.5	496
1920	S[784]	5903	172
1921	S[785]	5894.5	280
1922	RX[393]	5886	388
1923	S[786]	5877.5	496
1924	S[787]	5869	172
1925	RX[394]	5860.5	280
1926	S[788]	5852	388
1927	S[789]	5843.5	496
1928	RX[395]	5835	172
1929	S[790]	5826.5	280
1930	S[791]	5818	388
1931	RX[396]	5809.5	496
1932	S[792]	5801	172
1933	S[793]	5792.5	280
1934	RX[397]	5784	388
1935	S[794]	5775.5	496
1936	S[795]	5767	172
1937	RX[398]	5758.5	280
1938	S[796]	5750	388
1939	S[797]	5741.5	496
1940	RX[399]	5733	172
1941	S[798]	5724.5	280
1942	S[799]	5716	388
1943	RX[400]	5707.5	496
1944	S[800]	5699	172
1945	S[801]	5690.5	280
1946	RX[401]	5682	388
1947	S[802]	5673.5	496
1948	S[803]	5665	172
1949	RX[402]	5656.5	280
1950	S[804]	5648	388
1951	S[805]	5639.5	496
1952	RX[403]	5631	172
1953	S[806]	5622.5	280
1954	S[807]	5614	388
1955	RX[404]	5605.5	496
1956	S[808]	5597	172
1957	S[809]	5588.5	280
1958	RX[405]	5580	388
1959	S[810]	5571.5	496
1960	S[811]	5563	172
1961	RX[406]	5554.5	280
1962	S[812]	5546	388
1963	S[813]	5537.5	496
1964	RX[407]	5529	172
1965	S[814]	5520.5	280
1966	S[815]	5512	388
1967	RX[408]	5503.5	496
1968	S[816]	5495	172
1969	S[817]	5486.5	280
1970	RX[409]	5478	388
1971	S[818]	5469.5	496
1972	S[819]	5461	172
1973	RX[410]	5452.5	280
1974	S[820]	5444	388
1975	S[821]	5435.5	496
1976	RX[411]	5427	172
1977	S[822]	5418.5	280
1978	S[823]	5410	388
1979	RX[412]	5401.5	496
1980	S[824]	5393	172
1981	S[825]	5384.5	280
1982	RX[413]	5376	388
1983	S[826]	5367.5	496
1984	S[827]	5359	172
1985	RX[414]	5350.5	280
1986	S[828]	5342	388
1987	S[829]	5333.5	496
1988	RX[415]	5325	172
1989	S[830]	5316.5	280
1990	S[831]	5308	388
1991	RX[416]	5299.5	496
1992	S[832]	5291	172

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No.	PAD Name	X	Y
1993	S[833]	5282.5	280
1994	RX[417]	5274	388
1995	S[834]	5265.5	496
1996	S[835]	5257	172
1997	RX[418]	5248.5	280
1998	S[836]	5240	388
1999	S[837]	5231.5	496
2000	RX[419]	5223	172
2001	S[838]	5214.5	280
2002	S[839]	5206	388
2003	RX[420]	5197.5	496
2004	S[840]	5189	172
2005	S[841]	5180.5	280
2006	RX[421]	5172	388
2007	S[842]	5163.5	496
2008	S[843]	5155	172
2009	RX[422]	5146.5	280
2010	S[844]	5138	388
2011	S[845]	5129.5	496
2012	RX[423]	5121	172
2013	S[846]	5112.5	280
2014	S[847]	5104	388
2015	RX[424]	5095.5	496
2016	S[848]	5087	172
2017	S[849]	5078.5	280
2018	RX[425]	5070	388
2019	S[850]	5061.5	496
2020	S[851]	5053	172
2021	RX[426]	5044.5	280
2022	S[852]	5036	388
2023	S[853]	5027.5	496
2024	RX[427]	5019	172
2025	S[854]	5010.5	280
2026	S[855]	5002	388
2027	RX[428]	4993.5	496
2028	S[856]	4985	172
2029	S[857]	4976.5	280
2030	RX[429]	4968	388
2031	S[858]	4959.5	496
2032	S[859]	4951	172
2033	RX[430]	4942.5	280
2034	S[860]	4934	388
2035	S[861]	4925.5	496
2036	RX[431]	4917	172
2037	S[862]	4908.5	280
2038	S[863]	4900	388
2039	RX[432]	4891.5	496
2040	S[864]	4883	172
2041	S[865]	4874.5	280
2042	RX[433]	4866	388
2043	S[866]	4857.5	496
2044	S[867]	4849	172
2045	RX[434]	4840.5	280
2046	S[868]	4832	388
2047	S[869]	4823.5	496
2048	RX[435]	4815	172
2049	S[870]	4806.5	280
2050	S[871]	4798	388
2051	RX[436]	4789.5	496
2052	S[872]	4781	172
2053	S[873]	4772.5	280
2054	RX[437]	4764	388
2055	S[874]	4755.5	496
2056	S[875]	4747	172
2057	RX[438]	4738.5	280
2058	S[876]	4730	388
2059	S[877]	4721.5	496
2060	RX[439]	4713	172
2061	S[878]	4704.5	280
2062	S[879]	4696	388
2063	RX[440]	4687.5	496
2064	S[880]	4679	172
2065	S[881]	4670.5	280
2066	RX[441]	4662	388

No.	PAD Name	X	Y
2067	S[882]	4653.5	496
2068	S[883]	4645	172
2069	RX[442]	4636.5	280
2070	S[884]	4628	388
2071	S[885]	4619.5	496
2072	RX[443]	4611	172
2073	S[886]	4602.5	280
2074	S[887]	4594	388
2075	RX[444]	4585.5	496
2076	S[888]	4577	172
2077	S[889]	4568.5	280
2078	RX[445]	4560	388
2079	S[890]	4551.5	496
2080	S[891]	4543	172
2081	RX[446]	4534.5	280
2082	S[892]	4526	388
2083	S[893]	4517.5	496
2084	RX[447]	4509	172
2085	S[894]	4500.5	280
2086	S[895]	4492	388
2087	RX[448]	4483.5	496
2088	S[896]	4475	172
2089	S[897]	4466.5	280
2090	RX[449]	4458	388
2091	S[898]	4449.5	496
2092	S[899]	4441	172
2093	RX[450]	4432.5	280
2094	S[900]	4424	388
2095	S[901]	4415.5	496
2096	RX[451]	4407	172
2097	S[902]	4398.5	280
2098	S[903]	4390	388
2099	RX[452]	4381.5	496
2100	S[904]	4373	172
2101	S[905]	4364.5	280
2102	RX[453]	4356	388
2103	S[906]	4347.5	496
2104	S[907]	4339	172
2105	RX[454]	4330.5	280
2106	S[908]	4322	388
2107	S[909]	4313.5	496
2108	RX[455]	4305	172
2109	S[910]	4296.5	280
2110	S[911]	4288	388
2111	RX[456]	4279.5	496
2112	S[912]	4271	172
2113	S[913]	4262.5	280
2114	RX[457]	4254	388
2115	S[914]	4245.5	496
2116	S[915]	4237	172
2117	RX[458]	4228.5	280
2118	S[916]	4220	388
2119	S[917]	4211.5	496
2120	RX[459]	4203	172
2121	S[918]	4194.5	280
2122	S[919]	4186	388
2123	RX[460]	4177.5	496
2124	S[920]	4169	172
2125	S[921]	4160.5	280
2126	RX[461]	4152	388
2127	S[922]	4143.5	496
2128	S[923]	4135	172
2129	RX[462]	4126.5	280
2130	S[924]	4118	388
2131	S[925]	4109.5	496
2132	RX[463]	4101	172
2133	S[926]	4092.5	280
2134	S[927]	4084	388
2135	RX[464]	4075.5	496
2136	S[928]	4067	172
2137	S[929]	4058.5	280
2138	RX[465]	4050	388
2139	S[930]	4041.5	496
2140	S[931]	4033	172

No.	PAD Name	X	Y
2141	RX[466]	4024.5	280
2142	S[932]	4016	388
2143	S[933]	4007.5	496
2144	RX[467]	3999	172
2145	S[934]	3990.5	280
2146	S[935]	3982	388
2147	RX[468]	3973.5	496
2148	S[936]	3965	172
2149	S[937]	3956.5	280
2150	RX[469]	3948	388
2151	S[938]	3939.5	496
2152	S[939]	3931	172
2153	RX[470]	3922.5	280
2154	S[940]	3914	388
2155	S[941]	3905.5	496
2156	RX[471]	3897	172
2157	S[942]	3888.5	280
2158	S[943]	3880	388
2159	RX[472]	3871.5	496
2160	S[944]	3863	172
2161	S[945]	3854.5	280
2162	RX[473]	3846	388
2163	S[946]	3837.5	496
2164	S[947]	3829	172
2165	RX[474]	3820.5	280
2166	S[948]	3812	388
2167	S[949]	3803.5	496
2168	RX[475]	3795	172
2169	S[950]	3786.5	280
2170	S[951]	3778	388
2171	RX[476]	3769.5	496
2172	S[952]	3761	172
2173	S[953]	3752.5	280
2174	RX[477]	3744	388
2175	S[954]	3735.5	496
2176	S[955]	3727	172
2177	RX[478]	3718.5	280
2178	S[956]	3710	388
2179	S[957]	3701.5	496
2180	RX[479]	3693	172
2181	S[958]	3684.5	280
2182	S[959]	3676	388
2183	RX[480]	3667.5	496
2184	S[960]	3659	172
2185	S[961]	3650.5	280
2186	RX[481]	3642	388
2187	S[962]	3633.5	496
2188	S[963]	3625	172
2189	RX[482]	3616.5	280
2190	S[964]	3608	388
2191	S[965]	3599.5	496
2192	RX[483]	3591	172
2193	S[966]	3582.5	280
2194	S[967]	3574	388
2195	RX[484]	3565.5	496
2196	S[968]	3557	172
2197	S[969]	3548.5	280
2198	RX[485]	3540	388
2199	S[970]	3531.5	496
2200	S[971]	3523	172
2201	RX[486]	3514.5	280
2202	S[972]	3506	388
2203	S[973]	3497.5	496
2204	RX[487]	3489	172
2205	S[974]	3480.5	280
2206	S[975]	3472	388
2207	RX[488]	3463.5	496
2208	S[976]	3455	172
2209	S[977]	3446.5	280
2210	RX[489]	3438	388
2211	S[978]	3429.5	496
2212	S[979]	3421	172
2213	RX[490]	3412.5	280
2214	S[980]	3404	388

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No.	PAD Name	X	Y
2215	S[981]	3395.5	496
2216	RX[491]	3387	172
2217	S[982]	3378.5	280
2218	S[983]	3370	388
2219	RX[492]	3361.5	496
2220	S[984]	3353	172
2221	S[985]	3344.5	280
2222	RX[493]	3336	388
2223	S[986]	3327.5	496
2224	S[987]	3319	172
2225	RX[494]	3310.5	280
2226	S[988]	3302	388
2227	S[989]	3293.5	496
2228	RX[495]	3285	172
2229	S[990]	3276.5	280
2230	S[991]	3268	388
2231	RX[496]	3259.5	496
2232	S[992]	3251	172
2233	S[993]	3242.5	280
2234	RX[497]	3234	388
2235	S[994]	3225.5	496
2236	S[995]	3217	172
2237	RX[498]	3208.5	280
2238	S[996]	3200	388
2239	S[997]	3191.5	496
2240	RX[499]	3183	172
2241	S[998]	3174.5	280
2242	S[999]	3166	388
2243	RX[500]	3157.5	496
2244	S[1000]	3149	172
2245	S[1001]	3140.5	280
2246	RX[501]	3132	388
2247	S[1002]	3123.5	496
2248	S[1003]	3115	172
2249	RX[502]	3106.5	280
2250	S[1004]	3098	388
2251	S[1005]	3089.5	496
2252	RX[503]	3081	172
2253	S[1006]	3072.5	280
2254	S[1007]	3064	388
2255	RX[504]	3055.5	496
2256	S[1008]	3047	172
2257	S[1009]	3038.5	280
2258	RX[505]	3030	388
2259	S[1010]	3021.5	496
2260	S[1011]	3013	172
2261	RX[506]	3004.5	280
2262	S[1012]	2996	388
2263	S[1013]	2987.5	496
2264	RX[507]	2979	172
2265	S[1014]	2970.5	280
2266	S[1015]	2962	388
2267	RX[508]	2953.5	496
2268	S[1016]	2945	172
2269	S[1017]	2936.5	280
2270	RX[509]	2928	388
2271	S[1018]	2919.5	496
2272	S[1019]	2911	172
2273	RX[510]	2902.5	280
2274	S[1020]	2894	388
2275	S[1021]	2885.5	496
2276	RX[511]	2877	172
2277	S[1022]	2868.5	280
2278	S[1023]	2860	388
2279	RX[512]	2851.5	496
2280	S[1024]	2843	172
2281	S[1025]	2834.5	280
2282	RX[513]	2826	388
2283	S[1026]	2817.5	496
2284	S[1027]	2809	172
2285	RX[514]	2800.5	280
2286	S[1028]	2792	388
2287	S[1029]	2783.5	496
2288	RX[515]	2775	172

No.	PAD Name	X	Y
2289	S[1030]	2766.5	280
2290	S[1031]	2758	388
2291	RX[516]	2749.5	496
2292	S[1032]	2741	172
2293	S[1033]	2732.5	280
2294	RX[517]	2724	388
2295	S[1034]	2715.5	496
2296	S[1035]	2707	172
2297	RX[518]	2698.5	280
2298	S[1036]	2690	388
2299	S[1037]	2681.5	496
2300	RX[519]	2673	172
2301	S[1038]	2664.5	280
2302	S[1039]	2656	388
2303	RX[520]	2647.5	496
2304	S[1040]	2639	172
2305	S[1041]	2630.5	280
2306	RX[521]	2622	388
2307	S[1042]	2613.5	496
2308	S[1043]	2605	172
2309	RX[522]	2596.5	280
2310	S[1044]	2588	388
2311	S[1045]	2579.5	496
2312	RX[523]	2571	172
2313	S[1046]	2562.5	280
2314	S[1047]	2554	388
2315	RX[524]	2545.5	496
2316	S[1048]	2537	172
2317	S[1049]	2528.5	280
2318	RX[525]	2520	388
2319	S[1050]	2511.5	496
2320	S[1051]	2503	172
2321	RX[526]	2494.5	280
2322	S[1052]	2486	388
2323	S[1053]	2477.5	496
2324	RX[527]	2469	172
2325	S[1054]	2460.5	280
2326	S[1055]	2452	388
2327	RX[528]	2443.5	496
2328	S[1056]	2435	172
2329	S[1057]	2426.5	280
2330	RX[529]	2418	388
2331	S[1058]	2409.5	496
2332	S[1059]	2401	172
2333	RX[530]	2392.5	280
2334	S[1060]	2384	388
2335	S[1061]	2375.5	496
2336	RX[531]	2367	172
2337	S[1062]	2358.5	280
2338	S[1063]	2350	388
2339	RX[532]	2341.5	496
2340	S[1064]	2333	172
2341	S[1065]	2324.5	280
2342	RX[533]	2316	388
2343	S[1066]	2307.5	496
2344	S[1067]	2299	172
2345	RX[534]	2290.5	280
2346	S[1068]	2282	388
2347	S[1069]	2273.5	496
2348	RX[535]	2265	172
2349	S[1070]	2256.5	280
2350	S[1071]	2248	388
2351	RX[536]	2239.5	496
2352	S[1072]	2231	172
2353	S[1073]	2222.5	280
2354	RX[537]	2214	388
2355	S[1074]	2205.5	496
2356	S[1075]	2197	172
2357	RX[538]	2188.5	280
2358	S[1076]	2180	388
2359	S[1077]	2171.5	496
2360	RX[539]	2163	172
2361	S[1078]	2154.5	280
2362	S[1079]	2146	388

No.	PAD Name	X	Y
2363	RX[540]	2137.5	496
2364	S[1080]	2129	172
2365	S[1081]	2120.5	280
2366	RX[541]	2112	388
2367	S[1082]	2103.5	496
2368	S[1083]	2095	172
2369	RX[542]	2086.5	280
2370	S[1084]	2078	388
2371	S[1085]	2069.5	496
2372	RX[543]	2061	172
2373	S[1086]	2052.5	280
2374	S[1087]	2044	388
2375	RX[544]	2035.5	496
2376	S[1088]	2027	172
2377	S[1089]	2018.5	280
2378	RX[545]	2010	388
2379	S[1090]	2001.5	496
2380	S[1091]	1993	172
2381	RX[546]	1984.5	280
2382	S[1092]	1976	388
2383	S[1093]	1967.5	496
2384	RX[547]	1959	172
2385	S[1094]	1950.5	280
2386	S[1095]	1942	388
2387	RX[548]	1933.5	496
2388	S[1096]	1925	172
2389	S[1097]	1916.5	280
2390	RX[549]	1908	388
2391	S[1098]	1899.5	496
2392	S[1099]	1891	172
2393	RX[550]	1882.5	280
2394	S[1100]	1874	388
2395	S[1101]	1865.5	496
2396	RX[551]	1857	172
2397	S[1102]	1848.5	280
2398	S[1103]	1840	388
2399	RX[552]	1831.5	496
2400	S[1104]	1823	172
2401	S[1105]	1814.5	280
2402	RX[553]	1806	388
2403	S[1106]	1797.5	496
2404	S[1107]	1789	172
2405	RX[554]	1780.5	280
2406	S[1108]	1772	388
2407	S[1109]	1763.5	496
2408	RX[555]	1755	172
2409	S[1110]	1746.5	280
2410	S[1111]	1738	388
2411	RX[556]	1729.5	496
2412	S[1112]	1721	172
2413	S[1113]	1712.5	280
2414	RX[557]	1704	388
2415	S[1114]	1695.5	496
2416	S[1115]	1687	172
2417	RX[558]	1678.5	280
2418	S[1116]	1670	388
2419	S[1117]	1661.5	496
2420	RX[559]	1653	172
2421	S[1118]	1644.5	280
2422	S[1119]	1636	388
2423	RX[560]	1627.5	496
2424	S[1120]	1619	172
2425	S[1121]	1610.5	280
2426	RX[561]	1602	388
2427	S[1122]	1593.5	496
2428	S[1123]	1585	172
2429	RX[562]	1576.5	280
2430	S[1124]	1568	388
2431	S[1125]	1559.5	496
2432	RX[563]	1551	172
2433	S[1126]	1542.5	280
2434	S[1127]	1534	388
2435	RX[564]	1525.5	496
2436	S[1128]	1517	172

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No.	PAD Name	X	Y
2437	S[1129]	1508.5	280
2438	RX[565]	1500	388
2439	S[1130]	1491.5	496
2440	S[1131]	1483	172
2441	RX[566]	1474.5	280
2442	S[1132]	1466	388
2443	S[1133]	1457.5	496
2444	RX[567]	1449	172
2445	S[1134]	1440.5	280
2446	S[1135]	1432	388
2447	RX[568]	1423.5	496
2448	S[1136]	1415	172
2449	S[1137]	1406.5	280
2450	RX[569]	1398	388
2451	S[1138]	1389.5	496
2452	S[1139]	1381	172
2453	RX[570]	1372.5	280
2454	S[1140]	1364	388
2455	S[1141]	1355.5	496
2456	RX[571]	1347	172
2457	S[1142]	1338.5	280
2458	S[1143]	1330	388
2459	RX[572]	1321.5	496
2460	S[1144]	1313	172
2461	S[1145]	1304.5	280
2462	RX[573]	1296	388
2463	S[1146]	1287.5	496
2464	S[1147]	1279	172
2465	RX[574]	1270.5	280
2466	S[1148]	1262	388
2467	S[1149]	1253.5	496
2468	RX[575]	1245	172
2469	S[1150]	1236.5	280
2470	S[1151]	1228	388
2471	RX[576]	1219.5	496
2472	S[1152]	1211	172
2473	S[1153]	1202.5	280
2474	RX[577]	1194	388
2475	S[1154]	1185.5	496
2476	S[1155]	1177	172
2477	RX[578]	1168.5	280
2478	S[1156]	1160	388
2479	S[1157]	1151.5	496
2480	RX[579]	1143	172
2481	S[1158]	1134.5	280
2482	S[1159]	1126	388
2483	RX[580]	1117.5	496
2484	S[1160]	1109	172
2485	S[1161]	1100.5	280
2486	RX[581]	1092	388
2487	S[1162]	1083.5	496
2488	S[1163]	1075	172
2489	RX[582]	1066.5	280
2490	S[1164]	1058	388
2491	S[1165]	1049.5	496
2492	RX[583]	1041	172
2493	S[1166]	1032.5	280
2494	S[1167]	1024	388
2495	RX[584]	1015.5	496
2496	S[1168]	1007	172
2497	S[1169]	998.5	280
2498	RX[585]	990	388
2499	S[1170]	981.5	496
2500	S[1171]	973	172
2501	RX[586]	964.5	280
2502	S[1172]	956	388
2503	S[1173]	947.5	496
2504	RX[587]	939	172
2505	S[1174]	930.5	280
2506	S[1175]	922	388
2507	RX[588]	913.5	496
2508	S[1176]	905	172
2509	S[1177]	896.5	280
2510	RX[589]	888	388

No.	PAD Name	X	Y
2511	S[1178]	879.5	496
2512	S[1179]	871	172
2513	RX[590]	862.5	280
2514	S[1180]	854	388
2515	S[1181]	845.5	496
2516	RX[591]	837	172
2517	S[1182]	828.5	280
2518	S[1183]	820	388
2519	RX[592]	811.5	496
2520	S[1184]	803	172
2521	S[1185]	794.5	280
2522	RX[593]	786	388
2523	S[1186]	777.5	496
2524	S[1187]	769	172
2525	RX[594]	760.5	280
2526	S[1188]	752	388
2527	S[1189]	743.5	496
2528	RX[595]	735	172
2529	S[1190]	726.5	280
2530	S[1191]	718	388
2531	RX[596]	709.5	496
2532	S[1192]	701	172
2533	S[1193]	692.5	280
2534	RX[597]	684	388
2535	S[1194]	675.5	496
2536	S[1195]	667	172
2537	RX[598]	658.5	280
2538	S[1196]	650	388
2539	S[1197]	641.5	496
2540	RX[599]	633	172
2541	S[1198]	624.5	280
2542	S[1199]	616	388
2543	RX[600]	607.5	496
2544	S[1200]	599	172
2545	RX[601]	590.5	280
2546	RX[602]	582	388
2547	RX[603]	573.5	496
2548	RX[604]	565	172
2549	RX[605]	556.5	280
2550	RX[606]	548	388
2551	RX[607]	539.5	496
2552	RX[608]	531	172
2553	RX[609]	522.5	280
2554	RX[610]	514	388
2555	RX[611]	505.5	496
2556	RX[612]	497	172
2557	RX[613]	488.5	280
2558	RX[614]	480	388
2559	RX[615]	471.5	496
2560	RX[616]	463	172
2561	RX[617]	454.5	280
2562	RX[618]	446	388
2563	RX[619]	437.5	496
2564	RX[620]	429	172
2565	RX[621]	420.5	280
2566	RX[622]	412	388
2567	RX[623]	403.5	496
2568	RX[624]	395	172
2569	RX[625]	386.5	280
2570	RX[626]	378	388
2571	RX[627]	369.5	496
2572	RX[628]	361	172
2573	RX[629]	352.5	280
2574	RX[630]	344	388
2575	RX[631]	335.5	496
2576	RX[632]	327	172
2577	RX[633]	318.5	280
2578	RX[634]	310	388
2579	RX[635]	301.5	496
2580	RX[636]	293	172
2581	RX[637]	284.5	280
2582	RX[638]	276	388
2583	RX[639]	267.5	496
2584	RX[640]	259	172

No.	PAD Name	X	Y
2585	DUMMY	250.5	280
2586	DUMMY	242	388
2587	DUMMY	233.5	496
2588	DUMMY	225	172
2589	DUMMY	216.5	280
2590	DUMMY	208	388
2591	DUMMY	199.5	496
2592	DUMMY	191	172
2593	DUMMY	182.5	280
2594	DUMMY	174	388
2595	DUMMY	165.5	496
2596	DUMMY	157	172
2597	AVDD	148.5	280
2598	AVDD	140	388
2599	AVDD	131.5	496
2600	AVDD	123	172
2601	AVDD	114.5	280
2602	AVDD	106	388
2603	AVDD	97.5	496
2604	AVDD	89	172
2605	DUMMY	80.5	280
2606	DUMMY	72	388
2607	DUMMY	63.5	496
2608	DUMMY	55	172
2609	AVSS	46.5	280
2610	AVSS	38	388
2611	AVSS	29.5	496
2612	AVSS	21	172
2613	AVSS	12.5	280
2614	AVSS	4	388
2615	AVSS	-4.5	496
2616	AVSS	-13	172
2617	AVSS	-21.5	280
2618	AVSS	-30	388
2619	AVSS	-38.5	496
2620	AVSS	-47	172
2621	DUMMY	-55.5	280
2622	DUMMY	-64	388
2623	DUMMY	-72.5	496
2624	DUMMY	-81	172
2625	AVEE	-89.5	280
2626	AVEE	-98	388
2627	AVEE	-106.5	496
2628	AVEE	-115	172
2629	AVEE	-123.5	280
2630	AVEE	-132	388
2631	AVEE	-140.5	496
2632	AVEE	-149	172
2633	DUMMY	-157.5	280
2634	DUMMY	-166	388
2635	DUMMY	-174.5	496
2636	DUMMY	-183	172
2637	DUMMY	-191.5	280
2638	DUMMY	-200	388
2639	DUMMY	-208.5	496
2640	DUMMY	-217	172
2641	DUMMY	-225.5	280
2642	DUMMY	-234	388
2643	DUMMY	-242.5	496
2644	DUMMY	-251	172
2645	RX[641]	-259.5	280
2646	RX[642]	-268	388
2647	RX[643]	-276.5	496
2648	RX[644]	-285	172
2649	RX[645]	-293.5	280
2650	RX[646]	-302	388
2651	RX[647]	-310.5	496
2652	RX[648]	-319	172
2653	RX[649]	-327.5	280
2654	RX[650]	-336	388
2655	RX[651]	-344.5	496
2656	RX[652]	-353	172
2657	RX[653]	-361.5	280
2658	RX[654]	-370	388

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No.	PAD Name	X	Y
2659	RX[655]	-378.5	496
2660	RX[656]	-387	172
2661	RX[657]	-395.5	280
2662	RX[658]	-404	388
2663	RX[659]	-412.5	496
2664	RX[660]	-421	172
2665	RX[661]	-429.5	280
2666	RX[662]	-438	388
2667	RX[663]	-446.5	496
2668	RX[664]	-455	172
2669	RX[665]	-463.5	280
2670	RX[666]	-472	388
2671	RX[667]	-480.5	496
2672	RX[668]	-489	172
2673	RX[669]	-497.5	280
2674	RX[670]	-506	388
2675	RX[671]	-514.5	496
2676	RX[672]	-523	172
2677	RX[673]	-531.5	280
2678	RX[674]	-540	388
2679	RX[675]	-548.5	496
2680	RX[676]	-557	172
2681	RX[677]	-565.5	280
2682	RX[678]	-574	388
2683	RX[679]	-582.5	496
2684	RX[680]	-591	172
2685	S[1201]	-599.5	280
2686	RX[681]	-608	388
2687	S[1202]	-616.5	496
2688	S[1203]	-625	172
2689	RX[682]	-633.5	280
2690	S[1204]	-642	388
2691	S[1205]	-650.5	496
2692	RX[683]	-659	172
2693	S[1206]	-667.5	280
2694	S[1207]	-676	388
2695	RX[684]	-684.5	496
2696	S[1208]	-693	172
2697	S[1209]	-701.5	280
2698	RX[685]	-710	388
2699	S[1210]	-718.5	496
2700	S[1211]	-727	172
2701	RX[686]	-735.5	280
2702	S[1212]	-744	388
2703	S[1213]	-752.5	496
2704	RX[687]	-761	172
2705	S[1214]	-769.5	280
2706	S[1215]	-778	388
2707	RX[688]	-786.5	496
2708	S[1216]	-795	172
2709	S[1217]	-803.5	280
2710	RX[689]	-812	388
2711	S[1218]	-820.5	496
2712	S[1219]	-829	172
2713	RX[690]	-837.5	280
2714	S[1220]	-846	388
2715	S[1221]	-854.5	496
2716	RX[691]	-863	172
2717	S[1222]	-871.5	280
2718	S[1223]	-880	388
2719	RX[692]	-888.5	496
2720	S[1224]	-897	172
2721	S[1225]	-905.5	280
2722	RX[693]	-914	388
2723	S[1226]	-922.5	496
2724	S[1227]	-931	172
2725	RX[694]	-939.5	280
2726	S[1228]	-948	388
2727	S[1229]	-956.5	496
2728	RX[695]	-965	172
2729	S[1230]	-973.5	280
2730	S[1231]	-982	388
2731	RX[696]	-990.5	496
2732	S[1232]	-999	172

No.	PAD Name	X	Y
2733	S[1233]	-1007.5	280
2734	RX[697]	-1016	388
2735	S[1234]	-1024.5	496
2736	S[1235]	-1033	172
2737	RX[698]	-1041.5	280
2738	S[1236]	-1050	388
2739	S[1237]	-1058.5	496
2740	RX[699]	-1067	172
2741	S[1238]	-1075.5	280
2742	S[1239]	-1084	388
2743	RX[700]	-1092.5	496
2744	S[1240]	-1101	172
2745	S[1241]	-1109.5	280
2746	RX[701]	-1118	388
2747	S[1242]	-1126.5	496
2748	S[1243]	-1135	172
2749	RX[702]	-1143.5	280
2750	S[1244]	-1152	388
2751	S[1245]	-1160.5	496
2752	RX[703]	-1169	172
2753	S[1246]	-1177.5	280
2754	S[1247]	-1186	388
2755	RX[704]	-1194.5	496
2756	S[1248]	-1203	172
2757	S[1249]	-1211.5	280
2758	RX[705]	-1220	388
2759	S[1250]	-1228.5	496
2760	S[1251]	-1237	172
2761	RX[706]	-1245.5	280
2762	S[1252]	-1254	388
2763	S[1253]	-1262.5	496
2764	RX[707]	-1271	172
2765	S[1254]	-1279.5	280
2766	S[1255]	-1288	388
2767	RX[708]	-1296.5	496
2768	S[1256]	-1305	172
2769	S[1257]	-1313.5	280
2770	RX[709]	-1322	388
2771	S[1258]	-1330.5	496
2772	S[1259]	-1339	172
2773	RX[710]	-1347.5	280
2774	S[1260]	-1356	388
2775	S[1261]	-1364.5	496
2776	RX[711]	-1373	172
2777	S[1262]	-1381.5	280
2778	S[1263]	-1390	388
2779	RX[712]	-1398.5	496
2780	S[1264]	-1407	172
2781	S[1265]	-1415.5	280
2782	RX[713]	-1424	388
2783	S[1266]	-1432.5	496
2784	S[1267]	-1441	172
2785	RX[714]	-1449.5	280
2786	S[1268]	-1458	388
2787	S[1269]	-1466.5	496
2788	RX[715]	-1475	172
2789	S[1270]	-1483.5	280
2790	S[1271]	-1492	388
2791	RX[716]	-1500.5	496
2792	S[1272]	-1509	172
2793	S[1273]	-1517.5	280
2794	RX[717]	-1526	388
2795	S[1274]	-1534.5	496
2796	S[1275]	-1543	172
2797	RX[718]	-1551.5	280
2798	S[1276]	-1560	388
2799	S[1277]	-1568.5	496
2800	RX[719]	-1577	172
2801	S[1278]	-1585.5	280
2802	S[1279]	-1594	388
2803	RX[720]	-1602.5	496
2804	S[1280]	-1611	172
2805	S[1281]	-1619.5	280
2806	RX[721]	-1628	388

No.	PAD Name	X	Y
2807	S[1282]	-1636.5	496
2808	S[1283]	-1645	172
2809	RX[722]	-1653.5	280
2810	S[1284]	-1662	388
2811	S[1285]	-1670.5	496
2812	RX[723]	-1679	172
2813	S[1286]	-1687.5	280
2814	S[1287]	-1696	388
2815	RX[724]	-1704.5	496
2816	S[1288]	-1713	172
2817	S[1289]	-1721.5	280
2818	RX[725]	-1730	388
2819	S[1290]	-1738.5	496
2820	S[1291]	-1747	172
2821	RX[726]	-1755.5	280
2822	S[1292]	-1764	388
2823	S[1293]	-1772.5	496
2824	RX[727]	-1781	172
2825	S[1294]	-1789.5	280
2826	S[1295]	-1798	388
2827	RX[728]	-1806.5	496
2828	S[1296]	-1815	172
2829	S[1297]	-1823.5	280
2830	RX[729]	-1832	388
2831	S[1298]	-1840.5	496
2832	S[1299]	-1849	172
2833	RX[730]	-1857.5	280
2834	S[1300]	-1866	388
2835	S[1301]	-1874.5	496
2836	RX[731]	-1883	172
2837	S[1302]	-1891.5	280
2838	S[1303]	-1900	388
2839	RX[732]	-1908.5	496
2840	S[1304]	-1917	172
2841	S[1305]	-1925.5	280
2842	RX[733]	-1934	388
2843	S[1306]	-1942.5	496
2844	S[1307]	-1951	172
2845	RX[734]	-1959.5	280
2846	S[1308]	-1968	388
2847	S[1309]	-1976.5	496
2848	RX[735]	-1985	172
2849	S[1310]	-1993.5	280
2850	S[1311]	-2002	388
2851	RX[736]	-2010.5	496
2852	S[1312]	-2019	172
2853	S[1313]	-2027.5	280
2854	RX[737]	-2036	388
2855	S[1314]	-2044.5	496
2856	S[1315]	-2053	172
2857	RX[738]	-2061.5	280
2858	S[1316]	-2070	388
2859	S[1317]	-2078.5	496
2860	RX[739]	-2087	172
2861	S[1318]	-2095.5	280
2862	S[1319]	-2104	388
2863	RX[740]	-2112.5	496
2864	S[1320]	-2121	172
2865	S[1321]	-2129.5	280
2866	RX[741]	-2138	388
2867	S[1322]	-2146.5	496
2868	S[1323]	-2155	172
2869	RX[742]	-2163.5	280
2870	S[1324]	-2172	388
2871	S[1325]	-2180.5	496
2872	RX[743]	-2189	172
2873	S[1326]	-2197.5	280
2874	S[1327]	-2206	388
2875	RX[744]	-2214.5	496
2876	S[1328]	-2223	172
2877	S[1329]	-2231.5	280
2878	RX[745]	-2240	388
2879	S[1330]	-2248.5	496
2880	S[1331]	-2257	172

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No.	PAD Name	X	Y
2881	RX[746]	-2265.5	280
2882	S[1332]	-2274	388
2883	S[1333]	-2282.5	496
2884	RX[747]	-2291	172
2885	S[1334]	-2299.5	280
2886	S[1335]	-2308	388
2887	RX[748]	-2316.5	496
2888	S[1336]	-2325	172
2889	S[1337]	-2333.5	280
2890	RX[749]	-2342	388
2891	S[1338]	-2350.5	496
2892	S[1339]	-2359	172
2893	RX[750]	-2367.5	280
2894	S[1340]	-2376	388
2895	S[1341]	-2384.5	496
2896	RX[751]	-2393	172
2897	S[1342]	-2401.5	280
2898	S[1343]	-2410	388
2899	RX[752]	-2418.5	496
2900	S[1344]	-2427	172
2901	S[1345]	-2435.5	280
2902	RX[753]	-2444	388
2903	S[1346]	-2452.5	496
2904	S[1347]	-2461	172
2905	RX[754]	-2469.5	280
2906	S[1348]	-2478	388
2907	S[1349]	-2486.5	496
2908	RX[755]	-2495	172
2909	S[1350]	-2503.5	280
2910	S[1351]	-2512	388
2911	RX[756]	-2520.5	496
2912	S[1352]	-2529	172
2913	S[1353]	-2537.5	280
2914	RX[757]	-2546	388
2915	S[1354]	-2554.5	496
2916	S[1355]	-2563	172
2917	RX[758]	-2571.5	280
2918	S[1356]	-2580	388
2919	S[1357]	-2588.5	496
2920	RX[759]	-2597	172
2921	S[1358]	-2605.5	280
2922	S[1359]	-2614	388
2923	RX[760]	-2622.5	496
2924	S[1360]	-2631	172
2925	S[1361]	-2639.5	280
2926	RX[761]	-2648	388
2927	S[1362]	-2656.5	496
2928	S[1363]	-2665	172
2929	RX[762]	2673.5	280
2930	S[1364]	-2682	388
2931	S[1365]	-2690.5	496
2932	RX[763]	-2699	172
2933	S[1366]	-2707.5	280
2934	S[1367]	-2716	388
2935	RX[764]	-2724.5	496
2936	S[1368]	-2733	172
2937	S[1369]	-2741.5	280
2938	RX[765]	-2750	388
2939	S[1370]	-2758.5	496
2940	S[1371]	-2767	172
2941	RX[766]	-2775.5	280
2942	S[1372]	-2784	388
2943	S[1373]	-2792.5	496
2944	RX[767]	-2801	172
2945	S[1374]	-2809.5	280
2946	S[1375]	-2818	388
2947	RX[768]	-2826.5	496
2948	S[1376]	-2835	172
2949	S[1377]	-2843.5	280
2950	RX[769]	-2852	388
2951	S[1378]	-2860.5	496
2952	S[1379]	-2869	172
2953	RX[770]	-2877.5	280
2954	S[1380]	-2886	388

No.	PAD Name	X	Y
2955	S[1381]	-2894.5	496
2956	RX[771]	-2903	172
2957	S[1382]	-2911.5	280
2958	S[1383]	-2920	388
2959	RX[772]	-2928.5	496
2960	S[1384]	-2937	172
2961	S[1385]	-2945.5	280
2962	RX[773]	-2954	388
2963	S[1386]	-2962.5	496
2964	S[1387]	-2971	172
2965	RX[774]	-2979.5	280
2966	S[1388]	-2988	388
2967	S[1389]	-2996.5	496
2968	RX[775]	-3005	172
2969	S[1390]	-3013.5	280
2970	S[1391]	-3022	388
2971	RX[776]	-3030.5	496
2972	S[1392]	-3039	172
2973	S[1393]	-3047.5	280
2974	RX[777]	-3056	388
2975	S[1394]	-3064.5	496
2976	S[1395]	-3073	172
2977	RX[778]	-3081.5	280
2978	S[1396]	-3090	388
2979	S[1397]	-3098.5	496
2980	RX[779]	-3107	172
2981	S[1398]	-3115.5	280
2982	S[1399]	-3124	388
2983	RX[780]	-3132.5	496
2984	S[1400]	-3141	172
2985	S[1401]	-3149.5	280
2986	RX[781]	-3158	388
2987	S[1402]	-3166.5	496
2988	S[1403]	-3175	172
2989	RX[782]	-3183.5	280
2990	S[1404]	-3192	388
2991	S[1405]	-3200.5	496
2992	RX[783]	-3209	172
2993	S[1406]	-3217.5	280
2994	S[1407]	-3226	388
2995	RX[784]	-3234.5	496
2996	S[1408]	-3243	172
2997	S[1409]	-3251.5	280
2998	RX[785]	-3260	388
2999	S[1410]	-3268.5	496
3000	S[1411]	-3277	172
3001	RX[786]	-3285.5	280
3002	S[1412]	-3294	388
3003	S[1413]	-3302.5	496
3004	RX[787]	-3311	172
3005	S[1414]	-3319.5	280
3006	S[1415]	-3328	388
3007	RX[788]	-3336.5	496
3008	S[1416]	-3345	172
3009	S[1417]	-3353.5	280
3010	RX[789]	-3362	388
3011	S[1418]	-3370.5	496
3012	S[1419]	-3379	172
3013	RX[790]	-3387.5	280
3014	S[1420]	-3396	388
3015	S[1421]	-3404.5	496
3016	RX[791]	-3413	172
3017	S[1422]	-3421.5	280
3018	S[1423]	-3430	388
3019	RX[792]	-3438.5	496
3020	S[1424]	-3447	172
3021	S[1425]	-3455.5	280
3022	RX[793]	-3464	388
3023	S[1426]	-3472.5	496
3024	S[1427]	-3481	172
3025	RX[794]	-3489.5	280
3026	S[1428]	-3498	388
3027	S[1429]	-3506.5	496
3028	RX[795]	-3515	172

No.	PAD Name	X	Y
3029	S[1430]	-3523.5	280
3030	S[1431]	-3532	388
3031	RX[796]	-3540.5	496
3032	S[1432]	-3549	172
3033	S[1433]	-3557.5	280
3034	RX[797]	-3566	388
3035	S[1434]	-3574.5	496
3036	S[1435]	-3583	172
3037	RX[798]	-3591.5	280
3038	S[1436]	-3600	388
3039	S[1437]	-3608.5	496
3040	RX[799]	-3617	172
3041	S[1438]	-3625.5	280
3042	S[1439]	-3634	388
3043	RX[800]	-3642.5	496
3044	S[1440]	-3651	172
3045	S[1441]	-3659.5	280
3046	RX[801]	-3668	388
3047	S[1442]	-3676.5	496
3048	S[1443]	-3685	172
3049	RX[802]	-3693.5	280
3050	S[1444]	-3702	388
3051	S[1445]	-3710.5	496
3052	RX[803]	-3719	172
3053	S[1446]	-3727.5	280
3054	S[1447]	-3736	388
3055	RX[804]	-3744.5	496
3056	S[1448]	-3753	172
3057	S[1449]	-3761.5	280
3058	RX[805]	-3770	388
3059	S[1450]	-3778.5	496
3060	S[1451]	-3787	172
3061	RX[806]	-3795.5	280
3062	S[1452]	-3804	388
3063	S[1453]	-3812.5	496
3064	RX[807]	-3821	172
3065	S[1454]	-3829.5	280
3066	S[1455]	-3838	388
3067	RX[808]	-3846.5	496
3068	S[1456]	-3855	172
3069	S[1457]	-3863.5	280
3070	RX[809]	-3872	388
3071	S[1458]	-3880.5	496
3072	S[1459]	-3889	172
3073	RX[810]	-3897.5	280
3074	S[1460]	-3906	388
3075	S[1461]	-3914.5	496
3076	RX[811]	-3923	172
3077	S[1462]	-3931.5	280
3078	S[1463]	-3940	388
3079	RX[812]	-3948.5	496
3080	S[1464]	-3957	172
3081	S[1465]	-3965.5	280
3082	RX[813]	-3974	388
3083	S[1466]	-3982.5	496
3084	S[1467]	-3991	172
3085	RX[814]	-3999.5	280
3086	S[1468]	-4008	388
3087	S[1469]	-4016.5	496
3088	RX[815]	-4025	172
3089	S[1470]	-4033.5	280
3090	S[1471]	-4042	388
3091	RX[816]	-4050.5	496
3092	S[1472]	-4059	172
3093	S[1473]	-4067.5	280
3094	RX[817]	-4076	388
3095	S[1474]	-4084.5	496
3096	S[1475]	-4093	172
3097	RX[818]	-4101.5	280
3098	S[1476]	-4110	388
3099	S[1477]	-4118.5	496
3100	RX[819]	-4127	172
3101	S[1478]	-4135.5	280
3102	S[1479]	-4144	388

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No.	PAD Name	X	Y
3103	RX[820]	-4152.5	496
3104	S[1480]	-4161	172
3105	S[1481]	-4169.5	280
3106	RX[821]	-4178	388
3107	S[1482]	-4186.5	496
3108	S[1483]	-4195	172
3109	RX[822]	-4203.5	280
3110	S[1484]	-4212	388
3111	S[1485]	-4220.5	496
3112	RX[823]	-4229	172
3113	S[1486]	-4237.5	280
3114	S[1487]	-4246	388
3115	RX[824]	-4254.5	496
3116	S[1488]	-4263	172
3117	S[1489]	-4271.5	280
3118	RX[825]	-4280	388
3119	S[1490]	-4288.5	496
3120	S[1491]	-4297	172
3121	RX[826]	-4305.5	280
3122	S[1492]	-4314	388
3123	S[1493]	-4322.5	496
3124	RX[827]	-4331	172
3125	S[1494]	-4339.5	280
3126	S[1495]	-4348	388
3127	RX[828]	-4356.5	496
3128	S[1496]	-4365	172
3129	S[1497]	-4373.5	280
3130	RX[829]	-4382	388
3131	S[1498]	-4390.5	496
3132	S[1499]	-4399	172
3133	RX[830]	-4407.5	280
3134	S[1500]	-4416	388
3135	S[1501]	-4424.5	496
3136	RX[831]	-4433	172
3137	S[1502]	-4441.5	280
3138	S[1503]	-4450	388
3139	RX[832]	-4458.5	496
3140	S[1504]	-4467	172
3141	S[1505]	-4475.5	280
3142	RX[833]	-4484	388
3143	S[1506]	-4492.5	496
3144	S[1507]	-4501	172
3145	RX[834]	-4509.5	280
3146	S[1508]	-4518	388
3147	S[1509]	-4526.5	496
3148	RX[835]	-4535	172
3149	S[1510]	-4543.5	280
3150	S[1511]	-4552	388
3151	RX[836]	-4560.5	496
3152	S[1512]	-4569	172
3153	S[1513]	-4577.5	280
3154	RX[837]	-4586	388
3155	S[1514]	-4594.5	496
3156	S[1515]	-4603	172
3157	RX[838]	-4611.5	280
3158	S[1516]	-4620	388
3159	S[1517]	-4628.5	496
3160	RX[839]	-4637	172
3161	S[1518]	-4645.5	280
3162	S[1519]	-4654	388
3163	RX[840]	-4662.5	496
3164	S[1520]	-4671	172
3165	S[1521]	-4679.5	280
3166	RX[841]	-4688	388
3167	S[1522]	-4696.5	496
3168	S[1523]	-4705	172
3169	RX[842]	-4713.5	280
3170	S[1524]	-4722	388
3171	S[1525]	-4730.5	496
3172	RX[843]	-4739	172
3173	S[1526]	-4747.5	280
3174	S[1527]	-4756	388
3175	RX[844]	-4764.5	496
3176	S[1528]	-4773	172

No.	PAD Name	X	Y
3177	S[1529]	-4781.5	280
3178	RX[845]	-4790	388
3179	S[1530]	-4798.5	496
3180	S[1531]	-4807	172
3181	RX[846]	-4815.5	280
3182	S[1532]	-4824	388
3183	S[1533]	-4832.5	496
3184	RX[847]	-4841	172
3185	S[1534]	-4849.5	280
3186	S[1535]	-4858	388
3187	RX[848]	-4866.5	496
3188	S[1536]	-4875	172
3189	S[1537]	-4883.5	280
3190	RX[849]	-4892	388
3191	S[1538]	-4900.5	496
3192	S[1539]	-4909	172
3193	RX[850]	-4917.5	280
3194	S[1540]	-4926	388
3195	S[1541]	-4934.5	496
3196	RX[851]	-4943	172
3197	S[1542]	-4951.5	280
3198	S[1543]	-4960	388
3199	RX[852]	-4968.5	496
3200	S[1544]	-4977	172
3201	S[1545]	-4985.5	280
3202	RX[853]	-4994	388
3203	S[1546]	-5002.5	496
3204	S[1547]	-5011	172
3205	RX[854]	-5019.5	280
3206	S[1548]	-5028	388
3207	S[1549]	-5036.5	496
3208	RX[855]	-5045	172
3209	S[1550]	-5053.5	280
3210	S[1551]	-5062	388
3211	RX[856]	-5070.5	496
3212	S[1552]	-5079	172
3213	S[1553]	-5087.5	280
3214	RX[857]	-5096	388
3215	S[1554]	-5104.5	496
3216	S[1555]	-5113	172
3217	RX[858]	-5121.5	280
3218	S[1556]	-5130	388
3219	S[1557]	-5138.5	496
3220	RX[859]	-5147	172
3221	S[1558]	-5155.5	280
3222	S[1559]	-5164	388
3223	RX[860]	-5172.5	496
3224	S[1560]	-5181	172
3225	S[1561]	-5189.5	280
3226	RX[861]	-5198	388
3227	S[1562]	-5206.5	496
3228	S[1563]	-5215	172
3229	RX[862]	-5223.5	280
3230	S[1564]	-5232	388
3231	S[1565]	-5240.5	496
3232	RX[863]	-5249	172
3233	S[1566]	-5257.5	280
3234	S[1567]	-5266	388
3235	RX[864]	-5274.5	496
3236	S[1568]	-5283	172
3237	S[1569]	-5291.5	280
3238	RX[865]	-5300	388
3239	S[1570]	-5308.5	496
3240	S[1571]	-5317	172
3241	RX[866]	-5325.5	280
3242	S[1572]	-5334	388
3243	S[1573]	-5342.5	496
3244	RX[867]	-5351	172
3245	S[1574]	-5359.5	280
3246	S[1575]	-5368	388
3247	RX[868]	-5376.5	496
3248	S[1576]	-5385	172
3249	S[1577]	-5393.5	280
3250	RX[869]	-5402	388

No.	PAD Name	X	Y
3251	S[1578]	-5410.5	496
3252	S[1579]	-5419	172
3253	RX[870]	-5427.5	280
3254	S[1580]	-5436	388
3255	S[1581]	-5444.5	496
3256	RX[871]	-5453	172
3257	S[1582]	-5461.5	280
3258	S[1583]	-5470	388
3259	RX[872]	-5478.5	496
3260	S[1584]	-5487	172
3261	S[1585]	-5495.5	280
3262	RX[873]	-5504	388
3263	S[1586]	-5512.5	496
3264	S[1587]	-5521	172
3265	RX[874]	-5529.5	280
3266	S[1588]	-5538	388
3267	S[1589]	-5546.5	496
3268	RX[875]	-5555	172
3269	S[1590]	-5563.5	280
3270	S[1591]	-5572	388
3271	RX[876]	-5580.5	496
3272	S[1592]	-5589	172
3273	S[1593]	-5597.5	280
3274	RX[877]	-5606	388
3275	S[1594]	-5614.5	496
3276	S[1595]	-5623	172
3277	RX[878]	-5631.5	280
3278	S[1596]	-5640	388
3279	S[1597]	-5648.5	496
3280	RX[879]	-5657	172
3281	S[1598]	-5665.5	280
3282	S[1599]	-5674	388
3283	RX[880]	-5682.5	496
3284	S[1600]	-5691	172
3285	S[1601]	-5699.5	280
3286	RX[881]	-5708	388
3287	S[1602]	-5716.5	496
3288	S[1603]	-5725	172
3289	RX[882]	-5733.5	280
3290	S[1604]	-5742	388
3291	S[1605]	-5750.5	496
3292	RX[883]	-5759	172
3293	S[1606]	-5767.5	280
3294	S[1607]	-5776	388
3295	RX[884]	-5784.5	496
3296	S[1608]	-5793	172
3297	S[1609]	-5801.5	280
3298	RX[885]	-5810	388
3299	S[1610]	-5818.5	496
3300	S[1611]	-5827	172
3301	RX[886]	-5835.5	280
3302	S[1612]	-5844	388
3303	S[1613]	-5852.5	496
3304	RX[887]	-5861	172
3305	S[1614]	-5869.5	280
3306	S[1615]	-5878	388
3307	RX[888]	-5886.5	496
3308	S[1616]	-5895	172
3309	S[1617]	-5903.5	280
3310	RX[889]	-5912	388
3311	S[1618]	-5920.5	496
3312	S[1619]	-5929	172
3313	RX[890]	-5937.5	280
3314	S[1620]	-5946	388
3315	S[1621]	-5954.5	496
3316	RX[891]	-5963	172
3317	S[1622]	-5971.5	280
3318	S[1623]	-5980	388
3319	RX[892]	-5988.5	496
3320	S[1624]	-5997	172
3321	S[1625]	-6005.5	280
3322	RX[893]	-6014	388
3323	S[1626]	-6022.5	496
3324	S[1627]	-6031	172

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No.	PAD Name	X	Y
3325	RX[894]	-6039.5	280
3326	S[1628]	-6048	388
3327	S[1629]	-6056.5	496
3328	RX[895]	-6065	172
3329	S[1630]	-6073.5	280
3330	S[1631]	-6082	388
3331	RX[896]	-6090.5	496
3332	S[1632]	-6099	172
3333	S[1633]	-6107.5	280
3334	RX[897]	-6116	388
3335	S[1634]	-6124.5	496
3336	S[1635]	-6133	172
3337	RX[898]	-6141.5	280
3338	S[1636]	-6150	388
3339	S[1637]	-6158.5	496
3340	RX[899]	-6167	172
3341	S[1638]	-6175.5	280
3342	S[1639]	-6184	388
3343	RX[900]	-6192.5	496
3344	S[1640]	-6201	172
3345	S[1641]	-6209.5	280
3346	RX[901]	-6218	388
3347	S[1642]	-6226.5	496
3348	S[1643]	-6235	172
3349	RX[902]	-6243.5	280
3350	S[1644]	-6252	388
3351	S[1645]	-6260.5	496
3352	RX[903]	-6269	172
3353	S[1646]	-6277.5	280
3354	S[1647]	-6286	388
3355	RX[904]	-6294.5	496
3356	S[1648]	-6303	172
3357	S[1649]	-6311.5	280
3358	RX[905]	-6320	388
3359	S[1650]	-6328.5	496
3360	S[1651]	-6337	172
3361	RX[906]	-6345.5	280
3362	S[1652]	-6354	388
3363	S[1653]	-6362.5	496
3364	RX[907]	-6371	172
3365	S[1654]	-6379.5	280
3366	S[1655]	-6388	388
3367	RX[908]	-6396.5	496
3368	S[1656]	-6405	172
3369	S[1657]	-6413.5	280
3370	RX[909]	-6422	388
3371	S[1658]	-6430.5	496
3372	S[1659]	-6439	172
3373	RX[910]	-6447.5	280
3374	S[1660]	-6456	388
3375	S[1661]	-6464.5	496
3376	RX[911]	-6473	172
3377	S[1662]	-6481.5	280
3378	S[1663]	-6490	388
3379	RX[912]	-6498.5	496
3380	S[1664]	-6507	172
3381	S[1665]	-6515.5	280
3382	RX[913]	-6524	388
3383	S[1666]	-6532.5	496
3384	S[1667]	-6541	172
3385	RX[914]	-6549.5	280
3386	S[1668]	-6558	388
3387	S[1669]	-6566.5	496
3388	RX[915]	-6575	172
3389	S[1670]	-6583.5	280
3390	S[1671]	-6592	388
3391	RX[916]	-6600.5	496
3392	S[1672]	-6609	172
3393	S[1673]	-6617.5	280
3394	RX[917]	-6626	388
3395	S[1674]	-6634.5	496
3396	S[1675]	-6643	172
3397	RX[918]	-6651.5	280
3398	S[1676]	-6660	388

No.	PAD Name	X	Y
3399	S[1677]	-6668.5	496
3400	RX[919]	-6677	172
3401	S[1678]	-6685.5	280
3402	S[1679]	-6694	388
3403	RX[920]	-6702.5	496
3404	S[1680]	-6711	172
3405	S[1681]	-6719.5	280
3406	RX[921]	-6728	388
3407	S[1682]	-6736.5	496
3408	S[1683]	-6745	172
3409	RX[922]	-6753.5	280
3410	S[1684]	-6762	388
3411	S[1685]	-6770.5	496
3412	RX[923]	-6779	172
3413	S[1686]	-6787.5	280
3414	S[1687]	-6796	388
3415	RX[924]	-6804.5	496
3416	S[1688]	-6813	172
3417	S[1689]	-6821.5	280
3418	RX[925]	-6830	388
3419	S[1690]	-6838.5	496
3420	S[1691]	-6847	172
3421	RX[926]	-6855.5	280
3422	S[1692]	-6864	388
3423	S[1693]	-6872.5	496
3424	RX[927]	-6881	172
3425	S[1694]	-6889.5	280
3426	S[1695]	-6898	388
3427	RX[928]	-6906.5	496
3428	S[1696]	-6915	172
3429	S[1697]	-6923.5	280
3430	RX[929]	-6932	388
3431	S[1698]	-6940.5	496
3432	S[1699]	-6949	172
3433	RX[930]	-6957.5	280
3434	S[1700]	-6966	388
3435	S[1701]	-6974.5	496
3436	RX[931]	-6983	172
3437	S[1702]	-6991.5	280
3438	S[1703]	-7000	388
3439	RX[932]	-7008.5	496
3440	S[1704]	-7017	172
3441	S[1705]	-7025.5	280
3442	RX[933]	-7034	388
3443	S[1706]	-7042.5	496
3444	S[1707]	-7051	172
3445	RX[934]	-7059.5	280
3446	S[1708]	-7068	388
3447	S[1709]	-7076.5	496
3448	RX[935]	-7085	172
3449	S[1710]	-7093.5	280
3450	S[1711]	-7102	388
3451	RX[936]	-7110.5	496
3452	S[1712]	-7119	172
3453	S[1713]	-7127.5	280
3454	RX[937]	-7136	388
3455	S[1714]	-7144.5	496
3456	S[1715]	-7153	172
3457	RX[938]	-7161.5	280
3458	S[1716]	-7170	388
3459	S[1717]	-7178.5	496
3460	RX[939]	-7187	172
3461	S[1718]	-7195.5	280
3462	S[1719]	-7204	388
3463	RX[940]	-7212.5	496
3464	S[1720]	-7221	172
3465	S[1721]	-7229.5	280
3466	RX[941]	-7238	388
3467	S[1722]	-7246.5	496
3468	S[1723]	-7255	172
3469	RX[942]	-7263.5	280
3470	S[1724]	-7272	388
3471	S[1725]	-7280.5	496
3472	RX[943]	-7289	172

No.	PAD Name	X	Y
3473	S[1726]	-7297.5	280
3474	S[1727]	-7306	388
3475	RX[944]	-7314.5	496
3476	S[1728]	-7323	172
3477	S[1729]	-7331.5	280
3478	RX[945]	-7340	388
3479	S[1730]	-7348.5	496
3480	S[1731]	-7357	172
3481	RX[946]	-7365.5	280
3482	S[1732]	-7374	388
3483	S[1733]	-7382.5	496
3484	RX[947]	-7391	172
3485	S[1734]	-7399.5	280
3486	S[1735]	-7408	388
3487	RX[948]	-7416.5	496
3488	S[1736]	-7425	172
3489	S[1737]	-7433.5	280
3490	RX[949]	-7442	388
3491	S[1738]	-7450.5	496
3492	S[1739]	-7459	172
3493	RX[950]	-7467.5	280
3494	S[1740]	-7476	388
3495	S[1741]	-7484.5	496
3496	RX[951]	-7493	172
3497	S[1742]	-7501.5	280
3498	S[1743]	-7510	388
3499	RX[952]	-7518.5	496
3500	S[1744]	-7527	172
3501	S[1745]	-7535.5	280
3502	RX[953]	-7544	388
3503	S[1746]	-7552.5	496
3504	S[1747]	-7561	172
3505	RX[954]	-7569.5	280
3506	S[1748]	-7578	388
3507	S[1749]	-7586.5	496
3508	RX[955]	-7595	172
3509	S[1750]	-7603.5	280
3510	S[1751]	-7612	388
3511	RX[956]	-7620.5	496
3512	S[1752]	-7629	172
3513	S[1753]	-7637.5	280
3514	RX[957]	-7646	388
3515	S[1754]	-7654.5	496
3516	S[1755]	-7663	172
3517	RX[958]	-7671.5	280
3518	S[1756]	-7680	388
3519	S[1757]	-7688.5	496
3520	RX[959]	-7697	172
3521	S[1758]	-7705.5	280
3522	S[1759]	-7714	388
3523	RX[960]	-7722.5	496
3524	S[1760]	-7731	172
3525	S[1761]	-7739.5	280
3526	RX[961]	-7748	388
3527	S[1762]	-7756.5	496
3528	S[1763]	-7765	172
3529	RX[962]	-7773.5	280
3530	S[1764]	-7782	388
3531	S[1765]	-7790.5	496
3532	RX[963]	-7799	172
3533	S[1766]	-7807.5	280
3534	S[1767]	-7816	388
3535	RX[964]	-7824.5	496
3536	S[1768]	-7833	172
3537	S[1769]	-7841.5	280
3538	RX[965]	-7850	388
3539	S[1770]	-7858.5	496
3540	S[1771]	-7867	172
3541	RX[966]	-7875.5	280
3542	S[1772]	-7884	388
3543	S[1773]	-7892.5	496
3544	RX[967]	-7901	172
3545	S[1774]	-7909.5	280
3546	S[1775]	-7918	388

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No.	PAD Name	X	Y
3547	RX[968]	-7926.5	496
3548	S[1776]	-7935	172
3549	S[1777]	-7943.5	280
3550	RX[969]	-7952	388
3551	S[1778]	-7960.5	496
3552	S[1779]	-7969	172
3553	RX[970]	-7977.5	280
3554	S[1780]	-7986	388
3555	S[1781]	-7994.5	496
3556	RX[971]	-8003	172
3557	S[1782]	-8011.5	280
3558	S[1783]	-8020	388
3559	RX[972]	-8028.5	496
3560	S[1784]	-8037	172
3561	S[1785]	-8045.5	280
3562	RX[973]	-8054	388
3563	S[1786]	-8062.5	496
3564	S[1787]	-8071	172
3565	RX[974]	-8079.5	280
3566	S[1788]	-8088	388
3567	S[1789]	-8096.5	496
3568	RX[975]	-8105	172
3569	S[1790]	-8113.5	280
3570	S[1791]	-8122	388
3571	RX[976]	-8130.5	496
3572	S[1792]	-8139	172
3573	S[1793]	-8147.5	280
3574	RX[977]	-8156	388
3575	S[1794]	-8164.5	496
3576	S[1795]	-8173	172
3577	RX[978]	-8181.5	280
3578	S[1796]	-8190	388
3579	S[1797]	-8198.5	496
3580	RX[979]	-8207	172
3581	S[1798]	-8215.5	280
3582	S[1799]	-8224	388
3583	RX[980]	-8232.5	496
3584	S[1800]	-8241	172
3585	S[1801]	-8249.5	280
3586	RX[981]	-8258	388
3587	S[1802]	-8266.5	496
3588	S[1803]	-8275	172
3589	RX[982]	-8283.5	280
3590	S[1804]	-8292	388
3591	S[1805]	-8300.5	496
3592	RX[983]	-8309	172
3593	S[1806]	-8317.5	280
3594	S[1807]	-8326	388
3595	RX[984]	-8334.5	496
3596	S[1808]	-8343	172
3597	S[1809]	-8351.5	280
3598	RX[985]	-8360	388
3599	S[1810]	-8368.5	496
3600	S[1811]	-8377	172
3601	RX[986]	-8385.5	280
3602	S[1812]	-8394	388
3603	S[1813]	-8402.5	496
3604	RX[987]	-8411	172
3605	S[1814]	-8419.5	280
3606	S[1815]	-8428	388
3607	RX[988]	-8436.5	496
3608	S[1816]	-8445	172
3609	S[1817]	-8453.5	280
3610	RX[989]	-8462	388
3611	S[1818]	-8470.5	496
3612	S[1819]	-8479	172
3613	RX[990]	-8487.5	280
3614	S[1820]	-8496	388
3615	S[1821]	-8504.5	496
3616	RX[991]	-8513	172
3617	S[1822]	-8521.5	280
3618	S[1823]	-8530	388
3619	RX[992]	-8538.5	496
3620	S[1824]	-8547	172

No.	PAD Name	X	Y
3621	S[1825]	-8555.5	280
3622	RX[993]	-8564	388
3623	S[1826]	-8572.5	496
3624	S[1827]	-8581	172
3625	RX[994]	-8589.5	280
3626	S[1828]	-8598	388
3627	S[1829]	-8606.5	496
3628	RX[995]	-8615	172
3629	S[1830]	-8623.5	280
3630	S[1831]	-8632	388
3631	RX[996]	-8640.5	496
3632	S[1832]	-8649	172
3633	S[1833]	-8657.5	280
3634	RX[997]	-8666	388
3635	S[1834]	-8674.5	496
3636	S[1835]	-8683	172
3637	RX[998]	-8691.5	280
3638	S[1836]	-8700	388
3639	S[1837]	-8708.5	496
3640	RX[999]	-8717	172
3641	S[1838]	-8725.5	280
3642	S[1839]	-8734	388
3643	RX[1000]	-8742.5	496
3644	S[1840]	-8751	172
3645	S[1841]	-8759.5	280
3646	RX[1001]	-8768	388
3647	S[1842]	-8776.5	496
3648	S[1843]	-8785	172
3649	RX[1002]	-8793.5	280
3650	S[1844]	-8802	388
3651	S[1845]	-8810.5	496
3652	RX[1003]	-8819	172
3653	S[1846]	-8827.5	280
3654	S[1847]	-8836	388
3655	RX[1004]	-8844.5	496
3656	S[1848]	-8853	172
3657	S[1849]	-8861.5	280
3658	RX[1005]	-8870	388
3659	S[1850]	-8878.5	496
3660	S[1851]	-8887	172
3661	RX[1006]	-8895.5	280
3662	S[1852]	-8904	388
3663	S[1853]	-8912.5	496
3664	RX[1007]	-8921	172
3665	S[1854]	-8929.5	280
3666	S[1855]	-8938	388
3667	RX[1008]	-8946.5	496
3668	S[1856]	-8955	172
3669	S[1857]	-8963.5	280
3670	RX[1009]	-8972	388
3671	S[1858]	-8980.5	496
3672	S[1859]	-8989	172
3673	RX[1010]	-8997.5	280
3674	S[1860]	-9006	388
3675	S[1861]	-9014.5	496
3676	RX[1011]	-9023	172
3677	S[1862]	-9031.5	280
3678	S[1863]	-9040	388
3679	RX[1012]	-9048.5	496
3680	S[1864]	-9057	172
3681	S[1865]	-9065.5	280
3682	RX[1013]	-9074	388
3683	S[1866]	-9082.5	496
3684	S[1867]	-9091	172
3685	RX[1014]	-9099.5	280
3686	S[1868]	-9108	388
3687	S[1869]	-9116.5	496
3688	RX[1015]	-9125	172
3689	S[1870]	-9133.5	280
3690	S[1871]	-9142	388
3691	RX[1016]	-9150.5	496
3692	S[1872]	-9159	172
3693	S[1873]	-9167.5	280
3694	RX[1017]	-9176	388

No.	PAD Name	X	Y
3695	S[1874]	-9184.5	496
3696	S[1875]	-9193	172
3697	RX[1018]	-9201.5	280
3698	S[1876]	-9210	388
3699	S[1877]	-9218.5	496
3700	RX[1019]	-9227	172
3701	S[1878]	-9235.5	280
3702	S[1879]	-9244	388
3703	RX[1020]	-9252.5	496
3704	S[1880]	-9261	172
3705	S[1881]	-9269.5	280
3706	RX[1021]	-9278	388
3707	S[1882]	-9286.5	496
3708	S[1883]	-9295	172
3709	RX[1022]	-9303.5	280
3710	S[1884]	-9312	388
3711	S[1885]	-9320.5	496
3712	RX[1023]	-9329	172
3713	S[1886]	-9337.5	280
3714	S[1887]	-9346	388
3715	RX[1024]	-9354.5	496
3716	S[1888]	-9363	172
3717	S[1889]	-9371.5	280
3718	RX[1025]	-9380	388
3719	S[1890]	-9388.5	496
3720	S[1891]	-9397	172
3721	RX[1026]	-9405.5	280
3722	S[1892]	-9414	388
3723	S[1893]	-9422.5	496
3724	RX[1027]	-9431	172
3725	S[1894]	-9439.5	280
3726	S[1895]	-9448	388
3727	RX[1028]	-9456.5	496
3728	S[1896]	-9465	172
3729	S[1897]	-9473.5	280
3730	RX[1029]	-9482	388
3731	S[1898]	-9490.5	496
3732	S[1899]	-9499	172
3733	RX[1030]	-9507.5	280
3734	S[1900]	-9516	388
3735	S[1901]	-9524.5	496
3736	RX[1031]	-9533	172
3737	S[1902]	-9541.5	280
3738	S[1903]	-9550	388
3739	RX[1032]	-9558.5	496
3740	S[1904]	-9567	172
3741	S[1905]	-9575.5	280
3742	RX[1033]	-9584	388
3743	S[1906]	-9592.5	496
3744	S[1907]	-9601	172
3745	RX[1034]	-9609.5	280
3746	S[1908]	-9618	388
3747	S[1909]	-9626.5	496
3748	RX[1035]	-9635	172
3749	S[1910]	-9643.5	280
3750	S[1911]	-9652	388
3751	RX[1036]	-9660.5	496
3752	S[1912]	-9669	172
3753	S[1913]	-9677.5	280
3754	RX[1037]	-9686	388
3755	S[1914]	-9694.5	496
3756	S[1915]	-9703	172
3757	RX[1038]	-9711.5	280
3758	S[1916]	-9720	388
3759	S[1917]	-9728.5	496
3760	RX[1039]	-9737	172
3761	S[1918]	-9745.5	280
3762	S[1919]	-9754	388
3763	RX[1040]	-9762.5	496
3764	S[1920]	-9771	172
3765	S[1921]	-9779.5	280
3766	RX[1041]	-9788	388
3767	S[1922]	-9796.5	496
3768	S[1923]	-9805	172

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No.	PAD Name	X	Y
3769	RX[1042]	-9813.5	280
3770	S[1924]	-9822	388
3771	S[1925]	-9830.5	496
3772	RX[1043]	-9839	172
3773	S[1926]	-9847.5	280
3774	S[1927]	-9856	388
3775	RX[1044]	-9864.5	496
3776	S[1928]	-9873	172
3777	S[1929]	-9881.5	280
3778	RX[1045]	-9890	388
3779	S[1930]	-9898.5	496
3780	S[1931]	-9907	172
3781	RX[1046]	-9915.5	280
3782	S[1932]	-9924	388
3783	S[1933]	-9932.5	496
3784	RX[1047]	-9941	172
3785	S[1934]	-9949.5	280
3786	S[1935]	-9958	388
3787	RX[1048]	-9966.5	496
3788	S[1936]	-9975	172
3789	S[1937]	-9983.5	280
3790	RX[1049]	-9992	388
3791	S[1938]	-10000.5	496
3792	S[1939]	-10009	172
3793	RX[1050]	-10017.5	280
3794	S[1940]	-10026	388
3795	S[1941]	-10034.5	496
3796	RX[1051]	-10043	172
3797	S[1942]	-10051.5	280
3798	S[1943]	-10060	388
3799	RX[1052]	-10068.5	496
3800	S[1944]	-10077	172
3801	S[1945]	-10085.5	280
3802	RX[1053]	-10094	388
3803	S[1946]	-10102.5	496
3804	S[1947]	-10111	172
3805	RX[1054]	-10119.5	280
3806	S[1948]	-10128	388
3807	S[1949]	-10136.5	496
3808	RX[1055]	-10145	172
3809	S[1950]	-10153.5	280
3810	S[1951]	-10162	388
3811	RX[1056]	-10170.5	496
3812	S[1952]	-10179	172
3813	S[1953]	-10187.5	280
3814	RX[1057]	-10196	388
3815	S[1954]	-10204.5	496
3816	S[1955]	-10213	172
3817	RX[1058]	-10221.5	280
3818	S[1956]	-10230	388
3819	S[1957]	-10238.5	496
3820	RX[1059]	-10247	172
3821	S[1958]	-10255.5	280
3822	S[1959]	-10264	388
3823	RX[1060]	-10272.5	496
3824	S[1960]	-10281	172
3825	S[1961]	-10289.5	280
3826	RX[1061]	-10298	388
3827	S[1962]	-10306.5	496
3828	S[1963]	-10315	172
3829	RX[1062]	-10323.5	280
3830	S[1964]	-10332	388
3831	S[1965]	-10340.5	496
3832	RX[1063]	-10349	172
3833	S[1966]	-10357.5	280
3834	S[1967]	-10366	388
3835	RX[1064]	-10374.5	496
3836	S[1968]	-10383	172
3837	S[1969]	-10391.5	280
3838	RX[1065]	-10400	388
3839	S[1970]	-10408.5	496
3840	S[1971]	-10417	172
3841	RX[1066]	-10425.5	280
3842	S[1972]	-10434	388

No.	PAD Name	X	Y
3843	S[1973]	-10442.5	496
3844	RX[1067]	-10451	172
3845	S[1974]	-10459.5	280
3846	S[1975]	-10468	388
3847	RX[1068]	-10476.5	496
3848	S[1976]	-10485	172
3849	S[1977]	-10493.5	280
3850	RX[1069]	-10502	388
3851	S[1978]	-10510.5	496
3852	S[1979]	-10519	172
3853	RX[1070]	-10527.5	280
3854	S[1980]	-10536	388
3855	S[1981]	-10544.5	496
3856	RX[1071]	-10553	172
3857	S[1982]	-10561.5	280
3858	S[1983]	-10570	388
3859	RX[1072]	-10578.5	496
3860	S[1984]	-10587	172
3861	S[1985]	-10595.5	280
3862	RX[1073]	-10604	388
3863	S[1986]	-10612.5	496
3864	S[1987]	-10621	172
3865	RX[1074]	-10629.5	280
3866	S[1988]	-10638	388
3867	S[1989]	-10646.5	496
3868	RX[1075]	-10655	172
3869	S[1990]	-10663.5	280
3870	S[1991]	-10672	388
3871	RX[1076]	-10680.5	496
3872	S[1992]	-10689	172
3873	S[1993]	-10697.5	280
3874	RX[1077]	-10706	388
3875	S[1994]	-10714.5	496
3876	S[1995]	-10723	172
3877	RX[1078]	-10731.5	280
3878	S[1996]	-10740	388
3879	S[1997]	-10748.5	496
3880	RX[1079]	-10757	172
3881	S[1998]	-10765.5	280
3882	S[1999]	-10774	388
3883	RX[1080]	-10782.5	496
3884	S[2000]	-10791	172
3885	S[2001]	-10799.5	280
3886	RX[1081]	-10808	388
3887	S[2002]	-10816.5	496
3888	S[2003]	-10825	172
3889	RX[1082]	-10833.5	280
3890	S[2004]	-10842	388
3891	S[2005]	-10850.5	496
3892	RX[1083]	-10859	172
3893	S[2006]	-10867.5	280
3894	S[2007]	-10876	388
3895	RX[1084]	-10884.5	496
3896	S[2008]	-10893	172
3897	S[2009]	-10901.5	280
3898	RX[1085]	-10910	388
3899	S[2010]	-10918.5	496
3900	S[2011]	-10927	172
3901	RX[1086]	-10935.5	280
3902	S[2012]	-10944	388
3903	S[2013]	-10952.5	496
3904	RX[1087]	-10961	172
3905	S[2014]	-10969.5	280
3906	S[2015]	-10978	388
3907	RX[1088]	-10986.5	496
3908	S[2016]	-10995	169.2
3909	S[2017]	-11003.5	277.2
3910	RX[1089]	-11012	385.2
3911	S[2018]	-11020.5	493.2
3912	S[2019]	-11029	166.4
3913	RX[1090]	-11037.5	274.4
3914	S[2020]	-11046	382.4
3915	S[2021]	-11054.5	490.4
3916	RX[1091]	-11063	163.6

No.	PAD Name	X	Y
3917	S[2022]	-11071.5	271.6
3918	S[2023]	-11080	379.6
3919	RX[1092]	-11088.5	487.6
3920	S[2024]	-11097	160.8
3921	S[2025]	-11105.5	268.8
3922	RX[1093]	-11114	376.8
3923	S[2026]	-11122.5	484.8
3924	S[2027]	-11131	158
3925	RX[1094]	-11139.5	266
3926	S[2028]	-11148	374
3927	S[2029]	-11156.5	482
3928	RX[1095]	-11165	155.2
3929	S[2030]	-11173.5	263.2
3930	S[2031]	-11182	371.2
3931	RX[1096]	-11190.5	479.2
3932	S[2032]	-11199	152.4
3933	S[2033]	-11207.5	260.4
3934	RX[1097]	-11216	368.4
3935	S[2034]	-11224.5	476.4
3936	S[2035]	-11233	149.6
3937	RX[1098]	-11241.5	257.6
3938	S[2036]	-11250	365.6
3939	S[2037]	-11258.5	473.6
3940	RX[1099]	-11267	146.8
3941	S[2038]	-11275.5	254.8
3942	S[2039]	-11284	362.8
3943	RX[1100]	-11292.5	470.8
3944	S[2040]	-11301	144
3945	S[2041]	-11309.5	252
3946	RX[1101]	-11318	360
3947	S[2042]	-11326.5	468
3948	S[2043]	-11335	141.2
3949	RX[1102]	-11343.5	249.2
3950	S[2044]	-11352	357.2
3951	S[2045]	-11360.5	465.2
3952	RX[1103]	-11369	138.4
3953	S[2046]	-11377.5	246.4
3954	S[2047]	-11386	354.4
3955	RX[1104]	-11394.5	462.4
3956	S[2048]	-11403	135.6
3957	S[2049]	-11411.5	243.6
3958	RX[1105]	-11420	351.6
3959	S[2050]	-11428.5	459.6
3960	S[2051]	-11437	132.8
3961	RX[1106]	-11445.5	240.8
3962	S[2052]	-11454	348.8
3963	S[2053]	-11462.5	456.8
3964	RX[1107]	-11471	130
3965	S[2054]	-11479.5	238
3966	S[2055]	-11488	346
3967	RX[1108]	-11496.5	454
3968	S[2056]	-11505	127.2
3969	S[2057]	-11513.5	235.2
3970	RX[1109]	-11522	343.2
3971	S[2058]	-11530.5	451.2
3972	S[2059]	-11539	124.4
3973	RX[1110]	-11547.5	232.4
3974	S[2060]	-11556	340.4
3975	S[2061]	-11564.5	448.4
3976	RX[1111]	-11573	121.6
3977	S[2062]	-11581.5	229.6
3978	S[2063]	-11590	337.6
3979	RX[1112]	-11598.5	445.6
3980	S[2064]	-11607	118.8
3981	S[2065]	-11615.5	226.8
3982	RX[1113]	-11624	334.8
3983	S[2066]	-11632.5	442.8
3984	S[2067]	-11641	116
3985	RX[1114]	-11649.5	224
3986	S[2068]	-11658	332
3987	S[2069]	-11666.5	440
3988	RX[1115]	-11675	113.2
3989	S[2070]	-11683.5	221.2
3990	S[2071]	-11692	329.2

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No.	PAD Name	X	Y
3991	RX[1116]	-11700.5	437.2
3992	S[2072]	-11709	110.4
3993	S[2073]	-11717.5	218.4
3994	RX[1117]	-11726	326.4
3995	S[2074]	-11734.5	434.4
3996	S[2075]	-11743	107.6
3997	RX[1118]	-11751.5	215.6
3998	S[2076]	-11760	323.6
3999	S[2077]	-11768.5	431.6
4000	RX[1119]	-11777	104.8
4001	S[2078]	-11785.5	212.8
4002	S[2079]	-11794	320.8
4003	RX[1120]	-11802.5	428.8
4004	S[2080]	-11811	102
4005	S[2081]	-11819.5	210
4006	RX[1121]	-11828	318
4007	S[2082]	-11836.5	426
4008	S[2083]	-11845	99.2
4009	RX[1122]	-11853.5	207.2
4010	S[2084]	-11862	315.2
4011	S[2085]	-11870.5	423.2
4012	RX[1123]	-11879	96.4
4013	S[2086]	-11887.5	204.4
4014	S[2087]	-11896	312.4
4015	RX[1124]	-11904.5	420.4
4016	S[2088]	-11913	93.6
4017	S[2089]	-11921.5	201.6
4018	RX[1125]	-11930	309.6
4019	S[2090]	-11938.5	417.6
4020	S[2091]	-11947	90.8
4021	RX[1126]	-11955.5	198.8
4022	S[2092]	-11964	306.8
4023	S[2093]	-11972.5	414.8
4024	RX[1127]	-11981	88
4025	S[2094]	-11989.5	196
4026	S[2095]	-11998	304
4027	RX[1128]	-12006.5	412
4028	S[2096]	-12015	85.2
4029	S[2097]	-12023.5	193.2
4030	RX[1129]	-12032	301.2
4031	S[2098]	-12040.5	409.2
4032	S[2099]	-12049	82.4
4033	RX[1130]	-12057.5	190.4
4034	S[2100]	-12066	298.4
4035	S[2101]	-12074.5	406.4
4036	RX[1131]	-12083	79.6
4037	S[2102]	-12091.5	187.6
4038	S[2103]	-12100	295.6
4039	RX[1132]	-12108.5	403.6
4040	S[2104]	-12117	76.8
4041	S[2105]	-12125.5	184.8
4042	RX[1133]	-12134	292.8
4043	S[2106]	-12142.5	400.8
4044	S[2107]	-12151	74
4045	RX[1134]	-12159.5	182
4046	S[2108]	-12168	290
4047	S[2109]	-12176.5	398
4048	RX[1135]	-12185	71.2
4049	S[2110]	-12193.5	179.2
4050	S[2111]	-12202	287.2
4051	RX[1136]	-12210.5	395.2
4052	S[2112]	-12219	68.4
4053	S[2113]	-12227.5	176.4
4054	RX[1137]	-12236	284.4
4055	S[2114]	-12244.5	392.4
4056	S[2115]	-12253	65.6
4057	RX[1138]	-12261.5	173.6
4058	S[2116]	-12270	281.6
4059	S[2117]	-12278.5	389.6
4060	RX[1139]	-12287	62.8
4061	S[2118]	-12295.5	170.8
4062	S[2119]	-12304	278.8
4063	RX[1140]	-12312.5	386.8
4064	S[2120]	-12321	60
4065	S[2121]	-12329.5	168
4066	RX[1141]	-12338	276
4067	S[2122]	-12346.5	384
4068	S[2123]	-12355	57.2
4069	RX[1142]	-12363.5	165.2
4070	S[2124]	-12372	273.2
4071	S[2125]	-12380.5	381.2
4072	RX[1143]	-12389	54.4
4073	S[2126]	-12397.5	162.4
4074	S[2127]	-12406	270.4
4075	RX[1144]	-12414.5	378.4
4076	S[2128]	-12423	51.6
4077	S[2129]	-12431.5	159.6
4078	RX[1145]	-12440	267.6
4079	S[2130]	-12448.5	375.6
4080	S[2131]	-12457	48.8
4081	RX[1146]	-12465.5	156.8
4082	S[2132]	-12474	264.8
4083	S[2133]	-12482.5	372.8
4084	RX[1147]	-12491	46
4085	S[2134]	-12499.5	154
4086	S[2135]	-12508	262
4087	RX[1148]	-12516.5	370
4088	S[2136]	-12525	43.2
4089	S[2137]	-12533.5	151.2
4090	RX[1149]	-12542	259.2
4091	S[2138]	-12550.5	367.2
4092	S[2139]	-12559	40.4
4093	RX[1150]	-12567.5	148.4
4094	S[2140]	-12576	256.4
4095	S[2141]	-12584.5	364.4
4096	RX[1151]	-12593	37.6
4097	S[2142]	-12601.5	145.6
4098	S[2143]	-12610	253.6
4099	RX[1152]	-12618.5	361.6
4100	S[2144]	-12627	34.8
4101	S[2145]	-12635.5	142.8
4102	RX[1153]	-12644	250.8
4103	S[2146]	-12652.5	358.8
4104	S[2147]	-12661	32
4105	RX[1154]	-12669.5	140
4106	S[2148]	-12678	248
4107	S[2149]	-12686.5	356
4108	RX[1155]	-12695	29.2
4109	S[2150]	-12703.5	137.2
4110	S[2151]	-12712	245.2
4111	RX[1156]	-12720.5	353.2
4112	S[2152]	-12729	26.4
4113	S[2153]	-12737.5	134.4
4114	RX[1157]	-12746	242.4
4115	S[2154]	-12754.5	350.4
4116	S[2155]	-12763	23.6
4117	RX[1158]	-12771.5	131.6
4118	S[2156]	-12780	239.6
4119	S[2157]	-12788.5	347.6
4120	RX[1159]	-12797	20.8
4121	S[2158]	-12805.5	128.8
4122	S[2159]	-12814	236.8
4123	RX[1160]	-12822.5	344.8
4124	S[2160]	-12831	18
4125	S[2161]	-12839.5	126
4126	RX[1161]	-12848	234
4127	S[2162]	-12856.5	342
4128	S[2163]	-12865	15.2
4129	RX[1162]	-12873.5	123.2
4130	S[2164]	-12882	231.2
4131	S[2165]	-12890.5	339.2
4132	RX[1163]	-12899	12.4
4133	S[2166]	-12907.5	120.4
4134	S[2167]	-12916	228.4
4135	RX[1164]	-12924.5	336.4
4136	S[2168]	-12933	9.6
4137	S[2169]	-12941.5	117.6
4138	RX[1165]	-12950	225.6
4139	S[2170]	-12958.5	333.6
4140	S[2171]	-12967	6.8
4141	RX[1166]	-12975.5	114.8
4142	S[2172]	-12984	222.8
4143	S[2173]	-12992.5	330.8
4144	RX[1167]	-13001	4
4145	S[2174]	-13009.5	112
4146	S[2175]	-13018	220
4147	RX[1168]	-13026.5	328
4148	S[2176]	-13035	1.2
4149	S[2177]	-13043.5	109.2
4150	RX[1169]	-13052	217.2
4151	S[2178]	-13060.5	325.2
4152	S[2179]	-13069	-1.6
4153	RX[1170]	-13077.5	106.4
4154	S[2180]	-13086	214.4
4155	S[2181]	-13094.5	322.4
4156	RX[1171]	-13103	-4.4
4157	S[2182]	-13111.5	103.6
4158	S[2183]	-13120	211.6
4159	RX[1172]	-13128.5	319.6
4160	S[2184]	-13137	-7.2
4161	S[2185]	-13145.5	100.8
4162	RX[1173]	-13154	208.8
4163	S[2186]	-13162.5	316.8
4164	S[2187]	-13171	-10
4165	RX[1174]	-13179.5	98
4166	S[2188]	-13188	206
4167	S[2189]	-13196.5	314
4168	RX[1175]	-13205	-12.8
4169	S[2190]	-13213.5	95.2
4170	S[2191]	-13222	203.2
4171	RX[1176]	-13230.5	311.2
4172	S[2192]	-13239	-15.6
4173	S[2193]	-13247.5	92.4
4174	RX[1177]	-13256	200.4
4175	S[2194]	-13264.5	308.4
4176	S[2195]	-13273	-18.4
4177	RX[1178]	-13281.5	89.6
4178	S[2196]	-13290	197.6
4179	S[2197]	-13298.5	305.6
4180	RX[1179]	-13307	-21.2
4181	S[2198]	-13315.5	86.8
4182	S[2199]	-13324	194.8
4183	RX[1180]	-13332.5	302.8
4184	S[2200]	-13341	-24
4185	S[2201]	-13349.5	84
4186	RX[1181]	-13358	192
4187	S[2202]	-13366.5	300
4188	S[2203]	-13375	-26.8
4189	RX[1182]	-13383.5	81.2
4190	S[2204]	-13392	189.2
4191	S[2205]	-13400.5	297.2
4192	RX[1183]	-13409	-29.6
4193	S[2206]	-13417.5	78.4
4194	S[2207]	-13426	186.4
4195	RX[1184]	-13434.5	294.4
4196	S[2208]	-13443	-32.4
4197	S[2209]	-13451.5	75.6
4198	RX[1185]	-13460	183.6
4199	S[2210]	-13468.5	291.6
4200	S[2211]	-13477	-35.2
4201	RX[1186]	-13485.5	72.8
4202	S[2212]	-13494	180.8
4203	S[2213]	-13502.5	288.8
4204	RX[1187]	-13511	-38
4205	S[2214]	-13519.5	70
4206	S[2215]	-13528	178
4207	RX[1188]	-13536.5	286
4208	S[2216]	-13545	-40.8
4209	S[2217]	-13553.5	67.2
4210	RX[1189]	-13562	175.2
4211	S[2218]	-13570.5	283.2
4212	S[2219]	-13579	-43.6

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No.	PAD Name	X	Y
4213	RX[1190]	-13587.5	64.4
4214	S[2220]	-13596	172.4
4215	S[2221]	-13604.5	280.4
4216	RX[1191]	-13613	-46.4
4217	S[2222]	-13621.5	61.6
4218	S[2223]	-13630	169.6
4219	RX[1192]	-13638.5	277.6
4220	S[2224]	-13647	-49.2
4221	S[2225]	-13655.5	58.8
4222	RX[1193]	-13664	166.8
4223	S[2226]	-13672.5	274.8
4224	S[2227]	-13681	-52
4225	RX[1194]	-13689.5	56
4226	S[2228]	-13698	164
4227	S[2229]	-13706.5	272
4228	RX[1195]	-13715	-54.8
4229	S[2230]	-13723.5	53.2
4230	S[2231]	-13732	161.2
4231	RX[1196]	-13740.5	269.2
4232	S[2232]	-13749	-57.6
4233	S[2233]	-13757.5	50.4
4234	RX[1197]	-13766	158.4
4235	S[2234]	-13774.5	266.4
4236	S[2235]	-13783	-60.4
4237	RX[1198]	-13791.5	47.6
4238	S[2236]	-13800	155.6
4239	S[2237]	-13808.5	263.6
4240	RX[1199]	-13817	-63.2
4241	S[2238]	-13825.5	44.8
4242	S[2239]	-13834	152.8
4243	RX[1200]	-13842.5	260.8
4244	S[2240]	-13851	-66
4245	S[2241]	-13859.5	42
4246	RX[1201]	-13868	150
4247	S[2242]	-13876.5	258
4248	S[2243]	-13885	-68.8
4249	RX[1202]	-13893.5	39.2
4250	S[2244]	-13902	147.2
4251	S[2245]	-13910.5	255.2
4252	RX[1203]	-13919	-71.6
4253	S[2246]	-13927.5	36.4
4254	S[2247]	-13936	144.4
4255	RX[1204]	-13944.5	252.4
4256	S[2248]	-13953	-74.4
4257	S[2249]	-13961.5	33.6
4258	RX[1205]	-13970	141.6
4259	S[2250]	-13978.5	249.6
4260	S[2251]	-13987	-77.2
4261	RX[1206]	-13995.5	30.8
4262	S[2252]	-14004	138.8
4263	S[2253]	-14012.5	246.8
4264	RX[1207]	-14021	-80
4265	S[2254]	-14029.5	28
4266	S[2255]	-14038	136
4267	RX[1208]	-14046.5	244
4268	S[2256]	-14055	-82.8
4269	S[2257]	-14063.5	25.2
4270	RX[1209]	-14072	133.2
4271	S[2258]	-14080.5	241.2
4272	S[2259]	-14089	-85.6
4273	RX[1210]	-14097.5	22.4
4274	S[2260]	-14106	130.4
4275	S[2261]	-14114.5	238.4
4276	RX[1211]	-14123	-88.4
4277	S[2262]	-14131.5	19.6
4278	S[2263]	-14140	127.6
4279	RX[1212]	-14148.5	235.6
4280	S[2264]	-14157	-91.2
4281	S[2265]	-14165.5	16.8
4282	RX[1213]	-14174	124.8
4283	S[2266]	-14182.5	232.8
4284	S[2267]	-14191	-94
4285	RX[1214]	-14199.5	14
4286	S[2268]	-14208	122
4287	S[2269]	-14216.5	230
4288	RX[1215]	-14225	-96.8
4289	S[2270]	-14233.5	11.2
4290	S[2271]	-14242	119.2
4291	RX[1216]	-14250.5	227.2
4292	S[2272]	-14259	-99.6
4293	S[2273]	-14267.5	8.4
4294	RX[1217]	-14276	116.4
4295	S[2274]	-14284.5	224.4
4296	S[2275]	-14293	-102.4
4297	RX[1218]	-14301.5	5.6
4298	S[2276]	-14310	113.6
4299	S[2277]	-14318.5	221.6
4300	RX[1219]	-14327	-105.2
4301	S[2278]	-14335.5	2.8
4302	S[2279]	-14344	110.8
4303	RX[1220]	-14352.5	218.8
4304	S[2280]	-14361	-108
4305	S[2281]	-14369.5	0
4306	RX[1221]	-14378	108
4307	S[2282]	-14386.5	216
4308	S[2283]	-14395	-110.8
4309	RX[1222]	-14403.5	-2.8
4310	S[2284]	-14412	105.2
4311	S[2285]	-14420.5	213.2
4312	RX[1223]	-14429	-113.6
4313	S[2286]	-14437.5	-5.6
4314	S[2287]	-14446	102.4
4315	RX[1224]	-14454.5	210.4
4316	S[2288]	-14463	-116.4
4317	S[2289]	-14471.5	-8.4
4318	RX[1225]	-14480	99.6
4319	S[2290]	-14488.5	207.6
4320	S[2291]	-14497	-119.2
4321	RX[1226]	-14505.5	-11.2
4322	S[2292]	-14514	96.8
4323	S[2293]	-14522.5	204.8
4324	RX[1227]	-14531	-122
4325	S[2294]	-14539.5	-14
4326	S[2295]	-14548	94
4327	RX[1228]	-14556.5	202
4328	S[2296]	-14565	-124.8
4329	S[2297]	-14573.5	-16.8
4330	RX[1229]	-14582	91.2
4331	S[2298]	-14590.5	199.2
4332	S[2299]	-14599	-127.6
4333	RX[1230]	-14607.5	-19.6
4334	S[2300]	-14616	88.4
4335	S[2301]	-14624.5	196.4
4336	RX[1231]	-14633	-130.4
4337	S[2302]	-14641.5	-22.4
4338	S[2303]	-14650	85.6
4339	RX[1232]	-14658.5	193.6
4340	S[2304]	-14667	-133.2
4341	S[2305]	-14675.5	-25.2
4342	RX[1233]	-14684	82.8
4343	S[2306]	-14692.5	190.8
4344	S[2307]	-14701	-136
4345	RX[1234]	-14709.5	-28
4346	S[2308]	-14718	80
4347	S[2309]	-14726.5	188
4348	RX[1235]	-14735	-138.8
4349	S[2310]	-14743.5	-30.8
4350	S[2311]	-14752	77.2
4351	RX[1236]	-14760.5	185.2
4352	S[2312]	-14769	-141.6
4353	S[2313]	-14777.5	-33.6
4354	RX[1237]	-14786	74.4
4355	S[2314]	-14794.5	182.4
4356	S[2315]	-14803	-144.4
4357	RX[1238]	-14811.5	-36.4
4358	S[2316]	-14820	71.6
4359	S[2317]	-14828.5	179.6
4360	RX[1239]	-14837	-147.2
4361	S[2318]	-14845.5	-39.2
4362	S[2319]	-14854	68.8
4363	RX[1240]	-14862.5	176.8
4364	S[2320]	-14871	-150
4365	S[2321]	-14879.5	-42
4366	RX[1241]	-14888	66
4367	S[2322]	-14896.5	174
4368	S[2323]	-14905	-152.8
4369	RX[1242]	-14913.5	-44.8
4370	S[2324]	-14922	63.2
4371	S[2325]	-14930.5	171.2
4372	RX[1243]	-14939	-155.6
4373	S[2326]	-14947.5	-47.6
4374	S[2327]	-14956	60.4
4375	RX[1244]	-14964.5	168.4
4376	S[2328]	-14973	-158.4
4377	S[2329]	-14981.5	-50.4
4378	RX[1245]	-14990	57.6
4379	S[2330]	-14998.5	165.6
4380	S[2331]	-15007	-161.2
4381	RX[1246]	-15015.5	-53.2
4382	S[2332]	-15024	54.8
4383	S[2333]	-15032.5	162.8
4384	RX[1247]	-15041	-164
4385	S[2334]	-15049.5	-56
4386	S[2335]	-15058	52
4387	RX[1248]	-15066.5	160
4388	S[2336]	-15075	-166.8
4389	S[2337]	-15083.5	-58.8
4390	RX[1249]	-15092	49.2
4391	S[2338]	-15100.5	157.2
4392	S[2339]	-15109	-169.6
4393	RX[1250]	-15117.5	-61.6
4394	S[2340]	-15126	46.4
4395	S[2341]	-15134.5	154.4
4396	RX[1251]	-15143	-172.4
4397	S[2342]	-15151.5	-64.4
4398	S[2343]	-15160	43.6
4399	RX[1252]	-15168.5	151.6
4400	S[2344]	-15177	-175.2
4401	S[2345]	-15185.5	-67.2
4402	RX[1253]	-15194	40.8
4403	S[2346]	-15202.5	148.8
4404	S[2347]	-15211	-178
4405	RX[1254]	-15219.5	-70
4406	S[2348]	-15228	38
4407	S[2349]	-15236.5	146
4408	RX[1255]	-15245	-180.8
4409	S[2350]	-15253.5	-72.8
4410	S[2351]	-15262	35.2
4411	RX[1256]	-15270.5	143.2
4412	S[2352]	-15279	-183.6
4413	S[2353]	-15287.5	-75.6
4414	RX[1257]	-15296	32.4
4415	S[2354]	-15304.5	140.4
4416	S[2355]	-15313	-186.4
4417	RX[1258]	-15321.5	-78.4
4418	S[2356]	-15330	29.6
4419	S[2357]	-15338.5	137.6
4420	RX[1259]	-15347	-189.2
4421	S[2358]	-15355.5	-81.2
4422	S[2359]	-15364	26.8
4423	RX[1260]	-15372.5	134.8
4424	S[2360]	-15381	-192
4425	S[2361]	-15389.5	-84
4426	RX[1261]	-15398	24
4427	S[2362]	-15406.5	132
4428	S[2363]	-15415	-194.8
4429	RX[1262]	-15423.5	-86.8
4430	S[2364]	-15432	21.2
4431	S[2365]	-15440.5	129.2
4432	RX[1263]	-15449	-197.6
4433	S[2366]	-15457.5	-89.6
4434	S[2367]	-15466	18.4

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No.	PAD Name	X	Y
4435	RX[1264]	-15474.5	126.4
4436	S[2368]	-15483	-200.4
4437	S[2369]	-15491.5	-92.4
4438	RX[1265]	-15500	15.6
4439	S[2370]	-15508.5	123.6
4440	S[2371]	-15517	-203.2
4441	RX[1266]	-15525.5	-95.2
4442	S[2372]	-15534	12.8
4443	S[2373]	-15542.5	120.8
4444	RX[1267]	-15551	-206
4445	S[2374]	-15559.5	-98
4446	S[2375]	-15568	10
4447	RX[1268]	-15576.5	118
4448	S[2376]	-15585	-208.8
4449	S[2377]	-15593.5	-100.8
4450	RX[1269]	-15602	7.2
4451	S[2378]	-15610.5	115.2
4452	S[2379]	-15619	-211.6
4453	RX[1270]	-15627.5	-103.6
4454	S[2380]	-15636	4.4
4455	S[2381]	-15644.5	112.4
4456	RX[1271]	-15653	-214.4
4457	S[2382]	-15661.5	-106.4
4458	S[2383]	-15670	1.6
4459	RX[1272]	-15678.5	109.6
4460	S[2384]	-15687	-217.2
4461	S[2385]	-15695.5	-109.2
4462	RX[1273]	-15704	-1.2
4463	S[2386]	-15712.5	106.8
4464	S[2387]	-15721	-220
4465	RX[1274]	-15729.5	-112
4466	S[2388]	-15738	-4
4467	S[2389]	-15746.5	104
4468	RX[1275]	-15755	-222.8
4469	S[2390]	-15763.5	-114.8
4470	S[2391]	-15772	-6.8
4471	RX[1276]	-15780.5	101.2
4472	S[2392]	-15789	-225.6
4473	S[2393]	-15797.5	-117.6
4474	RX[1277]	-15806	-9.6
4475	S[2394]	-15814.5	98.4
4476	S[2395]	-15823	-228.4
4477	RX[1278]	-15831.5	-120.4
4478	S[2396]	-15840	-12.4
4479	S[2397]	-15848.5	95.6
4480	RX[1279]	-15857	-231.2
4481	S[2398]	-15865.5	-123.2
4482	S[2399]	-15874	-15.2
4483	RX[1280]	-15882.5	92.8
4484	S[2400]	-15891	-234
4485	S[2401]	-15899.5	-126
4486	VCOM_OPT_L	-15908	-18
4487	VCOM_OPT_L	-15916.5	90
4488	VCOM	-15925	-236.8
4489	VCOM	-15933.5	-128.8
4490	GAMMA_P_L[7]	-15942	-20.8
4491	GAMMA_P_L[6]	-15950.5	87.2
4492	GAMMA_P_L[5]	-15959	-239.6
4493	GAMMA_P_L[4]	-15967.5	-131.6
4494	GAMMA_P_L[3]	-15976	-23.6
4495	GAMMA_P_L[2]	-15984.5	84.4
4496	GAMMA_P_L[1]	-15993	-242.4
4497	GAMMA_P_L[0]	-16001.5	-134.4
4498	GAMMA_N_L[0]	-16010	-26.4
4499	GAMMA_N_L[1]	-16018.5	81.6
4500	GAMMA_N_L[2]	-16027	-245.2
4501	GAMMA_N_L[3]	-16035.5	-137.2
4502	GAMMA_N_L[4]	-16044	-29.2
4503	GAMMA_N_L[5]	-16052.5	78.8
4504	GAMMA_N_L[6]	-16061	-248
4505	GAMMA_N_L[7]	-16069.5	-140
4506	DUMMY_C	-11005	-173
4507	DUMMY_C	-10905	-173
4508	DUMMY_C	-10805	-173

No.	PAD Name	X	Y
4509	DUMMY_C	-10705	-173
4510	DUMMY_C	-10605	-173
4511	DUMMY_C	-10505	-173
4512	DUMMY_C	-10405	-173
4513	DUMMY_C	-10305	-173
4514	DUMMY_C	-10205	-173
4515	DUMMY_C	-10105	-173
4516	DUMMY_C	-10005	-173
4517	DUMMY_C	-9905	-173
4518	DUMMY_C	-9805	-173
4519	DUMMY_C	-9705	-173
4520	DUMMY_C	-9605	-173
4521	DUMMY_C	-9505	-173
4522	DUMMY_C	-9405	-173
4523	DUMMY_C	-9305	-173
4524	DUMMY_C	-9205	-173
4525	DUMMY_C	-9105	-173
4526	DUMMY_C	-9005	-173
4527	DUMMY_C	-8905	-173
4528	DUMMY_C	-8805	-173
4529	DUMMY_C	-8705	-173
4530	DUMMY_C	-8605	-173
4531	DUMMY_C	-8505	-173
4532	DUMMY_C	-8405	-173
4533	DUMMY_C	-8305	-173
4534	DUMMY_C	-8205	-173
4535	DUMMY_C	-8105	-173
4536	DUMMY_C	-8005	-173
4537	DUMMY_C	-7905	-173
4538	DUMMY_C	-7805	-173
4539	DUMMY_C	-7705	-173
4540	DUMMY_C	-7605	-173
4541	DUMMY_C	-7505	-173
4542	DUMMY_C	-7405	-173
4543	DUMMY_C	-7305	-173
4544	DUMMY_C	-7205	-173
4545	DUMMY_C	-7105	-173
4546	DUMMY_C	-7005	-173
4547	DUMMY_C	-6905	-173
4548	DUMMY_C	-6805	-173
4549	DUMMY_C	-6705	-173
4550	DUMMY_C	-6605	-173
4551	DUMMY_C	-6505	-173
4552	DUMMY_C	-6405	-173
4553	DUMMY_C	-6305	-173
4554	DUMMY_C	-6205	-173
4555	DUMMY_C	-6105	-173
4556	DUMMY_C	-6005	-173
4557	DUMMY_C	-5905	-173
4558	DUMMY_C	-5805	-173
4559	DUMMY_C	-5705	-173
4560	DUMMY_C	-5605	-173
4561	DUMMY_C	-5505	-173
4562	DUMMY_C	-5405	-173
4563	DUMMY_C	-5305	-173
4564	DUMMY_C	-5205	-173
4565	DUMMY_C	-5105	-173
4566	DUMMY_C	-5005	-173
4567	DUMMY_C	-4905	-173
4568	DUMMY_C	-4805	-173
4569	DUMMY_C	-4705	-173
4570	DUMMY_C	-4605	-173
4571	DUMMY_C	-4505	-173
4572	DUMMY_C	-4405	-173
4573	DUMMY_C	-4305	-173
4574	DUMMY_C	-4205	-173
4575	DUMMY_C	-4105	-173
4576	DUMMY_C	-4005	-173
4577	DUMMY_C	-3905	-173
4578	DUMMY_C	-3805	-173
4579	DUMMY_C	-3705	-173
4580	DUMMY_C	-3605	-173
4581	DUMMY_C	-3505	-173
4582	DUMMY_C	-3405	-173

No.	PAD Name	X	Y
4583	DUMMY_C	-3305	-173
4584	DUMMY_C	-3205	-173
4585	DUMMY_C	-3105	-173
4586	DUMMY_C	-3005	-173
4587	DUMMY_C	-2905	-173
4588	DUMMY_C	-2805	-173
4589	DUMMY_C	-2705	-173
4590	DUMMY_C	-2605	-173
4591	DUMMY_C	-2505	-173
4592	DUMMY_C	-2405	-173
4593	DUMMY_C	-2305	-173
4594	DUMMY_C	-2205	-173
4595	DUMMY_C	-2105	-173
4596	DUMMY_C	-2005	-173
4597	DUMMY_C	-1905	-173
4598	DUMMY_C	-1805	-173
4599	DUMMY_C	-1705	-173
4600	DUMMY_C	-1605	-173
4601	DUMMY_C	-1505	-173
4602	DUMMY_C	-1405	-173
4603	DUMMY_C	-1305	-173
4604	DUMMY_C	-1205	-173
4605	DUMMY_C	-1105	-173
4606	DUMMY_C	-1005	-173
4607	DUMMY_C	-905	-173
4608	DUMMY_C	-805	-173
4609	DUMMY_C	-705	-173
4610	DUMMY_C	-605	-173
4611	DUMMY_C	-505	-173
4612	DUMMY_C	-405	-173
4613	DUMMY_C	-305	-173
4614	DUMMY_C	-205	-173
4615	DUMMY_C	-105	-173
4616	DUMMY_C	-5	-173
4617	DUMMY_C	95	-173
4618	DUMMY_C	195	-173
4619	DUMMY_C	295	-173
4620	DUMMY_C	395	-173
4621	DUMMY_C	495	-173
4622	DUMMY_C	595	-173
4623	DUMMY_C	695	-173
4624	DUMMY_C	795	-173
4625	DUMMY_C	895	-173
4626	DUMMY_C	995	-173
4627	DUMMY_C	1095	-173
4628	DUMMY_C	1195	-173
4629	DUMMY_C	1295	-173
4630	DUMMY_C	1395	-173
4631	DUMMY_C	1495	-173
4632	DUMMY_C	1595	-173
4633	DUMMY_C	1695	-173
4634	DUMMY_C	1795	-173
4635	DUMMY_C	1895	-173
4636	DUMMY_C	1995	-173
4637	DUMMY_C	2095	-173
4638	DUMMY_C	2195	-173
4639	DUMMY_C	2295	-173
4640	DUMMY_C	2395	-173
4641	DUMMY_C	2495	-173
4642	DUMMY_C	2595	-173
4643	DUMMY_C	2695	-173
4644	DUMMY_C	2795	-173
4645	DUMMY_C	2895	-173
4646	DUMMY_C	2995	-173
4647	DUMMY_C	3095	-173
4648	DUMMY_C	3195	-173
4649	DUMMY_C	3295	-173
4650	DUMMY_C	3395	-173
4651	DUMMY_C	3495	-173
4652	DUMMY_C	3595	-173
4653	DUMMY_C	3695	-173
4654	DUMMY_C	3795	-173
4655	DUMMY_C	3895	-173
4656	DUMMY_C	3995	-173

No.	PAD Name	X	Y
4657	DUMMY_C	4095	-173
4658	DUMMY_C	4195	-173
4659	DUMMY_C	4295	-173
4660	DUMMY_C	4395	-173
4661	DUMMY_C	4495	-173
4662	DUMMY_C	4595	-173
4663	DUMMY_C	4695	-173
4664	DUMMY_C	4795	-173
4665	DUMMY_C	4895	-173
4666	DUMMY_C	4995	-173
4667	DUMMY_C	5095	-173
4668	DUMMY_C	5195	-173
4669	DUMMY_C	5295	-173
4670	DUMMY_C	5395	-173
4671	DUMMY_C	5495	-173
4672	DUMMY_C	5595	-173
4673	DUMMY_C	5695	-173
4674	DUMMY_C	5795	-173
4675	DUMMY_C	5895	-173
4676	DUMMY_C	5995	-173
4677	DUMMY_C	6095	-173
4678	DUMMY_C	6195	-173
4679	DUMMY_C	6295	-173
4680	DUMMY_C	6395	-173
4681	DUMMY_C	6495	-173
4682	DUMMY_C	6595	-173
4683	DUMMY_C	6695	-173
4684	DUMMY_C	6795	-173
4685	DUMMY_C	6895	-173
4686	DUMMY_C	6995	-173
4687	DUMMY_C	7095	-173
4688	DUMMY_C	7195	-173
4689	DUMMY_C	7295	-173
4690	DUMMY_C	7395	-173
4691	DUMMY_C	7495	-173
4692	DUMMY_C	7595	-173
4693	DUMMY_C	7695	-173
4694	DUMMY_C	7795	-173
4695	DUMMY_C	7895	-173
4696	DUMMY_C	7995	-173
4697	DUMMY_C	8095	-173
4698	DUMMY_C	8195	-173
4699	DUMMY_C	8295	-173
4700	DUMMY_C	8395	-173
4701	DUMMY_C	8495	-173
4702	DUMMY_C	8595	-173

No.	PAD Name	X	Y
4703	DUMMY_C	8695	-173
4704	DUMMY_C	8795	-173
4705	DUMMY_C	8895	-173
4706	DUMMY_C	8995	-173
4707	DUMMY_C	9095	-173
4708	DUMMY_C	9195	-173
4709	DUMMY_C	9295	-173
4710	DUMMY_C	9395	-173
4711	DUMMY_C	9495	-173
4712	DUMMY_C	9595	-173
4713	DUMMY_C	9695	-173
4714	DUMMY_C	9795	-173
4715	DUMMY_C	9895	-173
4716	DUMMY_C	9995	-173
4717	DUMMY_C	10095	-173
4718	DUMMY_C	10195	-173
4719	DUMMY_C	10295	-173
4720	DUMMY_C	10395	-173
4721	DUMMY_C	10495	-173
4722	DUMMY_C	10595	-173
4723	DUMMY_C	10695	-173
4724	DUMMY_C	10795	-173
4725	DUMMY_C	10895	-173
4726	DUMMY_C	10995	-173
4727	DUMMY_U	15807.5	460
4728	DUMMY_U	15707.5	460
4729	DUMMY_U	15607.5	460
4730	DUMMY_U	15507.5	460
4731	DUMMY_U	15407.5	460
4732	DUMMY_U	15307.5	460
4733	DUMMY_U	15207.5	460
4734	DUMMY_U	15107.5	460
4735	DUMMY_U	15007.5	460
4736	DUMMY_U	14907.5	460
4737	DUMMY_U	14807.5	460
4738	DUMMY_U	14707.5	460
4739	DUMMY_U	14607.5	460
4740	DUMMY_U	14507.5	460
4741	DUMMY_U	14407.5	460
4742	DUMMY_U	14307.5	460
4743	DUMMY_U	14207.5	460
4744	DUMMY_U	14107.5	460
4745	DUMMY_U	14007.5	460
4746	DUMMY_U	13907.5	460
4747	DUMMY_U	13807.5	460
4748	DUMMY_U	13707.5	460

No.	PAD Name	X	Y
4749	DUMMY_U	13607.5	460
4750	DUMMY_U	13507.5	460
4751	DUMMY_U	13407.5	460
4752	DUMMY_U	-13407.5	460
4753	DUMMY_U	-13507.5	460
4754	DUMMY_U	-13607.5	460
4755	DUMMY_U	-13707.5	460
4756	DUMMY_U	-13807.5	460
4757	DUMMY_U	-13907.5	460
4758	DUMMY_U	-14007.5	460
4759	DUMMY_U	-14107.5	460
4760	DUMMY_U	-14207.5	460
4761	DUMMY_U	-14307.5	460
4762	DUMMY_U	-14407.5	460
4763	DUMMY_U	-14507.5	460
4764	DUMMY_U	-14607.5	460
4765	DUMMY_U	-14707.5	460
4766	DUMMY_U	-14807.5	460
4767	DUMMY_U	-14907.5	460
4768	DUMMY_U	-15007.5	460
4769	DUMMY_U	-15107.5	460
4770	DUMMY_U	-15207.5	460
4771	DUMMY_U	-15307.5	460
4772	DUMMY_U	-15407.5	460
4773	DUMMY_U	-15507.5	460
4774	DUMMY_U	-15607.5	460
4775	DUMMY_U	-15707.5	460
4776	DUMMY_U	-15807.5	460

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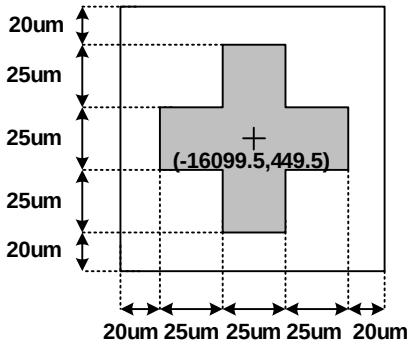
8.4 Alignment Mark

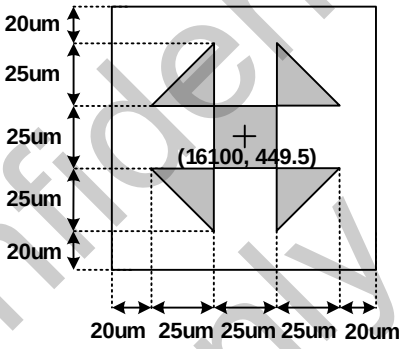
--Alignment Mark coordinate

Left (-16099.5,449.5)

Right (16100,449.5)

--Alignment Mark size





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10REVISION HISTORY

Date	Revision #	Description	Page	Auditor
Aug.05,2022	0.1	Original.		Frank.Huang

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