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ILI9340X

a-Si TFT LCD Single Chip Driver 240RGBx320 Resolution and 262K color

Specification

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1. Introduction

ILI9340X is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

ILI9340X supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface , 3-/4-line serial peripheral interface (SPI) and 2 lane SPI data transmission. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

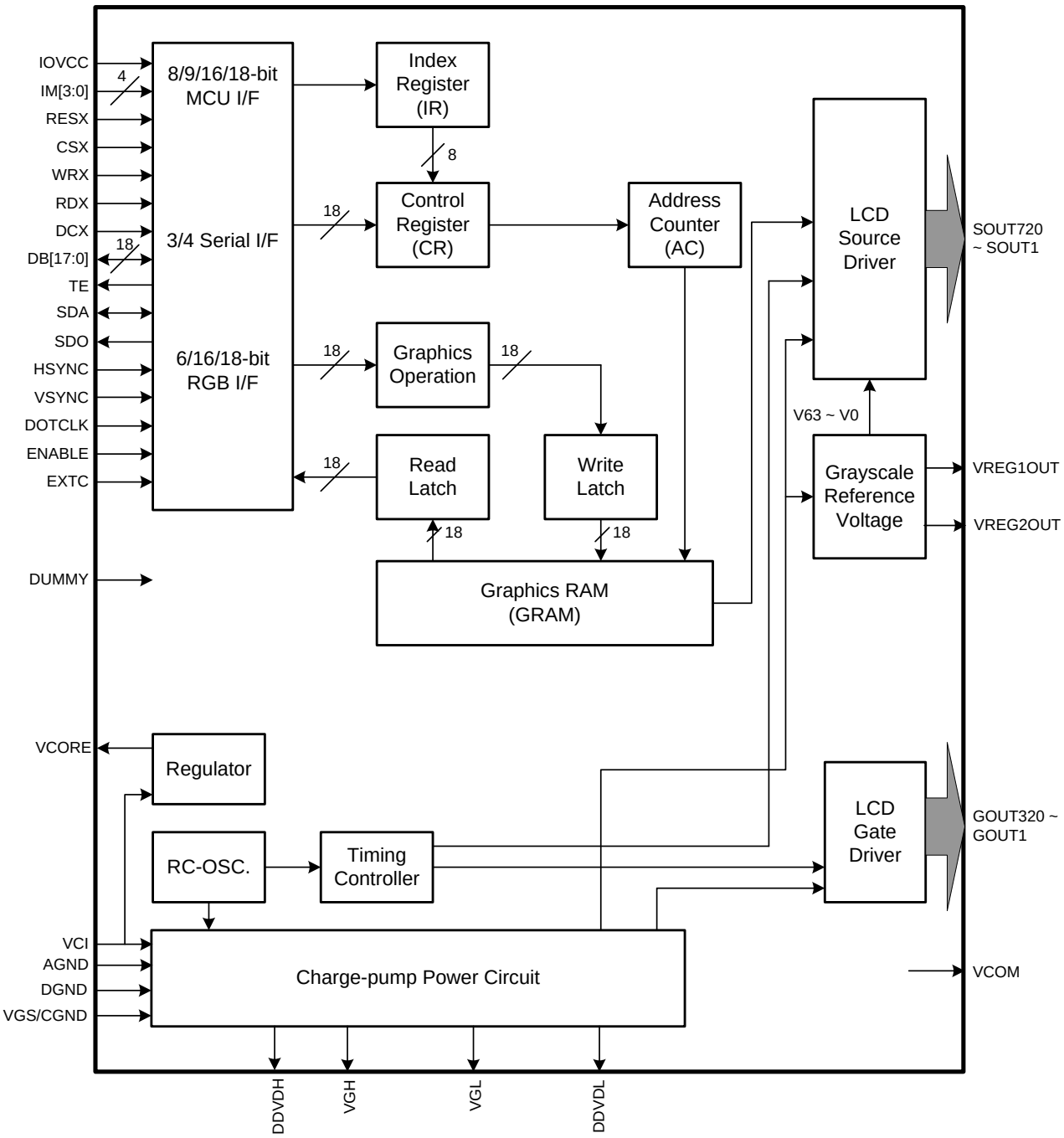
ILI9340X can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. ILI9340X supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9340X an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution: [240xRGB](H) x 320(V)
- Output:
  - 720 source outputs
  - 320 gate outputs
  - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-Ⅰ/8080-Ⅱ series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 3-line / 4-line serial interface / 2-lane mode serial interface
- Display mode:
  - Full color mode (Idle mode Off): 262K-color
  - Reduce color mode (Idle mode On): 8-color
- Power saving mode:
  - Sleep mode
- On chip functions:
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Dot/Column inversion
  - Gamma curves with separate RGB Gamma correction
- OTP :
  - 8-bits for ID1, ID2, ID3 (Provides 2 times)
  - MADCTL (MX/MY/MV/RGB/REV)
  - 7-bits for VCOM adjustment (provides 3 times)
  - GAMMA adjustment

- Low -power consumption architecture
  - Low operating power supplies:
    - IOVCC = 1.65V ~ 3.3V (logic)
    - VCI = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
  - Source power supply voltage
    - DDVDH - GND = 6.1V ~ 6.8V
    - DDVDL – GND = -4.3 ~ -5V
  - Gate driver output voltage
    - VGH - GND = 12.2V ~ 15.0V
    - VGL - GND = -7.0V ~ -12.6V
    - VGH - VGL ≦ 27.6V
  - VCOM driver output voltage
    - VCOM = 0 V
- Operate temperature range: -40℃ to 85℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram



4. Pin Descriptions

Power Supply Pins			
Pin Name	**I/O**	**Type**	**Descriptions**
IOVCC	I	Power	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)
VCI	I	Power	High voltage power supply for analog circuit blocks (2.5 ~ 3.3 V)
VCORE	O	Digital Power	Regulated Low voltage level for interface circuits
DGND	I	Digital Ground	- DGND for the digital side: DGND = 0V. In case of COG, connect to ground on the FPC to prevent noise.
AGND/VGS/CGND	I	Analog Ground	- AGND for the analog side: AGND = 0V. In case of COG, connect to ground on the FPC to prevent noise.

<table>
<tr><th colspan="3">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(IOVCC/GND)</td><td>- Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface Mode</th><th colspan="2">DB Pin in use</th></tr>
<tr><th>Register/Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface Ⅰ</td><td>DB[7:0]</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80 MCU 16-bit bus interface Ⅰ</td><td>DB[7:0]</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80 MCU 9-bit bus interface Ⅰ</td><td>DB[7:0]</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface Ⅰ</td><td>DB[7:0]</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-line 9-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/Out</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-line 8-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/Out</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface Ⅱ</td><td>DB[8:1]</td><td>DB[17:10]
DB[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface Ⅱ</td><td>DB[17:10]</td><td>DB[17:10],</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface Ⅱ</td><td>DB[8:1]</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface Ⅱ</td><td>DB[17:10]</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-line 9-bit data serial interface Ⅱ</td><td colspan="2">SDI: In
SDO: Out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-line 8-bit data serial interface Ⅱ</td><td colspan="2">SDI: In
SDO: Out</td></tr>
</table>
MPU Parallel interface bus and serial interface select
When the RGB Interface is used, the serial interface is selected for command setting.
* : Fix these pins at IOVCC or GND.</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>This signal will reset the device and must be applied properly to initialize the chip.
Signal is active low.</td></tr>
<tr><td>EXTC</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>Extended command set enable.
Low: extended command access set is prohibited.
High: extended command access set is accepted.
Please connect EXTC to IOVCC to access extended registers
Fix these pins at IOVCC or GND.</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>Chip select input pin (“Low” enable).
This pin can be permanently fixed “Low” state in MPU interface mode only.
In 2-lane SPI mode must be a high-to-low pulse between command 2Ch to pixel data interval time.
* note1,2</td></tr>
<tr><td>DCX
(SCL)</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>(DCX) This pin is used to select “Data or Command” in the parallel interface.
When DCX = ’1’, data is selected.
When DCX = ’0’, command is selected.</td></tr>
</table>

			(SCL) This pin is also used as serial interface clock in 3-line 9-bit / 4-line 8-bit serial data interface. If it's not used, this pin should be connected to IOVCC or Ground.
RDX	I	MCU (IOVCC/GND)	8080-Ⅰ/8080-Ⅱ system (RDX): Serves as a read signal and MCU read data at the rising edge. *Fix to IOVCC or GND level when not in use.*
WRX (D/CX)	I	MCU (IOVCC/GND)	- 8080-Ⅰ/8080-Ⅱ system (WRX): Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as Data or Command select. - In serial interface "2-data-lane data" transfers mode, serves as a second data pin (SDA2) *Fix to IOVCC or GND level when not in use.*
DB[17:0]	I/O	MCU (IOVCC/GND)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode *Fix to GND level when not in use*
SDA (SDI)	I/O	MCU (IOVCC/GND)	When IM3= '0', serves as a serial in/out signal.(SDA) When IM3 ='1', serves as a serial in signal.(SDI) The data is applied on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND.
SDO	O	MCU (IOVCC/GND)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (IOVCC/GND)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	MCU (IOVCC/GND)	Dot clock signal for RGB interface operation. *Fix to IOVCC or GND level when not in use.*
VSYNC	I	MCU (IOVCC/GND)	Frame synchronizing signal for RGB interface operation. *Fix to IOVCC or GND level when not in use.*
HSYNC	I	MCU (IOVCC/GND)	Line synchronizing signal for RGB interface operation. *Fix to IOVCC or GND level when not in use.*
ENABLE	I	MCU (IOVCC/GND)	Data enable signal for RGB interface operation. *Fix to IOVCC or GND level when not in use.*

Note.

1. If CSX is connected to GND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

3. 3-line 9bit serial interface and 4-line 8bit interface can use 2-lane SPI mode when send pixel data.

4. GND is short for ground.

LCD Driver Input/Output Pins			
Pin Name	**I/O**	**Type**	**Descriptions**
SOUT720~SOUT1	O	Source	Source output signals.. *Leave the pin to open when not in use.*
GOUT320~GOUT1	O	Gate	Gate output signals. *Leave the pin to open when not in use.*
DDVDH	O	Power	Power supply for the source driver.
DDVDL	O	Power	Power supply for the source driver.(Negative)
VGH	O	Power	Power supply for the gate driver.
VGL	O	Power	Power supply for the gate driver. (Negative)
VREG1OUT	O	-	Internal generated stable power for source driver unit. VREG1OUT is a positive grayscale reference voltage of source driver.
VREG2OUT	O	-	Internal generated stable power for source driver unit. VREG2OUT is a negative grayscale reference voltage of source driver.
VCOM_L VCOM_R	O	-	- The power supply of common voltage in DC VCOM driving.
LED_PWM	O		Output pin for tri-state driving. If not used,open this pad.
LED_EN	O		Output pin for tri-state driving. If not used,open this pad.

Test Pins			
Pin Name	**I/O**	**Type**	**Descriptions**
VPP	I	Power supply	Power supply pin for the OTP memory programming. Leave it open when not used.
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
TEST0~8 TESTOSC TEST_EN	I	Open	- Test pins Please leave these pins as open.

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		720 pins (240 x RGB)
2	TFT Gate Driver		320 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	SOUT1 ~ SOUT720	V0 ~ V63 grayscales
		GOUT1 ~ GOUT320	VGH - VGL
		VCOM_L VCOM_R	0V
5	Input Voltage	IOVCC	1.65V ~ 3.30V
		VCI	2.50V ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH	6.1V ~ 6.8V
		DDVDL	-4.3V ~ -5.0V
		VGH	12.2V ~ 15.0V
		VGL	-7.0V ~ -12.6V
		VGH - VGL	Max. 27.6V
7	Internal Step-up Circuits	DDVDH	VCI x 3
		DDVDL	VCI x -2
		VGH	VCI x 6
		VGL	VCI x-5

5. Pad Arrangement and Coordination

Chip Size：15150 um x 700 um

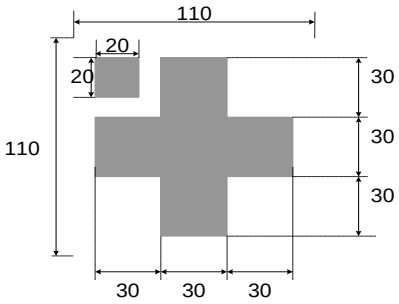
Chip Thickness：280um (typ.)

Pad Location：Pad Center.

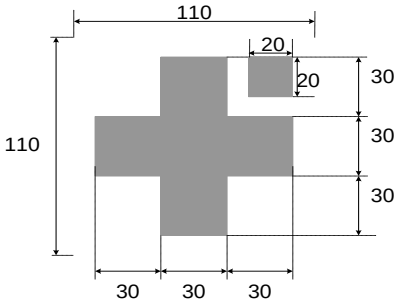
Coordinate Origin：Chip center (0,0)

Bump Height：9um (typ.)

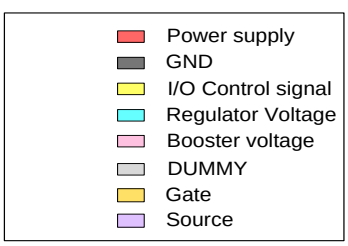
Alignment Marks

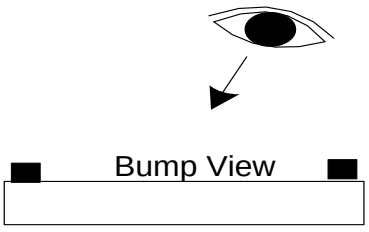


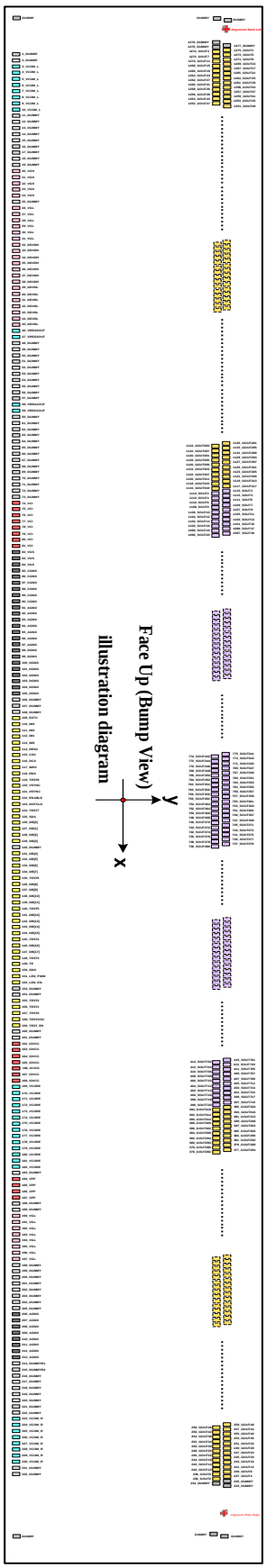
Alignment Mark: A1



Alignment Mark: A2







No.	Pad name	X	Y
1	DUMMY	-7291.21	-258
2	DUMMY	-7231.21	-258
3	VCOM_L	-7171.23	-258
4	VCOM_L	-7111.23	-258
5	VCOM_L	-7051.25	-258
6	VCOM_L	-6991.25	-258
7	VCOM_L	-6931.27	-258
8	VCOM_L	-6871.27	-258
9	VCOM_L	-6811.30	-258
10	VCOM_L	-6751.30	-258
11	DUMMY	-6691.32	-258
12	DUMMY	-6631.32	-258
13	DUMMY	-6571.34	-258
14	DUMMY	-6511.34	-258
15	DUMMY	-6451.36	-258
16	DUMMY	-6391.36	-258
17	DUMMY	-6331.38	-258
18	DUMMY	-6271.38	-258
19	DUMMY	-6211.40	-258
20	VGL	-6151.40	-258
21	VGL	-6091.43	-258
22	VGL	-6031.43	-258
23	VGL	-5971.45	-258
24	VGL	-5911.45	-258
25	DUMMY	-5851.47	-258
26	VGL	-5791.47	-258
27	VGL	-5731.49	-258
28	VGL	-5671.49	-258
29	VGL	-5611.51	-258
30	VGL	-5551.51	-258
31	VGL	-5491.53	-258
32	VGH	-5431.53	-258
33	VGH	-5371.55	-258
34	VGH	-5311.55	-258
35	VGH	-5251.58	-258
36	VGH	-5191.58	-258
37	VGH	-5131.60	-258
38	VGH	-5071.60	-258
39	DDVDL	-5011.62	-258
40	DDVDL	-4951.62	-258
41	DDVDL	-4891.64	-258
42	DDVDL	-4831.64	-258
43	DDVDL	-4771.66	-258
44	DDVDL	-4711.66	-258
45	DDVDL	-4651.68	-258
46	VREG2OUT	-4591.68	-258
47	VREG2OUT	-4531.70	-258
48	DUMMY	-4471.70	-258
49	DUMMY	-4411.73	-258
50	DUMMY	-4351.73	-258
51	DUMMY	-4291.75	-258
52	DUMMY	-4231.75	-258
53	DUMMY	-4171.77	-258
54	DUMMY	-4111.77	-258
55	DUMMY	-4051.79	-258
56	DUMMY	-3991.79	-258
57	DUMMY	-3931.81	-258
58	VREG1OUT	-3871.81	-258
59	VREG1OUT	-3811.83	-258
60	DUMMY	-3751.83	-258
61	DUMMY	-3691.86	-258
62	DUMMY	-3631.86	-258
63	DUMMY	-3571.88	-258
64	DUMMY	-3511.88	-258
65	DUMMY	-3451.90	-258
66	DUMMY	-3391.90	-258
67	DUMMY	-3331.92	-258
68	DUMMY	-3271.92	-258
69	DUMMY	-3211.94	-258
70	DUMMY	-3151.94	-258
71	DUMMY	-3091.96	-258
72	DUMMY	-3031.96	-258
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74	VCI	-2911.98	-258
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77	VCI	-2732.03	-258
78	VCI	-2672.03	-258
79	VCI	-2612.05	-258
80	VCI	-2552.05	-258
81	VCI	-2492.07	-258
82	VGS	-2432.07	-258
83	VGS	-2372.09	-258
84	VGS	-2312.09	-258
85	AGND	-2252.11	-258
86	AGND	-2192.11	-258
87	AGND	-2132.13	-258
88	AGND	-2072.13	-258
89	AGND	-2012.16	-258
90	AGND	-1952.16	-258
91	AGND	-1892.18	-258
92	AGND	-1832.18	-258
93	AGND	-1772.20	-258
94	AGND	-1712.20	-258
95	AGND	-1652.22	-258
96	AGND	-1592.22	-258
97	AGND	-1532.24	-258
98	DGND	-1472.24	-258
99	DGND	-1412.26	-258
100	DGND	-1352.26	-258
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102	DGND	-1232.29	-258
103	DGND	-1172.31	-258
104	DGND	-1112.31	-258
105	DGND	-1052.33	-258
106	DUMMY	-992.33	-258
107	DUMMY	-932.35	-258
108	DUMMY	-872.35	-258
109	EXTC	-812.37	-258
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112	IM1	-632.39	-258
113	IM0	-572.41	-258
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115	CSX	-452.44	-258
116	DCX	-392.44	-258
117	WRX	-332.46	-258
118	RDX	-272.46	-258
119	TEST8	-212.48	-258
120	VSYNC	-152.48	-258
121	HSYNC	-92.50	-258
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148	TEST3	2002.21	-258
149	TE	2074.69	-258
150	SDO	2159.69	-258
151	LED_PWM	2244.66	-258
152	LED_EN	2329.66	-258
153	DUMMY	2402.14	-258
154	DUMMY	2462.14	-258
155	TEST2	2534.62	-258
156	TEST1	2619.62	-258
157	TEST0	2704.59	-258
158	TESTOSC	2789.59	-258
159	TEST_EN	2874.57	-258
160	DUMMY	2959.57	-258
161	DUMMY	3032.04	-258
162	IOVCC	3092.04	-258
163	IOVCC	3152.02	-258
164	IOVCC	3212.02	-258
165	IOVCC	3272.00	-258
166	IOVCC	3332.00	-258
167	IOVCC	3391.97	-258
168	IOVCC	3451.97	-258
169	VCORE	3511.95	-258
170	VCORE	3571.95	-258
171	VCORE	3631.92	-258
172	VCORE	3691.92	-258
173	VCORE	3751.90	-258
174	VCORE	3811.90	-258
175	VCORE	3871.88	-258
176	VCORE	3931.88	-258
177	VCORE	3991.85	-258
178	VCORE	4051.85	-258
179	VCORE	4111.83	-258
180	VCORE	4171.83	-258
181	VCORE	4231.80	-258
182	VCORE	4291.80	-258
183	DUMMY	4351.78	-258
184	VPP	4411.78	-258
185	VPP	4471.76	-258
186	VPP	4531.76	-258
187	VPP	4591.73	-258
188	DUMMY	4651.73	-258
189	DUMMY	4711.71	-258
190	DDVDH	4771.71	-258
191	DDVDH	4831.68	-258
192	DDVDH	4891.68	-258
193	DDVDH	4951.66	-258
194	DDVDH	5011.66	-258
195	DDVDH	5071.64	-258
196	DDVDH	5131.64	-258
197	DDVDH	5191.61	-258
198	DUMMY	5251.61	-258
199	DUMMY	5311.59	-258
200	DUMMY	5371.59	-258

No.	Pad name	X	Y
201	DUMMY	5371.59	-258
202	DUMMY	5431.56	-258
203	DUMMY	5491.56	-258
204	DUMMY	5551.54	-258
205	DUMMY	5611.54	-258
206	AGND	5671.52	-258
207	AGND	5731.52	-258
208	AGND	5791.49	-258
209	AGND	5851.49	-258
210	AGND	5911.47	-258
211	AGND	5971.47	-258
212	AGND	6031.44	-258
213	AGND	6091.44	-258
214	DUMMY	6151.42	-258
215	DUMMY	6211.42	-258
216	DUMMY	6271.40	-258
217	DUMMY	6331.40	-258
218	DUMMY	6391.37	-258
219	DUMMY	6451.37	-258
220	DUMMY	6511.35	-258
221	DUMMY	6571.35	-258
222	DUMMY	6631.32	-258
223	VCOM_R	6691.32	-258
224	VCOM_R	6751.30	-258
225	VCOM_R	6811.30	-258
226	VCOM_R	6871.28	-258
227	VCOM_R	6931.28	-258
228	VCOM_R	6991.25	-258
229	VCOM_R	7051.25	-258
230	VCOM_R	7111.23	-258
231	DUMMY	7171.23	-258
232	DUMMY	7231.20	-258
233	DUMMY	7291.20	256
234	DUMMY	7397.69	125
235	DUMMY	7383.70	256
236	GOUT2	7369.70	125
237	GOUT4	7355.70	256
238	GOUT6	7341.70	125
239	GOUT8	7327.71	256
240	GOUT10	7313.71	125
241	GOUT12	7299.71	256
242	GOUT14	7285.71	125
243	GOUT16	7271.72	256
244	GOUT18	7257.72	125
245	GOUT20	7243.72	256
246	GOUT22	7229.72	125
247	GOUT24	7215.73	256
248	GOUT26	7201.73	125
249	GOUT28	7187.73	256
250	GOUT30	7173.73	125

No.	Pad name	X	Y
251	GOUT32	7145.74	256
252	GOUT34	7131.74	125
253	GOUT36	7117.74	256
254	GOUT38	7103.75	125
255	GOUT40	7089.75	256
256	GOUT42	7075.75	125
257	GOUT44	7061.75	256
258	GOUT46	7047.76	125
259	GOUT48	7033.76	256
260	GOUT50	7019.76	125
261	GOUT52	7005.76	256
262	GOUT54	6991.77	125
263	GOUT56	6977.77	256
264	GOUT58	6963.77	125
265	GOUT60	6949.77	256
266	GOUT62	6935.78	125
267	GOUT64	6921.78	256
268	GOUT66	6907.78	125
269	GOUT68	6893.78	256
270	GOUT70	6879.79	125
271	GOUT72	6865.79	256
272	GOUT74	6851.79	125
273	GOUT76	6837.79	256
274	GOUT78	6823.80	125
275	GOUT80	6809.80	256
276	GOUT82	6795.80	125
277	GOUT84	6781.80	256
278	GOUT86	6767.81	125
279	GOUT88	6753.81	256
280	GOUT90	6739.81	125
281	GOUT92	6725.81	256
282	GOUT94	6711.82	125
283	GOUT96	6697.82	256
284	GOUT98	6683.82	125
285	GOUT100	6669.82	256
286	GOUT102	6655.83	125
287	GOUT104	6641.83	256
288	GOUT106	6627.83	125
289	GOUT108	6613.83	256
290	GOUT110	6599.84	125
291	GOUT112	6585.84	256
292	GOUT114	6571.84	125
293	GOUT116	6557.84	256
294	GOUT118	6543.85	125
295	GOUT120	6529.85	256
296	GOUT122	6515.85	125
297	GOUT124	6501.85	256
298	GOUT126	6487.86	125
299	GOUT128	6473.86	256
300	GOUT130	6459.86	125

No.	Pad name	X	Y
301	GOUT132	6445.86	256
302	GOUT134	6431.87	125
303	GOUT136	6417.87	256
304	GOUT138	6403.87	125
305	GOUT140	6389.87	256
306	GOUT142	6375.88	125
307	GOUT144	6361.88	256
308	GOUT146	6347.88	125
309	GOUT148	6333.88	256
310	GOUT150	6319.89	125
311	GOUT152	6305.89	256
312	GOUT154	6291.89	125
313	GOUT156	6277.89	256
314	GOUT158	6263.90	125
315	GOUT160	6249.90	256
316	GOUT162	6235.90	125
317	GOUT164	6221.90	256
318	GOUT166	6207.91	125
319	GOUT168	6193.91	256
320	GOUT170	6179.91	125
321	GOUT172	6165.91	256
322	GOUT174	6151.92	125
323	GOUT176	6137.92	256
324	GOUT178	6123.92	125
325	GOUT180	6109.92	256
326	GOUT182	6095.93	125
327	GOUT184	6081.93	256
328	GOUT186	6067.93	125
329	GOUT188	6053.93	256
330	GOUT190	6039.94	125
331	GOUT192	6025.94	256
332	GOUT194	6011.94	125
333	GOUT196	5997.94	256
334	GOUT198	5983.95	125
335	GOUT200	5969.95	256
336	GOUT202	5955.95	125
337	GOUT204	5941.95	256
338	GOUT206	5927.96	125
339	GOUT208	5913.96	256
340	GOUT210	5899.96	125
341	GOUT212	5885.96	256
342	GOUT214	5871.97	125
343	GOUT216	5857.97	256
344	GOUT218	5843.97	125
345	GOUT220	5829.97	256
346	GOUT222	5815.98	125
347	GOUT224	5801.98	256
348	GOUT226	5787.98	125
349	GOUT228	5773.98	256
350	GOUT230	5759.99	125

No.	Pad name	X	Y
351	GOUT232	5745.99	256
352	GOUT234	5731.99	125
353	GOUT236	5717.99	256
354	GOUT238	5704.00	125
355	GOUT240	5690.00	256
356	GOUT242	5676.00	125
357	GOUT244	5662.00	256
358	GOUT246	5648.01	125
359	GOUT248	5634.01	256
360	GOUT250	5620.01	125
361	GOUT252	5606.01	256
362	GOUT254	5592.02	125
363	GOUT256	5578.02	256
364	GOUT258	5564.02	125
365	GOUT260	5550.02	256
366	GOUT262	5536.03	125
367	GOUT264	5522.03	256
368	GOUT266	5508.03	125
369	GOUT268	5494.03	256
370	GOUT270	5480.04	125
371	GOUT272	5466.04	256
372	GOUT274	5452.04	125
373	GOUT276	5438.04	256
374	GOUT278	5424.05	125
375	GOUT280	5410.05	256
376	GOUT282	5396.05	125
377	GOUT284	5382.05	256
378	GOUT286	5368.06	125
379	GOUT288	5354.06	256
380	GOUT290	5340.06	125
381	GOUT292	5326.06	256
382	GOUT294	5312.07	125
383	GOUT296	5298.07	256
384	GOUT298	5284.07	125
385	GOUT300	5270.07	256
386	GOUT302	5256.08	125
387	GOUT304	5242.08	256
388	GOUT306	5228.08	125
389	GOUT308	5214.08	256
390	GOUT310	5200.09	125
391	GOUT312	5186.09	256
392	GOUT314	5172.09	125
393	GOUT316	5158.09	256
394	GOUT318	5144.10	125
395	GOUT320	5130.10	256
396	SOUT720	5074.10	125
397	SOUT719	5060.10	256
398	SOUT718	5046.11	125
399	SOUT717	5032.11	256
400	SOUT716	5018.11	125

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
401	SOUT715	5004.11	256	451	SOUT665	4304.24	256	501	SOUT615	3604.36	256	551	SOUT565	2904.49	256
402	SOUT714	4990.12	125	452	SOUT664	4290.24	125	502	SOUT614	3590.37	125	552	SOUT564	2890.49	125
403	SOUT713	4976.12	256	453	SOUT663	4276.24	256	503	SOUT613	3576.37	256	553	SOUT563	2876.49	256
404	SOUT712	4962.12	125	454	SOUT662	4262.25	125	504	SOUT612	3562.37	125	554	SOUT562	2862.50	125
405	SOUT711	4948.12	256	455	SOUT661	4248.25	256	505	SOUT611	3548.37	256	555	SOUT561	2848.50	256
406	SOUT710	4934.13	125	456	SOUT660	4234.25	125	506	SOUT610	3534.38	125	556	SOUT560	2834.50	125
407	SOUT709	4920.13	256	457	SOUT659	4220.25	256	507	SOUT609	3520.38	256	557	SOUT559	2820.50	256
408	SOUT708	4906.13	125	458	SOUT658	4206.26	125	508	SOUT608	3506.38	125	558	SOUT558	2806.51	125
409	SOUT707	4892.13	256	459	SOUT657	4192.26	256	509	SOUT607	3492.38	256	559	SOUT557	2792.51	256
410	SOUT706	4878.14	125	460	SOUT656	4178.26	125	510	SOUT606	3478.39	125	560	SOUT556	2778.51	125
411	SOUT705	4864.14	256	461	SOUT655	4164.26	256	511	SOUT605	3464.39	256	561	SOUT555	2764.51	256
412	SOUT704	4850.14	125	462	SOUT654	4150.27	125	512	SOUT604	3450.39	125	562	SOUT554	2750.52	125
413	SOUT703	4836.14	256	463	SOUT653	4136.27	256	513	SOUT603	3436.39	256	563	SOUT553	2736.52	256
414	SOUT702	4822.15	125	464	SOUT652	4122.27	125	514	SOUT602	3422.40	125	564	SOUT552	2722.52	125
415	SOUT701	4808.15	256	465	SOUT651	4108.27	256	515	SOUT601	3408.40	256	565	SOUT551	2708.52	256
416	SOUT700	4794.15	125	466	SOUT650	4094.28	125	516	SOUT600	3394.40	125	566	SOUT550	2694.53	125
417	SOUT699	4780.15	256	467	SOUT649	4080.28	256	517	SOUT599	3380.40	256	567	SOUT549	2680.53	256
418	SOUT698	4766.16	125	468	SOUT648	4066.28	125	518	SOUT598	3366.41	125	568	SOUT548	2666.53	125
419	SOUT697	4752.16	256	469	SOUT647	4052.28	256	519	SOUT597	3352.41	256	569	SOUT547	2652.53	256
420	SOUT696	4738.16	125	470	SOUT646	4038.29	125	520	SOUT596	3338.41	125	570	SOUT546	2638.54	125
421	SOUT695	4724.16	256	471	SOUT645	4024.29	256	521	SOUT595	3324.41	256	571	SOUT545	2624.54	256
422	SOUT694	4710.17	125	472	SOUT644	4010.29	125	522	SOUT594	3310.42	125	572	SOUT544	2610.54	125
423	SOUT693	4696.17	256	473	SOUT643	3996.29	256	523	SOUT593	3296.42	256	573	SOUT543	2596.54	256
424	SOUT692	4682.17	125	474	SOUT642	3982.30	125	524	SOUT592	3282.42	125	574	SOUT542	2582.55	125
425	SOUT691	4668.17	256	475	SOUT641	3968.30	256	525	SOUT591	3268.42	256	575	SOUT541	2568.55	256
426	SOUT690	4654.18	125	476	SOUT640	3954.30	125	526	SOUT590	3254.43	125	576	SOUT540	2554.55	125
427	SOUT689	4640.18	256	477	SOUT639	3940.30	256	527	SOUT589	3240.43	256	577	SOUT539	2540.55	256
428	SOUT688	4626.18	125	478	SOUT638	3926.31	125	528	SOUT588	3226.43	125	578	SOUT538	2526.56	125
429	SOUT687	4612.18	256	479	SOUT637	3912.31	256	529	SOUT587	3212.43	256	579	SOUT537	2512.56	256
430	SOUT686	4598.19	125	480	SOUT636	3898.31	125	530	SOUT586	3198.44	125	580	SOUT536	2498.56	125
431	SOUT685	4584.19	256	481	SOUT635	3884.31	256	531	SOUT585	3184.44	256	581	SOUT535	2484.56	256
432	SOUT684	4570.19	125	482	SOUT634	3870.32	125	532	SOUT584	3170.44	125	582	SOUT534	2470.57	125
433	SOUT683	4556.19	256	483	SOUT633	3856.32	256	533	SOUT583	3156.44	256	583	SOUT533	2456.57	256
434	SOUT682	4542.20	125	484	SOUT632	3842.32	125	534	SOUT582	3142.45	125	584	SOUT532	2442.57	125
435	SOUT681	4528.20	256	485	SOUT631	3828.32	256	535	SOUT581	3128.45	256	585	SOUT531	2428.57	256
436	SOUT680	4514.20	125	486	SOUT630	3814.33	125	536	SOUT580	3114.45	125	586	SOUT530	2414.58	125
437	SOUT679	4500.20	256	487	SOUT629	3800.33	256	537	SOUT579	3100.45	256	587	SOUT529	2400.58	256
438	SOUT678	4486.21	125	488	SOUT628	3786.33	125	538	SOUT578	3086.46	125	588	SOUT528	2386.58	125
439	SOUT677	4472.21	256	489	SOUT627	3772.33	256	539	SOUT577	3072.46	256	589	SOUT527	2372.58	256
440	SOUT676	4458.21	125	490	SOUT626	3758.34	125	540	SOUT576	3058.46	125	590	SOUT526	2358.59	125
441	SOUT675	4444.21	256	491	SOUT625	3744.34	256	541	SOUT575	3044.46	256	591	SOUT525	2344.59	256
442	SOUT674	4430.22	125	492	SOUT624	3730.34	125	542	SOUT574	3030.47	125	592	SOUT524	2330.59	125
443	SOUT673	4416.22	256	493	SOUT623	3716.34	256	543	SOUT573	3016.47	256	593	SOUT523	2316.59	256
444	SOUT672	4402.22	125	494	SOUT622	3702.35	125	544	SOUT572	3002.47	125	594	SOUT522	2302.60	125
445	SOUT671	4388.22	256	495	SOUT621	3688.35	256	545	SOUT571	2988.47	256	595	SOUT521	2288.60	256
446	SOUT670	4374.23	125	496	SOUT620	3674.35	125	546	SOUT570	2974.48	125	596	SOUT520	2274.60	125
447	SOUT669	4360.23	256	497	SOUT619	3660.35	256	547	SOUT569	2960.48	256	597	SOUT519	2260.60	256
448	SOUT668	4346.23	125	498	SOUT618	3646.36	125	548	SOUT568	2946.48	125	598	SOUT518	2246.61	125
449	SOUT667	4332.23	256	499	SOUT617	3632.36	256	549	SOUT567	2932.48	256	599	SOUT517	2232.61	256
450	SOUT666	4318.24	125	500	SOUT616	3618.36	125	550	SOUT566	2918.49	125	600	SOUT516	2218.61	125

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
601	SOUT515	2204.61	256	651	SOUT465	1504.74	256	701	SOUT415	804.86	256	751	SOUT365	104.99	256
602	SOUT514	2190.62	125	652	SOUT464	1490.74	125	702	SOUT414	790.87	125	752	SOUT364	90.99	125
603	SOUT513	2176.62	256	653	SOUT463	1476.74	256	703	SOUT413	776.87	256	753	SOUT363	76.99	256
604	SOUT512	2162.62	125	654	SOUT462	1462.75	125	704	SOUT412	762.87	125	754	SOUT362	63.00	125
605	SOUT511	2148.62	256	655	SOUT461	1448.75	256	705	SOUT411	748.87	256	755	SOUT361	49.00	256
606	SOUT510	2134.63	125	656	SOUT460	1434.75	125	706	SOUT410	734.88	125	756	SOUT360	-49.00	125
607	SOUT509	2120.63	256	657	SOUT459	1420.75	256	707	SOUT409	720.88	256	757	SOUT359	-63.00	256
608	SOUT508	2106.63	125	658	SOUT458	1406.76	125	708	SOUT408	706.88	125	758	SOUT358	-76.99	125
609	SOUT507	2092.63	256	659	SOUT457	1392.76	256	709	SOUT407	692.88	256	759	SOUT357	-90.99	256
610	SOUT506	2078.64	125	660	SOUT456	1378.76	125	710	SOUT406	678.89	125	760	SOUT356	-104.99	125
611	SOUT505	2064.64	256	661	SOUT455	1364.76	256	711	SOUT405	664.89	256	761	SOUT355	-118.99	256
612	SOUT504	2050.64	125	662	SOUT454	1350.77	125	712	SOUT404	650.89	125	762	SOUT354	-132.98	125
613	SOUT503	2036.64	256	663	SOUT453	1336.77	256	713	SOUT403	636.89	256	763	SOUT353	-146.98	256
614	SOUT502	2022.65	125	664	SOUT452	1322.77	125	714	SOUT402	622.90	125	764	SOUT352	-160.98	125
615	SOUT501	2008.65	256	665	SOUT451	1308.77	256	715	SOUT401	608.90	256	765	SOUT351	-174.98	256
616	SOUT500	1994.65	125	666	SOUT450	1294.78	125	716	SOUT400	594.90	125	766	SOUT350	-188.97	125
617	SOUT499	1980.65	256	667	SOUT449	1280.78	256	717	SOUT399	580.90	256	767	SOUT349	-202.97	256
618	SOUT498	1966.66	125	668	SOUT448	1266.78	125	718	SOUT398	566.91	125	768	SOUT348	-216.97	125
619	SOUT497	1952.66	256	669	SOUT447	1252.78	256	719	SOUT397	552.91	256	769	SOUT347	-230.97	256
620	SOUT496	1938.66	125	670	SOUT446	1238.79	125	720	SOUT396	538.91	125	770	SOUT346	-244.96	125
621	SOUT495	1924.66	256	671	SOUT445	1224.79	256	721	SOUT395	524.91	256	771	SOUT345	-258.96	256
622	SOUT494	1910.67	125	672	SOUT444	1210.79	125	722	SOUT394	510.92	125	772	SOUT344	-272.96	125
623	SOUT493	1896.67	256	673	SOUT443	1196.79	256	723	SOUT393	496.92	256	773	SOUT343	-286.96	256
624	SOUT492	1882.67	125	674	SOUT442	1182.80	125	724	SOUT392	482.92	125	774	SOUT342	-300.95	125
625	SOUT491	1868.67	256	675	SOUT441	1168.80	256	725	SOUT391	468.92	256	775	SOUT341	-314.95	256
626	SOUT490	1854.68	125	676	SOUT440	1154.80	125	726	SOUT390	454.93	125	776	SOUT340	-328.95	125
627	SOUT489	1840.68	256	677	SOUT439	1140.80	256	727	SOUT389	440.93	256	777	SOUT339	-342.95	256
628	SOUT488	1826.68	125	678	SOUT438	1126.81	125	728	SOUT388	426.93	125	778	SOUT338	-356.94	125
629	SOUT487	1812.68	256	679	SOUT437	1112.81	256	729	SOUT387	412.93	256	779	SOUT337	-370.94	256
630	SOUT486	1798.69	125	680	SOUT436	1098.81	125	730	SOUT386	398.94	125	780	SOUT336	-384.94	125
631	SOUT485	1784.69	256	681	SOUT435	1084.81	256	731	SOUT385	384.94	256	781	SOUT335	-398.94	256
632	SOUT484	1770.69	125	682	SOUT434	1070.82	125	732	SOUT384	370.94	125	782	SOUT334	-412.93	125
633	SOUT483	1756.69	256	683	SOUT433	1056.82	256	733	SOUT383	356.94	256	783	SOUT333	-426.93	256
634	SOUT482	1742.70	125	684	SOUT432	1042.82	125	734	SOUT382	342.95	125	784	SOUT332	-440.93	125
635	SOUT481	1728.70	256	685	SOUT431	1028.82	256	735	SOUT381	328.95	256	785	SOUT331	-454.93	256
636	SOUT480	1714.70	125	686	SOUT430	1014.83	125	736	SOUT380	314.95	125	786	SOUT330	-468.92	125
637	SOUT479	1700.70	256	687	SOUT429	1000.83	256	737	SOUT379	300.95	256	787	SOUT329	-482.92	256
638	SOUT478	1686.71	125	688	SOUT428	986.83	125	738	SOUT378	286.96	125	788	SOUT328	-496.92	125
639	SOUT477	1672.71	256	689	SOUT427	972.83	256	739	SOUT377	272.96	256	789	SOUT327	-510.92	256
640	SOUT476	1658.71	125	690	SOUT426	958.84	125	740	SOUT376	258.96	125	790	SOUT326	-524.91	125
641	SOUT475	1644.71	256	691	SOUT425	944.84	256	741	SOUT375	244.96	256	791	SOUT325	-538.91	256
642	SOUT474	1630.72	125	692	SOUT424	930.84	125	742	SOUT374	230.97	125	792	SOUT324	-552.91	125
643	SOUT473	1616.72	256	693	SOUT423	916.84	256	743	SOUT373	216.97	256	793	SOUT323	-566.91	256
644	SOUT472	1602.72	125	694	SOUT422	902.85	125	744	SOUT372	202.97	125	794	SOUT322	-580.90	125
645	SOUT471	1588.72	256	695	SOUT421	888.85	256	745	SOUT371	188.97	256	795	SOUT321	-594.90	256
646	SOUT470	1574.73	125	696	SOUT420	874.85	125	746	SOUT370	174.98	125	796	SOUT320	-608.90	125
647	SOUT469	1560.73	256	697	SOUT419	860.85	256	747	SOUT369	160.98	256	797	SOUT319	-622.90	256
648	SOUT468	1546.73	125	698	SOUT418	846.86	125	748	SOUT368	146.98	125	798	SOUT318	-636.89	125
649	SOUT467	1532.73	256	699	SOUT417	832.86	256	749	SOUT367	132.98	256	799	SOUT317	-650.89	256
650	SOUT466	1518.74	125	700	SOUT416	818.86	125	750	SOUT366	118.99	125	800	SOUT316	-664.89	125

No.	Pad name	X	Y
801	SOUT315	-678.89	256
802	SOUT314	-692.88	125
803	SOUT313	-706.88	256
804	SOUT312	-720.88	125
805	SOUT311	-734.88	256
806	SOUT310	-748.87	125
807	SOUT309	-762.87	256
808	SOUT308	-776.87	125
809	SOUT307	-790.87	256
810	SOUT306	-804.86	125
811	SOUT305	-818.86	256
812	SOUT304	-832.86	125
813	SOUT303	-846.86	256
814	SOUT302	-860.85	125
815	SOUT301	-874.85	256
816	SOUT300	-888.85	125
817	SOUT299	-902.85	256
818	SOUT298	-916.84	125
819	SOUT297	-930.84	256
820	SOUT296	-944.84	125
821	SOUT295	-958.84	256
822	SOUT294	-972.83	125
823	SOUT293	-986.83	256
824	SOUT292	-1000.83	125
825	SOUT291	-1014.83	256
826	SOUT290	-1028.82	125
827	SOUT289	-1042.82	256
828	SOUT288	-1056.82	125
829	SOUT287	-1070.82	256
830	SOUT286	-1084.81	125
831	SOUT285	-1098.81	256
832	SOUT284	-1112.81	125
833	SOUT283	-1126.81	256
834	SOUT282	-1140.80	125
835	SOUT281	-1154.80	256
836	SOUT280	-1168.80	125
837	SOUT279	-1182.80	256
838	SOUT278	-1196.79	125
839	SOUT277	-1210.79	256
840	SOUT276	-1224.79	125
841	SOUT275	-1238.79	256
842	SOUT274	-1252.78	125
843	SOUT273	-1266.78	256
844	SOUT272	-1280.78	125
845	SOUT271	-1294.78	256
846	SOUT270	-1308.77	125
847	SOUT269	-1322.77	256
848	SOUT268	-1336.77	125
849	SOUT267	-1350.77	256
850	SOUT266	-1364.76	125
851	SOUT265	-1378.76	256
852	SOUT264	-1392.76	125
853	SOUT263	-1406.76	256
854	SOUT262	-1420.75	125
855	SOUT261	-1434.75	256
856	SOUT260	-1448.75	125
857	SOUT259	-1462.75	256
858	SOUT258	-1476.74	125
859	SOUT257	-1490.74	256
860	SOUT256	-1504.74	125
861	SOUT255	-1518.74	256
862	SOUT254	-1532.73	125
863	SOUT253	-1546.73	256
864	SOUT252	-1560.73	125
865	SOUT251	-1574.73	256
866	SOUT250	-1588.72	125
867	SOUT249	-1602.72	256
868	SOUT248	-1616.72	125
869	SOUT247	-1630.72	256
870	SOUT246	-1644.71	125
871	SOUT245	-1658.71	256
872	SOUT244	-1672.71	125
873	SOUT243	-1686.71	256
874	SOUT242	-1700.70	125
875	SOUT241	-1714.70	256
876	SOUT240	-1728.70	125
877	SOUT239	-1742.70	256
878	SOUT238	-1756.69	125
879	SOUT237	-1770.69	256
880	SOUT236	-1784.69	125
881	SOUT235	-1798.69	256
882	SOUT234	-1812.68	125
883	SOUT233	-1826.68	256
884	SOUT232	-1840.68	125
885	SOUT231	-1854.68	256
886	SOUT230	-1868.67	125
887	SOUT229	-1882.67	256
888	SOUT228	-1896.67	125
889	SOUT227	-1910.67	256
890	SOUT226	-1924.66	125
891	SOUT225	-1938.66	256
892	SOUT224	-1952.66	125
893	SOUT223	-1966.66	256
894	SOUT222	-1980.65	125
895	SOUT221	-1994.65	256
896	SOUT220	-2008.65	125
897	SOUT219	-2022.65	256
898	SOUT218	-2036.64	125
899	SOUT217	-2050.64	256
900	SOUT216	-2064.64	125
901	SOUT215	-2078.64	256
902	SOUT214	-2092.63	125
903	SOUT213	-2106.63	256
904	SOUT212	-2120.63	125
905	SOUT211	-2134.63	256
906	SOUT210	-2148.62	125
907	SOUT209	-2162.62	256
908	SOUT208	-2176.62	125
909	SOUT207	-2190.62	256
910	SOUT206	-2204.61	125
911	SOUT205	-2218.61	256
912	SOUT204	-2232.61	125
913	SOUT203	-2246.61	256
914	SOUT202	-2260.60	125
915	SOUT201	-2274.60	256
916	SOUT200	-2288.60	125
917	SOUT199	-2302.60	256
918	SOUT198	-2316.59	125
919	SOUT197	-2330.59	256
920	SOUT196	-2344.59	125
921	SOUT195	-2358.59	256
922	SOUT194	-2372.58	125
923	SOUT193	-2386.58	256
924	SOUT192	-2400.58	125
925	SOUT191	-2414.58	256
926	SOUT190	-2428.57	125
927	SOUT189	-2442.57	256
928	SOUT188	-2456.57	125
929	SOUT187	-2470.57	256
930	SOUT186	-2484.56	125
931	SOUT185	-2498.56	256
932	SOUT184	-2512.56	125
933	SOUT183	-2526.56	256
934	SOUT182	-2540.55	125
935	SOUT181	-2554.55	256
936	SOUT180	-2568.55	125
937	SOUT179	-2582.55	256
938	SOUT178	-2596.54	125
939	SOUT177	-2610.54	256
940	SOUT176	-2624.54	125
941	SOUT175	-2638.54	256
942	SOUT174	-2652.53	125
943	SOUT173	-2666.53	256
944	SOUT172	-2680.53	125
945	SOUT171	-2694.53	256
946	SOUT170	-2708.52	125
947	SOUT169	-2722.52	256
948	SOUT168	-2736.52	125
949	SOUT167	-2750.52	256
950	SOUT166	-2764.51	125
951	SOUT165	-2778.51	256
952	SOUT164	-2792.51	125
953	SOUT163	-2806.51	256
954	SOUT162	-2820.50	125
955	SOUT161	-2834.50	256
956	SOUT160	-2848.50	125
957	SOUT159	-2862.50	256
958	SOUT158	-2876.49	125
959	SOUT157	-2890.49	256
960	SOUT156	-2904.49	125
961	SOUT155	-2918.49	256
962	SOUT154	-2932.48	125
963	SOUT153	-2946.48	256
964	SOUT152	-2960.48	125
965	SOUT151	-2974.48	256
966	SOUT150	-2988.47	125
967	SOUT149	-3002.47	256
968	SOUT148	-3016.47	125
969	SOUT147	-3030.47	256
970	SOUT146	-3044.46	125
971	SOUT145	-3058.46	256
972	SOUT144	-3072.46	125
973	SOUT143	-3086.46	256
974	SOUT142	-3100.45	125
975	SOUT141	-3114.45	256
976	SOUT140	-3128.45	125
977	SOUT139	-3142.45	256
978	SOUT138	-3156.44	125
979	SOUT137	-3170.44	256
980	SOUT136	-3184.44	125
981	SOUT135	-3198.44	256
982	SOUT134	-3212.43	125
983	SOUT133	-3226.43	256
984	SOUT132	-3240.43	125
985	SOUT131	-3254.43	256
986	SOUT130	-3268.42	125
987	SOUT129	-3282.42	256
988	SOUT128	-3296.42	125
989	SOUT127	-3310.42	256
990	SOUT126	-3324.41	125
991	SOUT125	-3338.41	256
992	SOUT124	-3352.41	125
993	SOUT123	-3366.41	256
994	SOUT122	-3380.40	125
995	SOUT121	-3394.40	256
996	SOUT120	-3408.40	125
997	SOUT119	-3422.40	256
998	SOUT118	-3436.39	125
999	SOUT117	-3450.39	256
1000	SOUT116	-3464.39	125

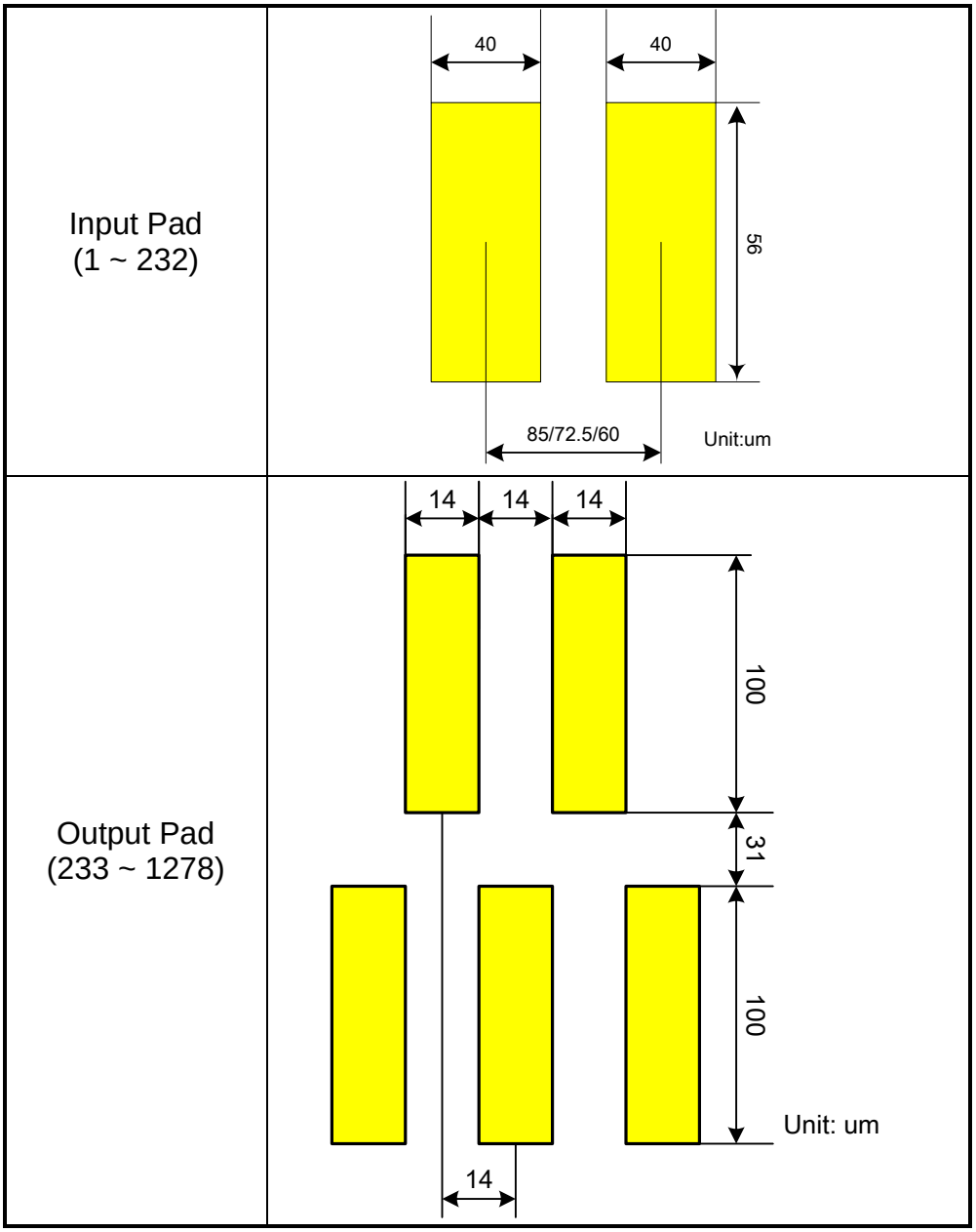
No.	Pad name	X	Y
1001	SOUT115	-3478.39	256
1002	SOUT114	-3492.38	125
1003	SOUT113	-3506.38	256
1004	SOUT112	-3520.38	125
1005	SOUT111	-3534.38	256
1006	SOUT110	-3548.37	125
1007	SOUT109	-3562.37	256
1008	SOUT108	-3576.37	125
1009	SOUT107	-3590.37	256
1010	SOUT106	-3604.36	125
1011	SOUT105	-3618.36	256
1012	SOUT104	-3632.36	125
1013	SOUT103	-3646.36	256
1014	SOUT102	-3660.35	125
1015	SOUT101	-3674.35	256
1016	SOUT100	-3688.35	125
1017	SOUT99	-3702.35	256
1018	SOUT98	-3716.34	125
1019	SOUT97	-3730.34	256
1020	SOUT96	-3744.34	125
1021	SOUT95	-3758.34	256
1022	SOUT94	-3772.33	125
1023	SOUT93	-3786.33	256
1024	SOUT92	-3800.33	125
1025	SOUT91	-3814.33	256
1026	SOUT90	-3828.32	125
1027	SOUT89	-3842.32	256
1028	SOUT88	-3856.32	125
1029	SOUT87	-3870.32	256
1030	SOUT86	-3884.31	125
1031	SOUT85	-3898.31	256
1032	SOUT84	-3912.31	125
1033	SOUT83	-3926.31	256
1034	SOUT82	-3940.30	125
1035	SOUT81	-3954.30	256
1036	SOUT80	-3968.30	125
1037	SOUT79	-3982.30	256
1038	SOUT78	-3996.29	125
1039	SOUT77	-4010.29	256
1040	SOUT76	-4024.29	125
1041	SOUT75	-4038.29	256
1042	SOUT74	-4052.28	125
1043	SOUT73	-4066.28	256
1044	SOUT72	-4080.28	125
1045	SOUT71	-4094.28	256
1046	SOUT70	-4108.27	125
1047	SOUT69	-4122.27	256
1048	SOUT68	-4136.27	125
1049	SOUT67	-4150.27	256
1050	SOUT66	-4164.26	125
1051	SOUT65	-4178.26	256
1052	SOUT64	-4192.26	125
1053	SOUT63	-4206.26	256
1054	SOUT62	-4220.25	125
1055	SOUT61	-4234.25	256
1056	SOUT60	-4248.25	125
1057	SOUT59	-4262.25	256
1058	SOUT58	-4276.24	125
1059	SOUT57	-4290.24	256
1060	SOUT56	-4304.24	125
1061	SOUT55	-4318.24	256
1062	SOUT54	-4332.23	125
1063	SOUT53	-4346.23	256
1064	SOUT52	-4360.23	125
1065	SOUT51	-4374.23	256
1066	SOUT50	-4388.22	125
1067	SOUT49	-4402.22	256
1068	SOUT48	-4416.22	125
1069	SOUT47	-4430.22	256
1070	SOUT46	-4444.21	125
1071	SOUT45	-4458.21	256
1072	SOUT44	-4472.21	125
1073	SOUT43	-4486.21	256
1074	SOUT42	-4500.20	125
1075	SOUT41	-4514.20	256
1076	SOUT40	-4528.20	125
1077	SOUT39	-4542.20	256
1078	SOUT38	-4556.19	125
1079	SOUT37	-4570.19	256
1080	SOUT36	-4584.19	125
1081	SOUT35	-4598.19	256
1082	SOUT34	-4612.18	125
1083	SOUT33	-4626.18	256
1084	SOUT32	-4640.18	125
1085	SOUT31	-4654.18	256
1086	SOUT30	-4668.17	125
1087	SOUT29	-4682.17	256
1088	SOUT28	-4696.17	125
1089	SOUT27	-4710.17	256
1090	SOUT26	-4724.16	125
1091	SOUT25	-4738.16	256
1092	SOUT24	-4752.16	125
1093	SOUT23	-4766.16	256
1094	SOUT22	-4780.15	125
1095	SOUT21	-4794.15	256
1096	SOUT20	-4808.15	125
1097	SOUT19	-4822.15	256
1098	SOUT18	-4836.14	125
1099	SOUT17	-4850.14	256
1100	SOUT16	-4864.14	125
1101	SOUT15	-4878.14	256
1102	SOUT14	-4892.13	125
1103	SOUT13	-4906.13	256
1104	SOUT12	-4920.13	125
1105	SOUT11	-4934.13	256
1106	SOUT10	-4948.12	125
1107	SOUT9	-4962.12	256
1108	SOUT8	-4976.12	125
1109	SOUT7	-4990.12	256
1110	SOUT6	-5004.11	125
1111	SOUT5	-5018.11	256
1112	SOUT4	-5032.11	125
1113	SOUT3	-5046.11	256
1114	SOUT2	-5060.10	125
1115	SOUT1	-5074.10	256
1116	GOUT319	-5130.10	125
1117	GOUT317	-5144.10	256
1118	GOUT315	-5158.09	125
1119	GOUT313	-5172.09	256
1120	GOUT311	-5186.09	125
1121	GOUT309	-5200.09	256
1122	GOUT307	-5214.08	125
1123	GOUT305	-5228.08	256
1124	GOUT303	-5242.08	125
1125	GOUT301	-5256.08	256
1126	GOUT299	-5270.07	125
1127	GOUT297	-5284.07	256
1128	GOUT295	-5298.07	125
1129	GOUT293	-5312.07	256
1130	GOUT291	-5326.06	125
1131	GOUT289	-5340.06	256
1132	GOUT287	-5354.06	125
1133	GOUT285	-5368.06	256
1134	GOUT283	-5382.05	125
1135	GOUT281	-5396.05	256
1136	GOUT279	-5410.05	125
1137	GOUT277	-5424.05	256
1138	GOUT275	-5438.04	125
1139	GOUT273	-5452.04	256
1140	GOUT271	-5466.04	125
1141	GOUT269	-5480.04	256
1142	GOUT267	-5494.03	125
1143	GOUT265	-5508.03	256
1144	GOUT263	-5522.03	125
1145	GOUT261	-5536.03	256
1146	GOUT259	-5550.02	125
1147	GOUT257	-5564.02	256
1148	GOUT255	-5578.02	125
1149	GOUT253	-5592.02	256
1150	GOUT251	-5606.01	125
1151	GOUT249	-5620.01	256
1152	GOUT247	-5634.01	125
1153	GOUT245	-5648.01	256
1154	GOUT243	-5662.00	125
1155	GOUT241	-5676.00	256
1156	GOUT239	-5690.00	125
1157	GOUT237	-5704.00	256
1158	GOUT235	-5717.99	125
1159	GOUT233	-5731.99	256
1160	GOUT231	-5745.99	125
1161	GOUT229	-5759.99	256
1162	GOUT227	-5773.98	125
1163	GOUT225	-5787.98	256
1164	GOUT223	-5801.98	125
1165	GOUT221	-5815.98	256
1166	GOUT219	-5829.97	125
1167	GOUT217	-5843.97	256
1168	GOUT215	-5857.97	125
1169	GOUT213	-5871.97	256
1170	GOUT211	-5885.96	125
1171	GOUT209	-5899.96	256
1172	GOUT207	-5913.96	125
1173	GOUT205	-5927.96	256
1174	GOUT203	-5941.95	125
1175	GOUT201	-5955.95	256
1176	GOUT199	-5969.95	125
1177	GOUT197	-5983.95	256
1178	GOUT195	-5997.94	125
1179	GOUT193	-6011.94	256
1180	GOUT191	-6025.94	125
1181	GOUT189	-6039.94	256
1182	GOUT187	-6053.93	125
1183	GOUT185	-6067.93	256
1184	GOUT183	-6081.93	125
1185	GOUT181	-6095.93	256
1186	GOUT179	-6109.92	125
1187	GOUT177	-6123.92	256
1188	GOUT175	-6137.92	125
1189	GOUT173	-6151.92	256
1190	GOUT171	-6165.91	125
1191	GOUT169	-6179.91	256
1192	GOUT167	-6193.91	125
1193	GOUT165	-6207.91	256
1194	GOUT163	-6221.90	125
1195	GOUT161	-6235.90	256
1196	GOUT159	-6249.90	125
1197	GOUT157	-6263.90	256
1198	GOUT155	-6277.89	125
1199	GOUT153	-6291.89	256
1200	GOUT151	-6305.89	125

No.	Pad name	X	Y
1201	GOUT149	-6319.89	256
1202	GOUT147	-6333.88	125
1203	GOUT145	-6347.88	256
1204	GOUT143	-6361.88	125
1205	GOUT141	-6375.88	256
1206	GOUT139	-6389.87	125
1207	GOUT137	-6403.87	256
1208	GOUT135	-6417.87	125
1209	GOUT133	-6431.87	256
1210	GOUT131	-6445.86	125
1211	GOUT129	-6459.86	256
1212	GOUT127	-6473.86	125
1213	GOUT125	-6487.86	256
1214	GOUT123	-6501.85	125
1215	GOUT121	-6515.85	256
1216	GOUT119	-6529.85	125
1217	GOUT117	-6543.85	256
1218	GOUT115	-6557.84	125
1219	GOUT113	-6571.84	256
1220	GOUT111	-6585.84	125
1221	GOUT109	-6599.84	256
1222	GOUT107	-6613.83	125
1223	GOUT105	-6627.83	256
1224	GOUT103	-6641.83	125
1225	GOUT101	-6655.83	256
1226	GOUT99	-6669.82	125
1227	GOUT97	-6683.82	256
1228	GOUT95	-6697.82	125
1229	GOUT93	-6711.82	256
1230	GOUT91	-6725.81	125
1231	GOUT89	-6739.81	256
1232	GOUT87	-6753.81	125
1233	GOUT85	-6767.81	256
1234	GOUT83	-6781.80	125
1235	GOUT81	-6795.80	256
1236	GOUT79	-6809.80	125
1237	GOUT77	-6823.80	256
1238	GOUT75	-6837.79	125
1239	GOUT73	-6851.79	256
1240	GOUT71	-6865.79	125
1241	GOUT69	-6879.79	256
1242	GOUT67	-6893.78	125
1243	GOUT65	-6907.78	256
1244	GOUT63	-6921.78	125
1245	GOUT61	-6935.78	256
1246	GOUT59	-6949.77	125
1247	GOUT57	-6963.77	256
1248	GOUT55	-6977.77	125
1249	GOUT53	-6991.77	256
1250	GOUT51	-7005.76	125

No.	Pad name	X	Y
1251	GOUT49	-7019.76	256
1252	GOUT47	-7033.76	125
1253	GOUT45	-7047.76	256
1254	GOUT43	-7061.75	125
1255	GOUT41	-7075.75	256
1256	GOUT39	-7089.75	125
1257	GOUT37	-7103.75	256
1258	GOUT35	-7117.74	125
1259	GOUT33	-7131.74	256
1260	GOUT31	-7145.74	125
1261	GOUT29	-7159.74	256
1262	GOUT27	-7173.73	125
1263	GOUT25	-7187.73	256
1264	GOUT23	-7201.73	125
1265	GOUT21	-7215.73	256
1266	GOUT19	-7229.72	125
1267	GOUT17	-7243.72	256
1268	GOUT15	-7257.72	125
1269	GOUT13	-7271.72	256
1270	GOUT11	-7285.71	125
1271	GOUT9	-7299.71	256
1272	GOUT7	-7313.71	125
1273	GOUT5	-7327.71	256
1274	GOUT3	-7341.70	125
1275	GOUT1	-7355.70	256
1276	DUMMY	-7369.70	125
1277	DUMMY	-7383.70	256
1278	DUMMY	-7397.69	125

Alignment mark	X	Y
Left COG Align	-7480	253
Right COG Align	7480	253

BUMP Size



6. Block Function Description

MCU System Interface

ILI9340X provides several kinds of MCU system interface with 8080-Ⅰ/8080-Ⅱ series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface Ⅰ	DB[7:0]	DB[7:0],WRX,RDX,CSX,DCX
0	0	0	1	8080 MCU 16-bit bus interface Ⅰ	DB[7:0]	DB[15:0] ,WRX,RDX,CSX,DCX
0	0	1	0	8080 MCU 9-bit bus interface Ⅰ	DB[7:0]	DB[8:0] ,WRX,RDX,CSX,DCX
0	0	1	1	8080 MCU 18-bit bus interface Ⅰ	DB[7:0]	DB[17:0] ,WRX,RDX,CSX,DCX
0	1	0	1	3-line 9-bit data serial interface Ⅰ	SCL,SDA,CSX	
0	1	1	0	4-line 8-bit data serial interface Ⅰ	SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface Ⅱ	DB[8:1]	DB[17:10], DB[8:1] , WRX,RDX,CSX,DCX
1	0	0	1	8080 MCU 8-bit bus interface Ⅱ	DB[17:10]	DB[17:10], WRX,RDX,CSX,DCX
1	0	1	0	8080 MCU 18-bit bus interface Ⅱ	DB[8:1]	DB[17:0] , WRX,RDX,CSX,DCX
1	0	1	1	8080 MCU 9-bit bus interface Ⅱ	DB[17:10]	DB[17:9] , WRX,RDX,CSX,DCX
1	1	0	1	3-line 9-bit data serial interface Ⅱ	SCL,SDI,SDO, CSX	
1	1	1	0	4-line 8-bit data serial interface Ⅱ	SCL,SDI,D/CX,SDO, CSX	

In 8080-Ⅰ/8080-Ⅱ series parallel interface, the registers are accessed by the DB[17:0] data pins.

8080-Ⅰ Series				**8080-Ⅱ Series**				**Operation**
CSX	**DCX**	**RDX**	**WRX**	**CSX**	**DCX**	**RDX**	**WRX**	
"L"	"L"	"H"	↑	"L"	"L"	"H"	↑	Write command
"L"	"H"	↑	"H"	"L"	"H"	↑	"H"	Read parameter
"L"	"H"	"H"	↑	"L"	"H"	"H"	↑	Write parameter

Parallel RGB Interface

ILI9340X also supports the RGB interface for displaying a moving picture. The display data of RGB interface synchronize with external signals - VSYNC, HSYNC, and DOTCLK and the input data are written to ILI9340X according to the polarity of enable signal (ENABLE).

Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 240(RGB) x320 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9340X can display maximum 262,144 colors.

Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as DDVDH, DDVDL, VGH, VGL and VCOM for driving TFT LCD panel.

Timing controller

The timing controller generates all the timing signals for display and GRAM access.

Oscillator

ILI9340X incorporates RC oscillator circuit and output a stable frequency for operation.

Panel Driver Circuit

Liquid crystal display driver circuit consists of 720-output source driver (SOUT1~SOUT720), 320-output gate driver (GOUT1~GOUT320), and VCOM signal.

7. Function Description

7.1. MCU interfaces

ILI9340X provides the 8-/9-/16-/18-bit parallel system interface for 8080-Ⅰ/8080-Ⅱ series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

7.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	MCU-Interface Mode	DB Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface Ⅰ	DB[7:0]	DB[7:0]
0	0	0	1	8080 MCU 16-bit bus interface Ⅰ	DB[7:0]	DB[15:0]
0	0	1	0	8080 MCU 9-bit bus interface Ⅰ	DB[7:0]	DB[8:0]
0	0	1	1	8080 MCU 18-bit bus interface Ⅰ	DB[7:0]	DB[17:0]
0	1	0	1	3-line 9-bit data serial interface Ⅰ	SDA: In/Out	
0	1	1	0	4-line 8-bit data serial interface Ⅰ	SDA: In/Out	
1	0	0	0	8080 MCU 16-bit bus interface Ⅱ	DB[8:1]	DB[17:10], DB[8:1]
1	0	0	1	8080 MCU 8-bit bus interface Ⅱ	DB[17:10]	DB[17:10]
1	0	1	0	8080 MCU 18-bit bus interface Ⅱ	DB[8:1]	DB[17:0]
1	0	1	1	8080 MCU 9-bit bus interface Ⅱ	DB[17:10]	DB [17:9]
1	1	0	1	3-line 9-bit data serial interface Ⅱ	SDI: In SDO: Out	
1	1	1	0	4-line 8-bit data serial interface Ⅱ	SDI: In SDO: Out	

8080-Ⅰ Series Parallel Interface

ILI9340X can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅰ series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9340X chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and DB [17:0] is parallel data bus.

ILI9340X latches the input data at the rising edge of WRX signal. The DCX is the signal of data/command selection. When DCX='1', DB [17:0] bits are display RAM data or command's parameters. When DCX='0', DB [17:0] bits are commands.

The 8080-Ⅰ series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-Ⅰ Interface selection is done when IM3 pin is low state (GND level). Interface bus width can be selected by IM [3:0] bits.

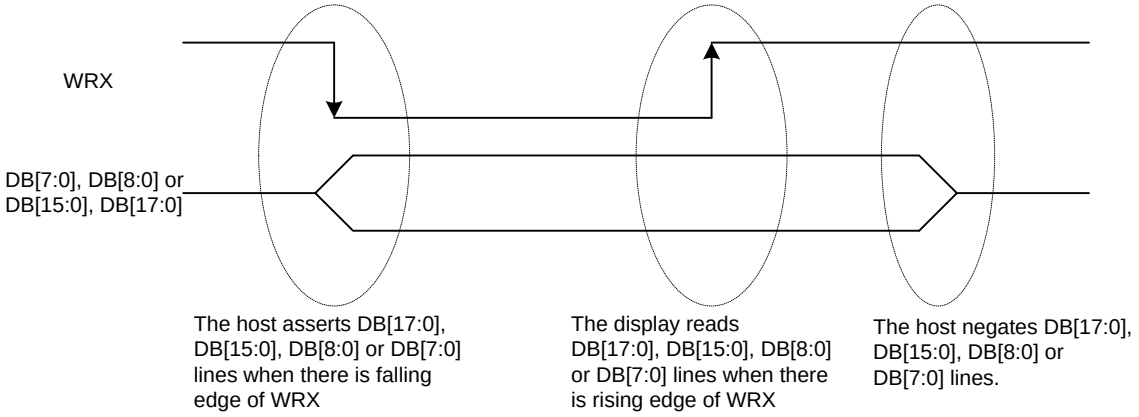
The selection of 8080-Ⅰ series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	DCX	Function
0	0	0	0	8080 MCU 8-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Read parameter or display data.
0	0	0	1	8080 MCU 16-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Read parameter or display data.
0	0	1	0	8080 MCU 9-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Read parameter or display data.
0	0	1	1	8080 MCU 18-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Read parameter or display data.

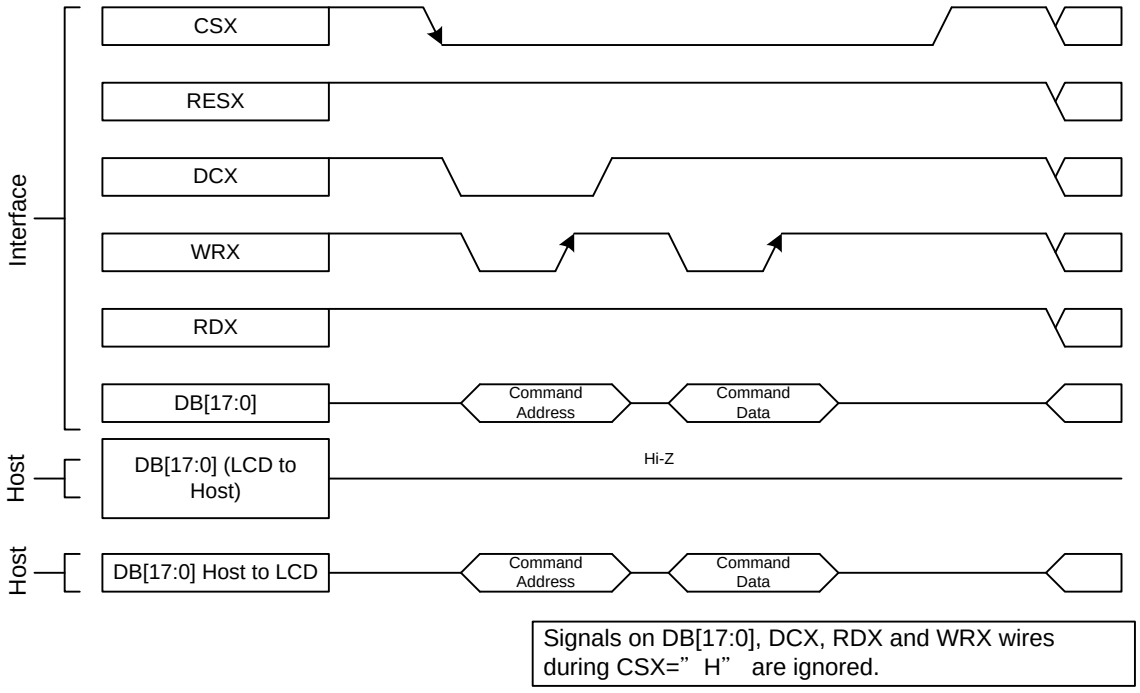
7.1.2. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the DCX signal is driven to low level, then input data on the interface is interpreted as command information. The DCX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080- Ⅰ MCU interface.



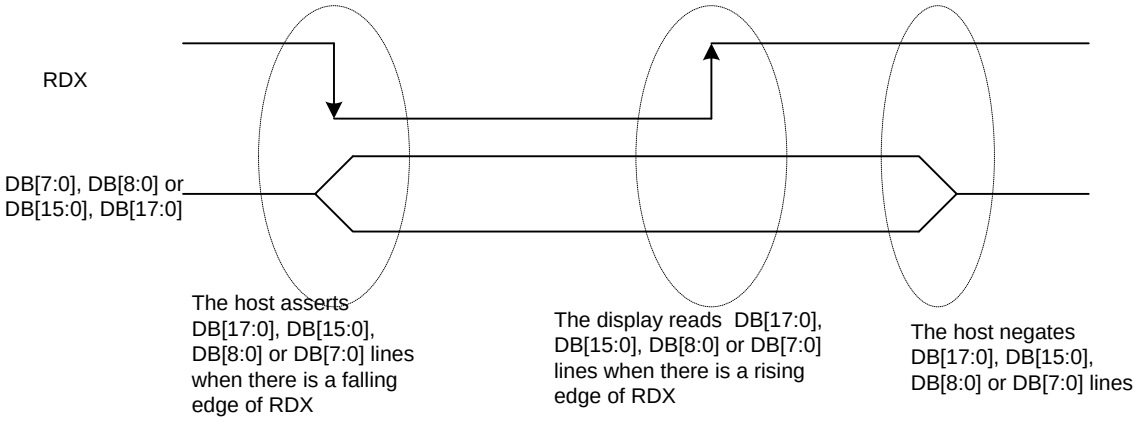
Note: WRX is an unsynchronized signal (It can be stopped)



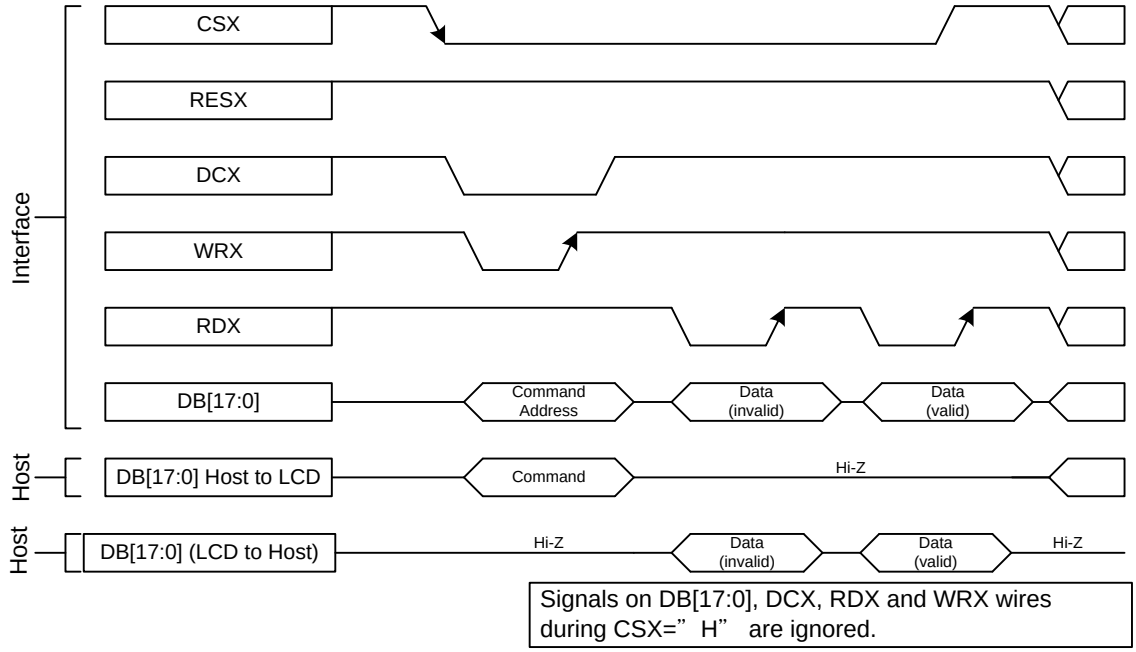
7.1.3. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the DCX signal is driven to low level, then input data on the interface is interpreted as command. The DCX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080- Ⅰ MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the DCX input is pulled high. If DCX is driven low during read then the display information outputs will be High-Z.

7.1.4. 8080-Ⅱ Series Parallel Interface

ILI9340X can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅱ series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9340X chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and DB[17:0] is parallel data bus.

ILI9340X latches the input data at the rising edge of WRX signal. The DCX is the signal of data/command selection. When DCX='1', DB[17:0] bits are display RAM data or command's parameters. When DCX='0', D [17:0] bits are commands.

The 8080-Ⅱ series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-Ⅱ Interface selection is done when IM3 pin is high state (IOVCC level). Interface bus width can be selected by IM [3:0] bits.

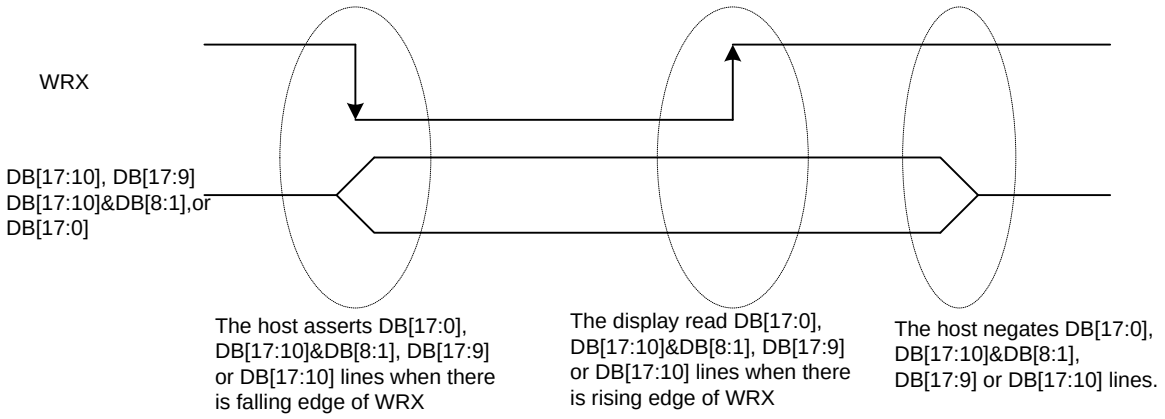
The selection of 8080-Ⅱ series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	DCX	Function
1	0	0	0	8080 MCU 16-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
1	0	0	1	8080 MCU 8-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
1	0	1	0	8080 MCU 18-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
1	0	1	1	8080 MCU 9-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

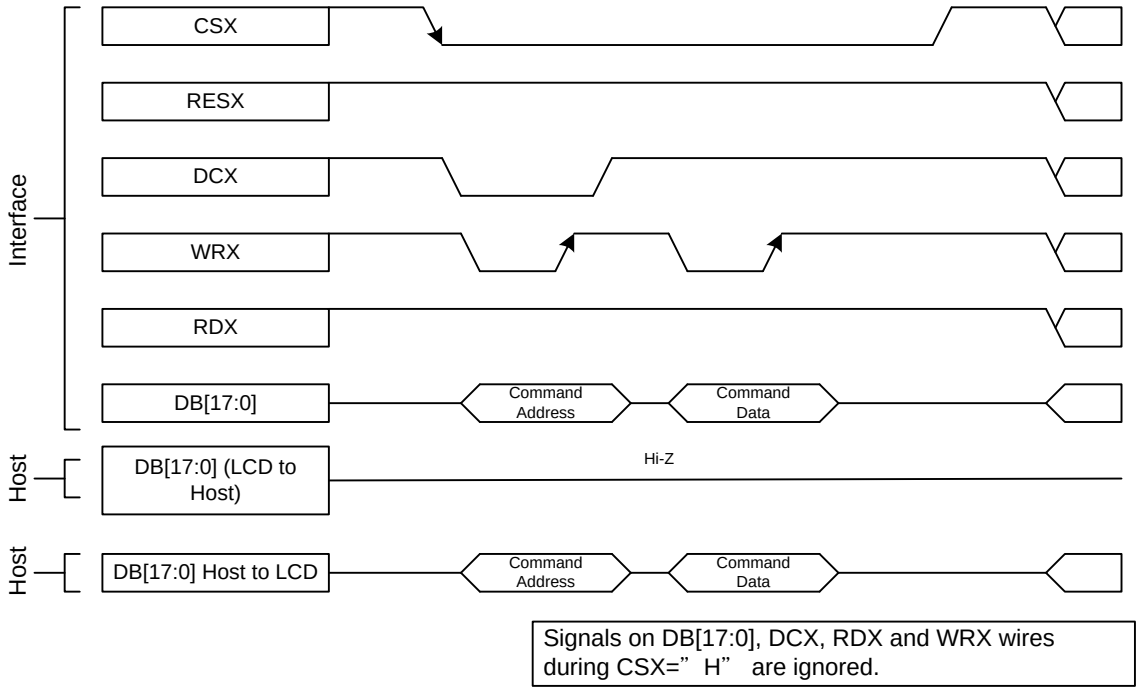
7.1.5. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the DCX signal is driven to low level, then input data on the interface is interpreted as command information. The DCX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-Ⅱ MCU interface.



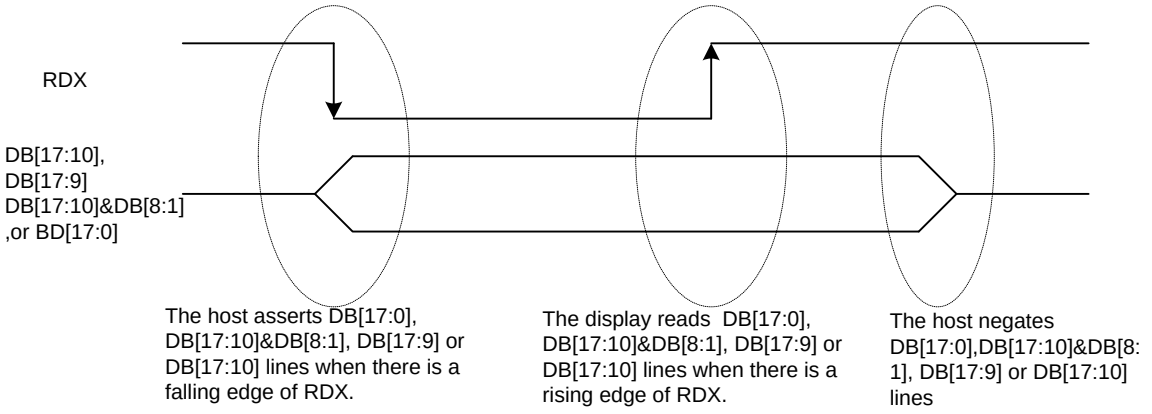
Note: WRX is an unsynchronized signal (It can be stopped)



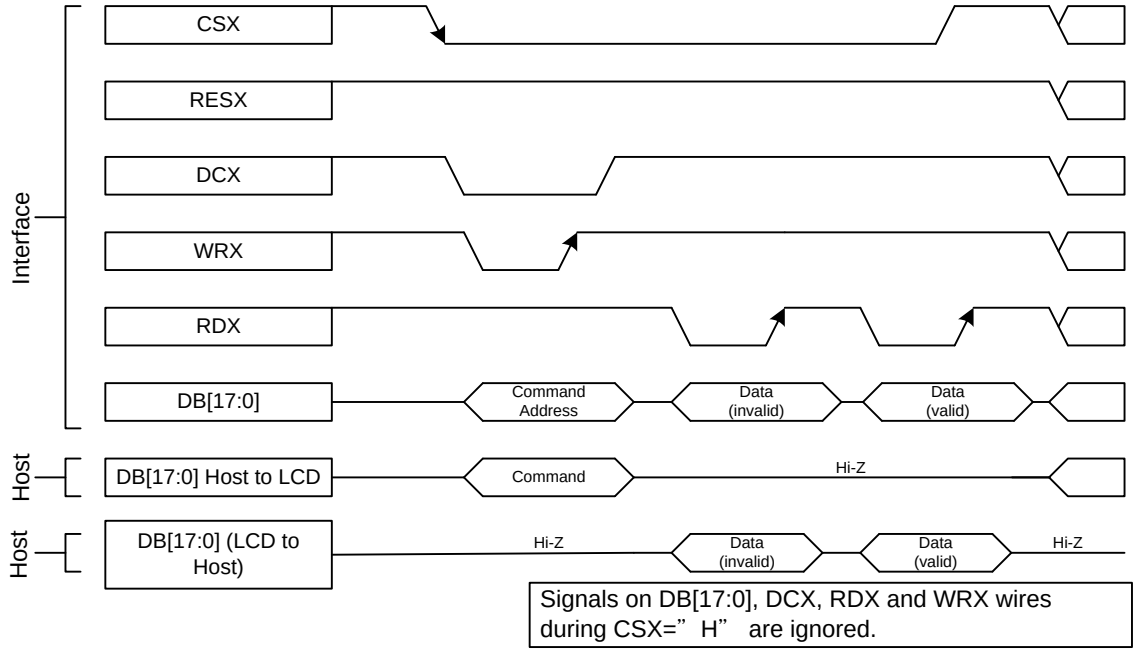
7.1.6. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the DCX signal is driven to low level, then input data on the interface is interpreted as command. The DCX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-Ⅱ MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the DCX input is pulled high. If DCX is driven low during read then the display information outputs will be High-Z.

7.1.7. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	1	0	1	3-line serial interface I	"L"	-	↑	Read/Write command, parameter or display data.
0	1	1	0	4-line serial interface I	"L"	'H/L"	↑	Read/Write command, parameter or display data.
1	1	0	1	3-line serial interface II	"L"	-	↑	Read/Write command, parameter or display data.
1	1	1	0	4-line serial interface II	"L"	'H/L"	↑	Read/Write command, parameter or display data.

ILI9340X supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9340X. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (interface I: SDA or interface II: SDI/SDO). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (DB [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

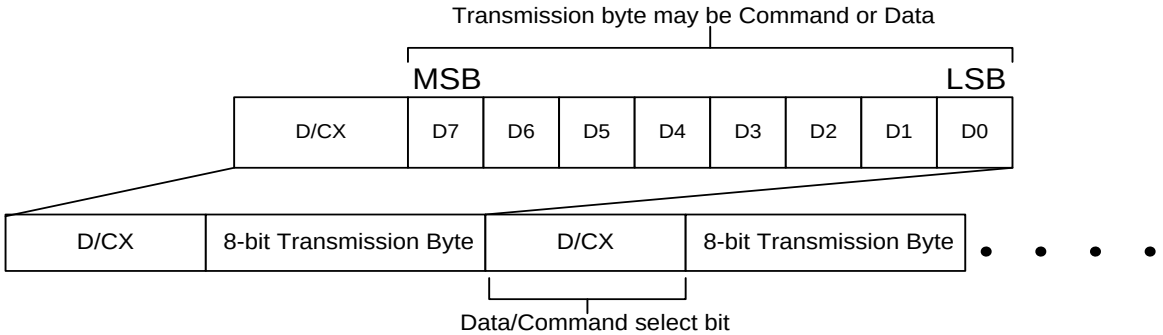
7.1.8. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to ILI9340X. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or as the parameter of command register

.

Any instruction can be sent in any order to ILI9340X and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

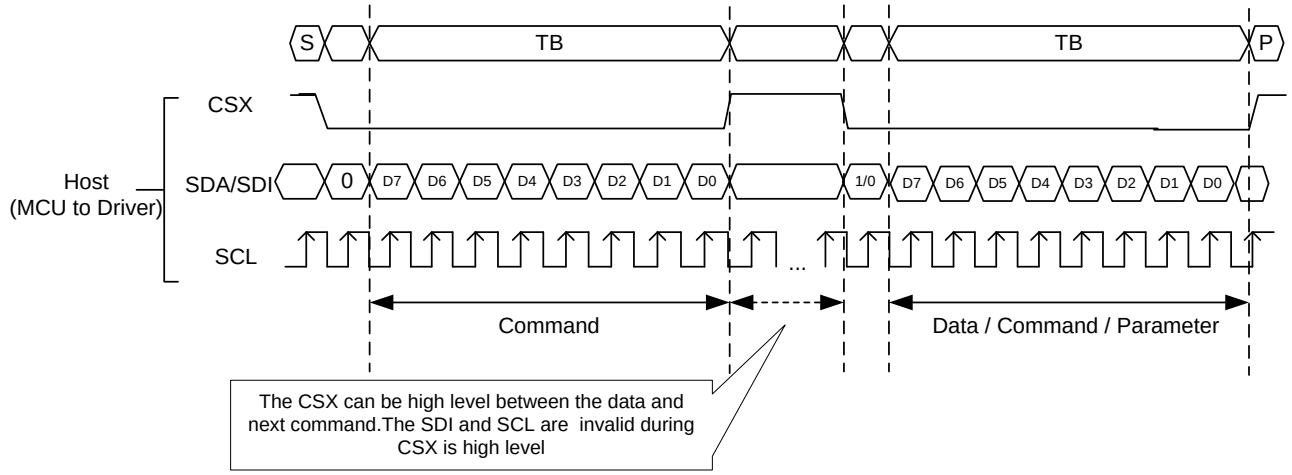
3-line Serial Interface Data Format



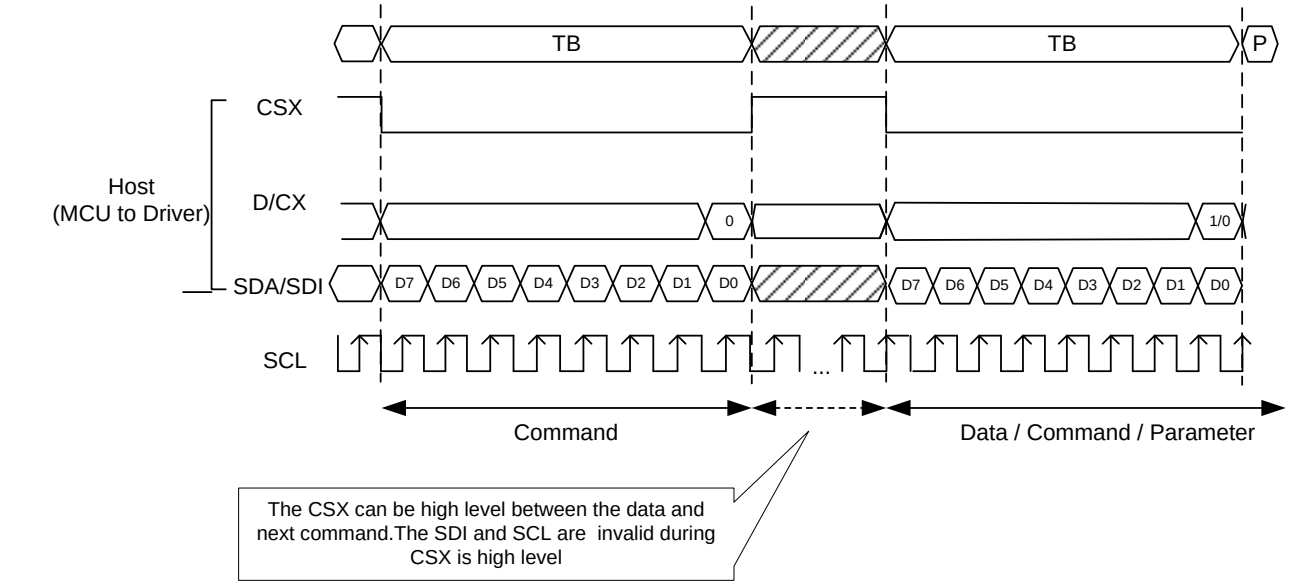
Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9340X on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by

the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. In 4-line Serial Interface Protocol the optional D/CX pin is used, a command or a data is eight cycles width. The 3/4-line serial interface writes sequence described in the figure as below.

3-line Serial Interface Protocol



4-line Serial Interface Protocol



7.1.9. 2-data-lane Serial interface

The 2-data-lane mode of the interface means that host writes pixel data by 2 lines to ILI9340X.

Use the D/CX (command/data select) lane as the additional data lane for 2-data-lane protocol.

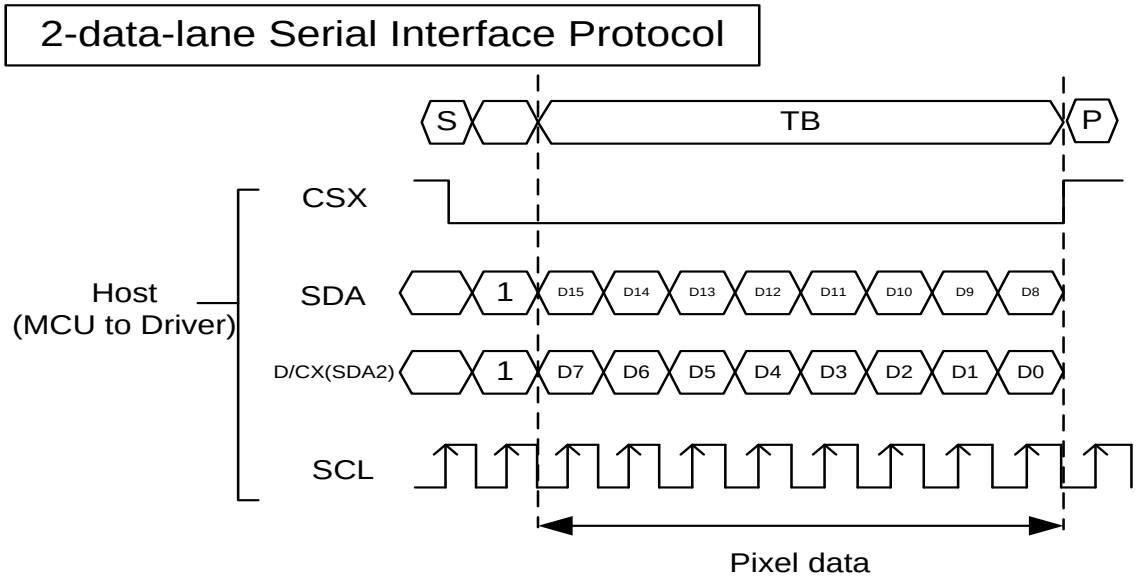
Enable 2-data-Lane in SPI mode:

When bit[1] of command C6h is in “high” level voltage and send command 2Ch at next, it enters the 2-data-lane mode.

Leave 2-data-Lane in SPI mode:

If the MSB of SDA lane sends “low” level voltage(Write any command), it leaves the 2-data-lane mode.

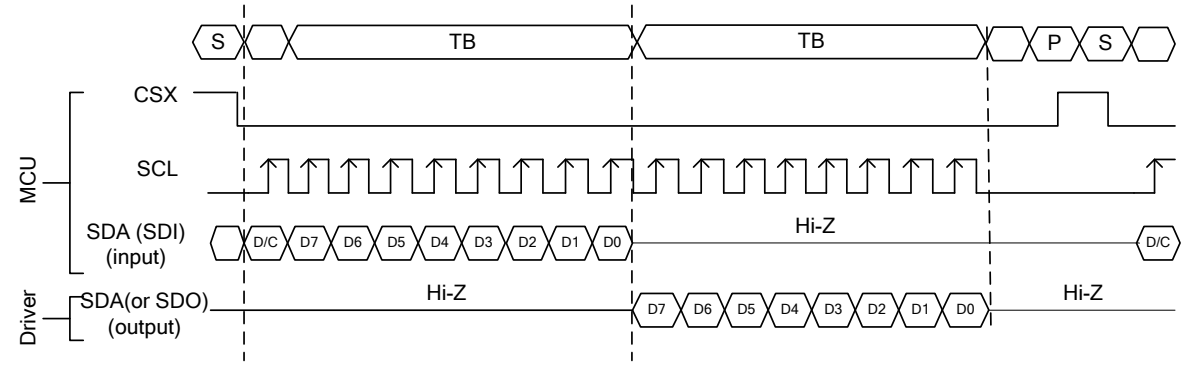
-Only pixel data can be sent in 2-data-lane protocol.



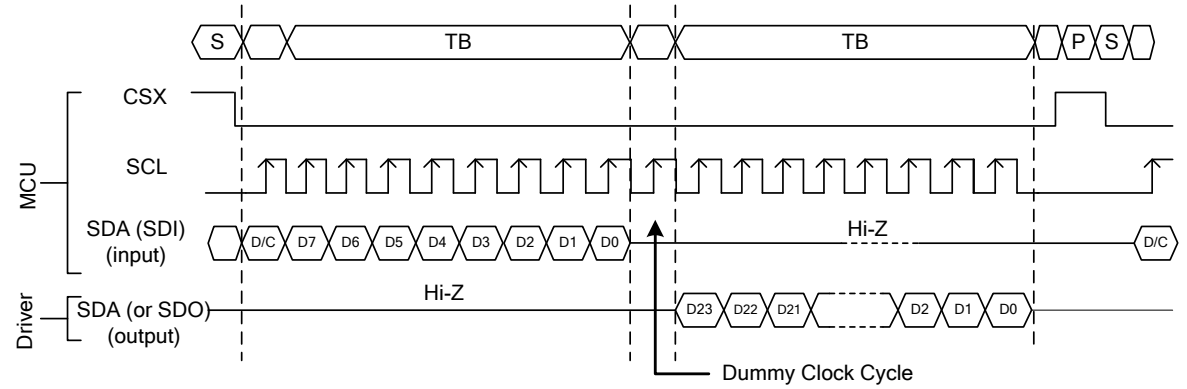
7.1.10. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter or display data from ILI9340X. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9340X latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

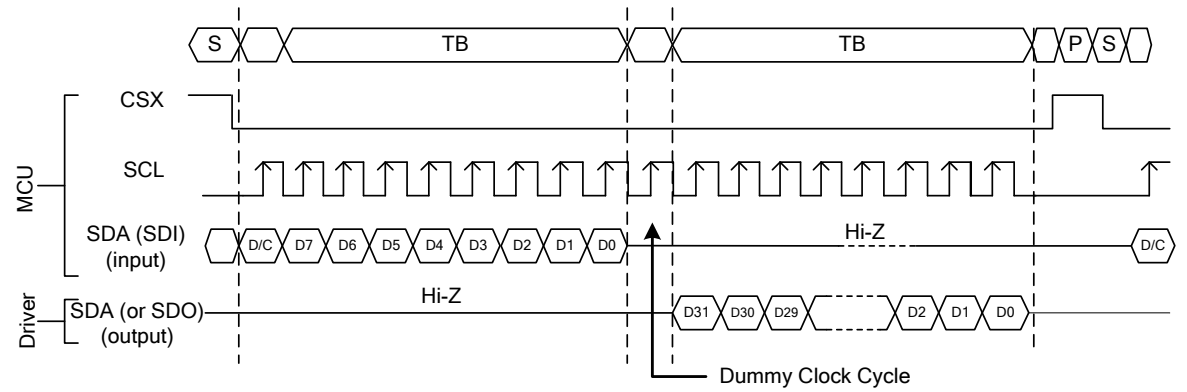
3-line Serial Protocol (for RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



3-line Serial Protocol (for RDDID command: 24-bit read)

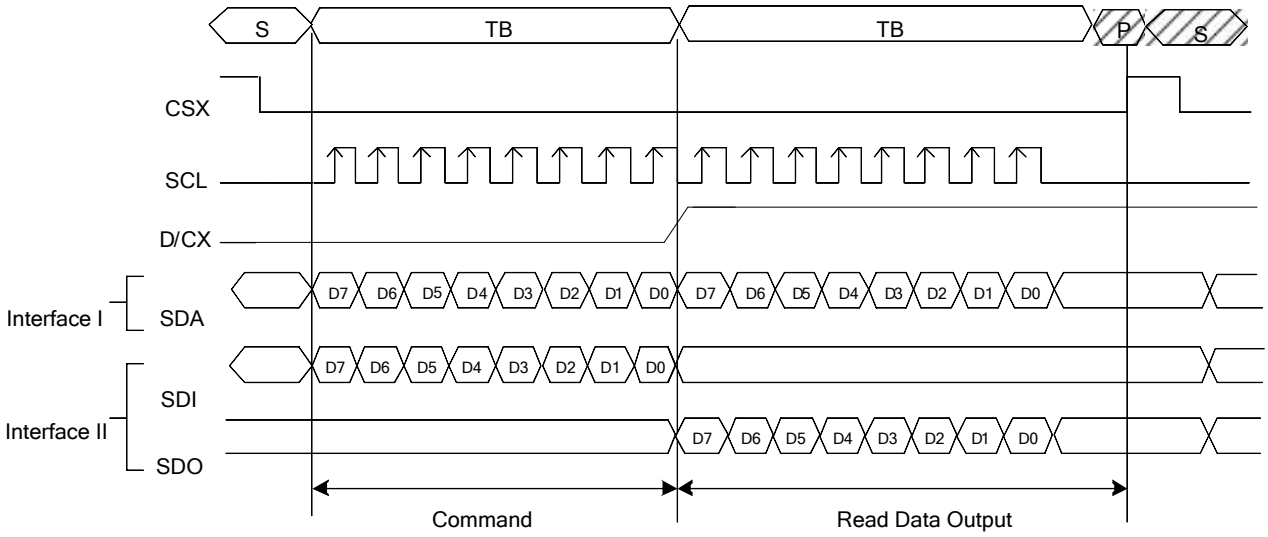


3-line Serial Protocol (for RDDST command: 32-bit read)

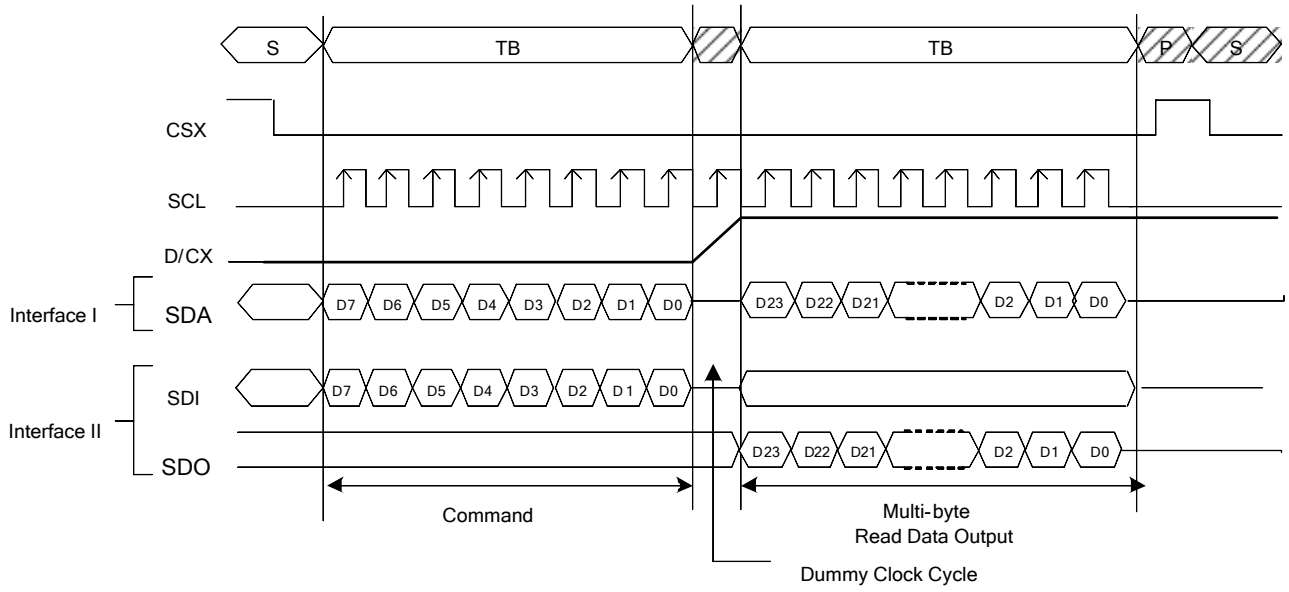


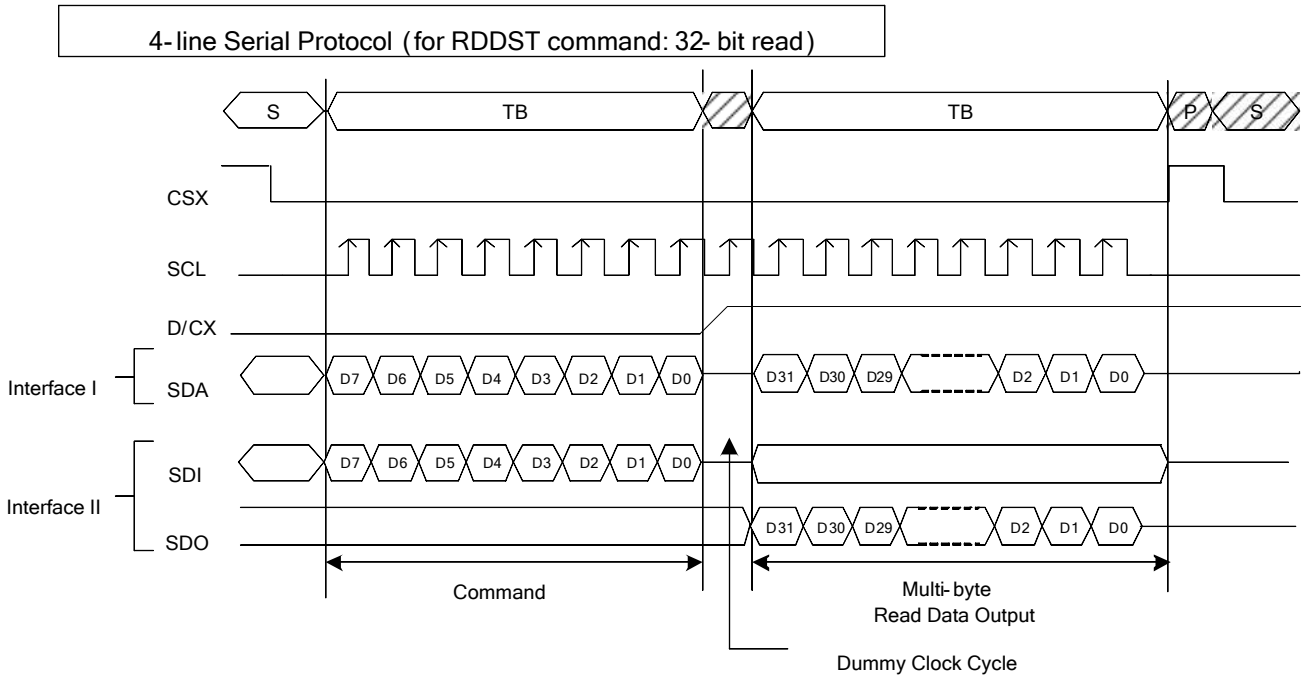
4-line Serial Interface Protocol

4- line Serial Protocol (for RDID1/ RDID2/ RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command 8- bit read)



4- line Serial Protocol (for RDDID command: 24- bit read)

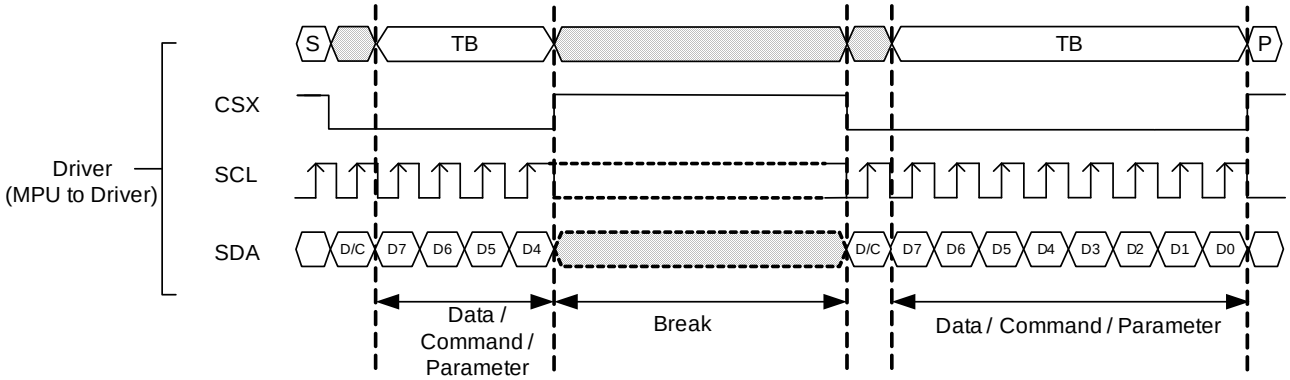




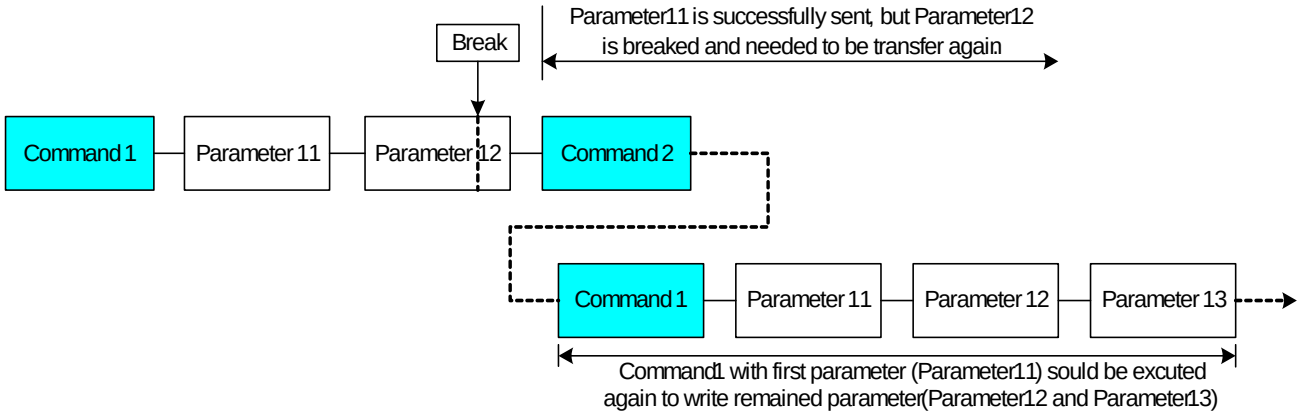
7.1.11. Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

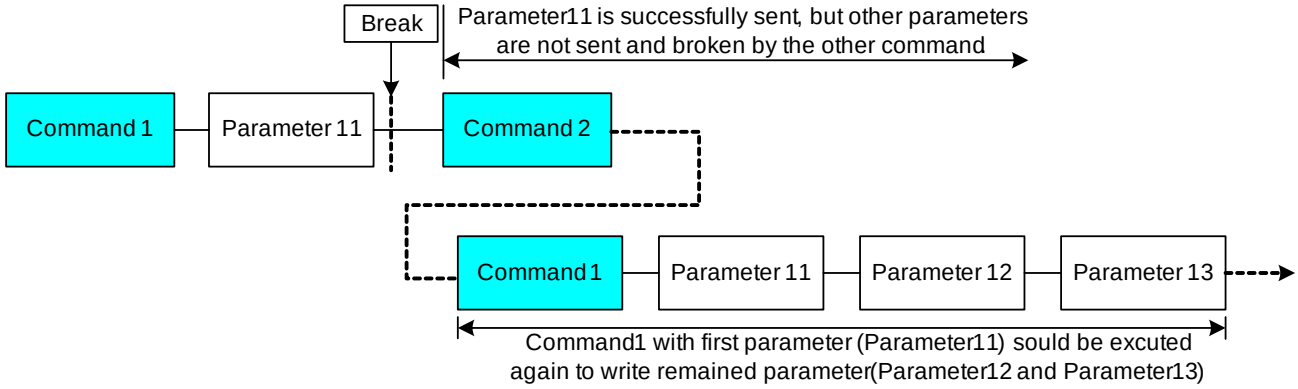
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.



7.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9340X will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

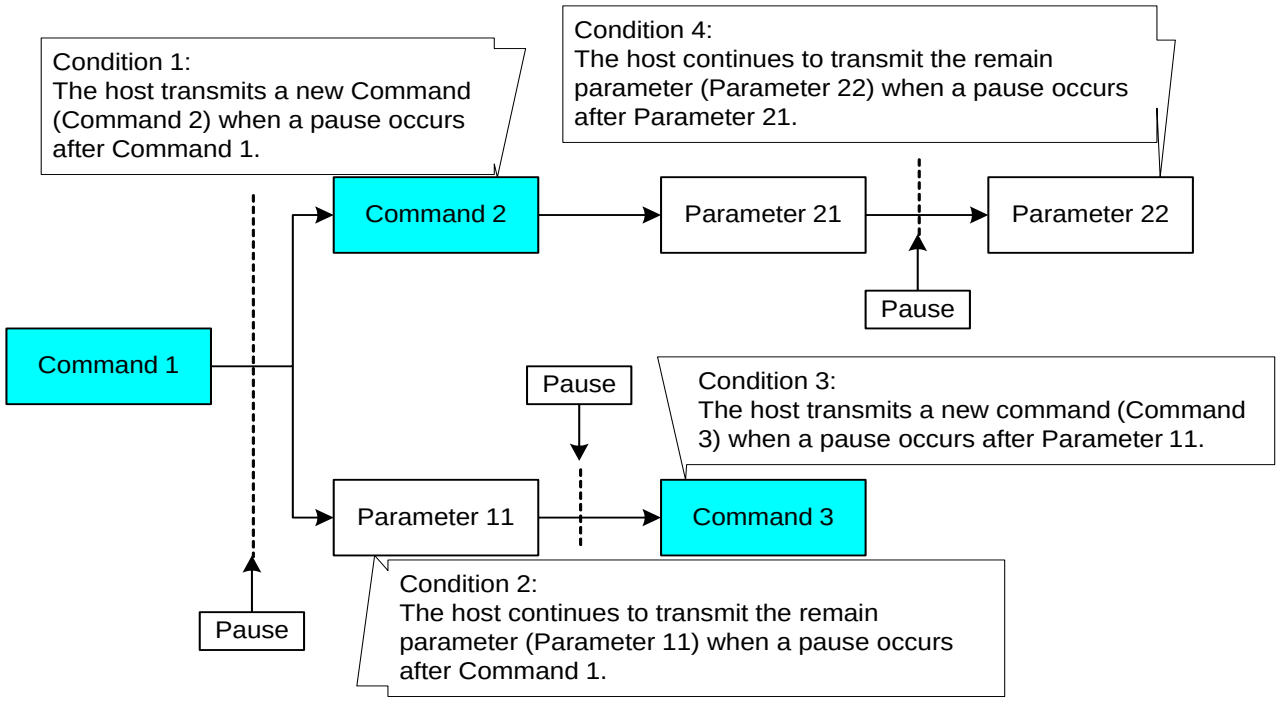
This applies to the following 4 conditions:

1) Command-Pause-Command

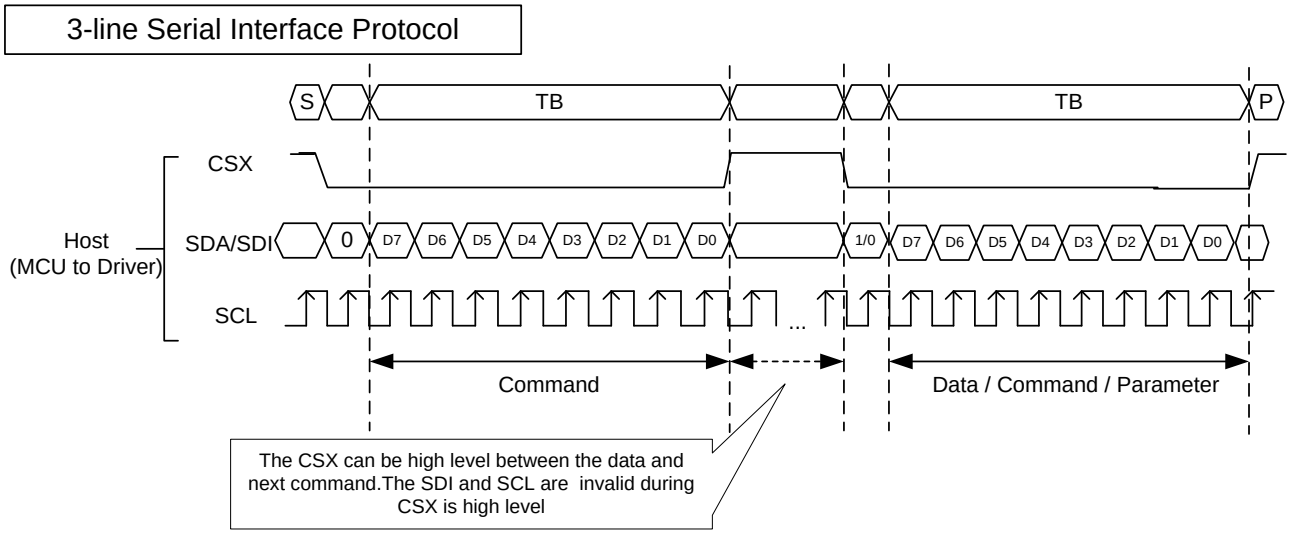
2) Command-Pause-Parameter

3) Parameter-Pause-Command

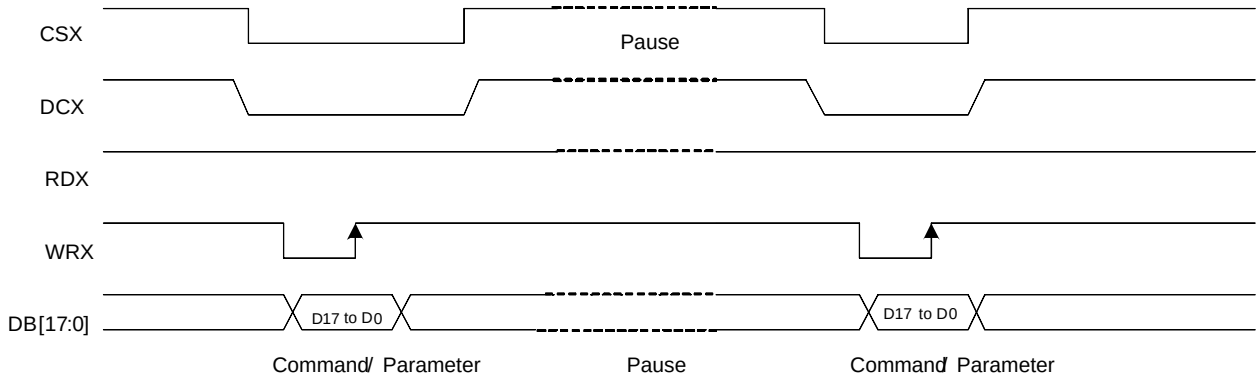
4) Parameter-Pause-Parameter



7.1.13. Serial Interface Pause (3_line)



7.1.14. Parallel Interface Pause

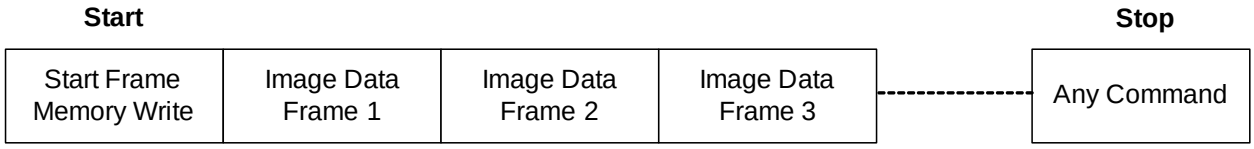


7.1.15. Data Transfer Mode

ILI9340X can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

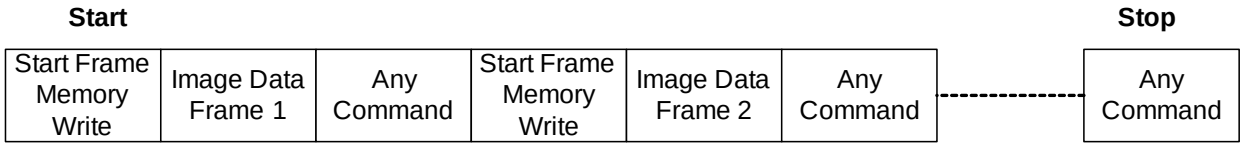
7.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

7.2. RGB Interface

7.2.1. RGB Interface Selection

ILI9340X has several kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DB [17:0] pins. Using RGB interface must selection serial interface.

ILI9340X supports two kinds pixel formats that can be selected by DPI [2:0] bits of “Pixel Format Set (3Ah)” and RIM bit of command F6h. The selection of a given interfaces is done by setting RCM [1:0] and DPI [2:0] as show in the following table.

RCM[1:0]		RIM	DPI[2:0]			RGB Interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	**DE Mode** Valid data is determined by the ENABLE signal	VSYNC, HSYNC, ENABLE, DOTCLK,DB[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, ENABLE, DOTCLK, DB[17:13] & DB[11:1]
1	0	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, ENABLE, DOTCLK, DB[5:0]
1	0	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, ENABLE, DOTCLK, DB[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	**SYNC Mode** In SYNC mode, ENABLE signal is ignored; blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, DB[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, DB[17:13] & DB[11:1]
1	1	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, DOTCLK, DB[5:0]
1	1	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, DB[5:0]

18-bit data bus interface (DB[17:0] is used) , DPI[2:0] = 110, and RIM=0

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (DB[17:13] & DB[11:1] is used) , DPI[2:0] = 101, and RIM=0

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	

The LSB data of red/blue color depends on the EPF[1:0] setting.

6-bit data bus interface (DB[5:0] is used) , DPI[2:0] = 110, and RIM=1

	DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

6-bit data bus interface (DB[5:0] is used) , DPI[2:0] = 101, and RIM=1

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	

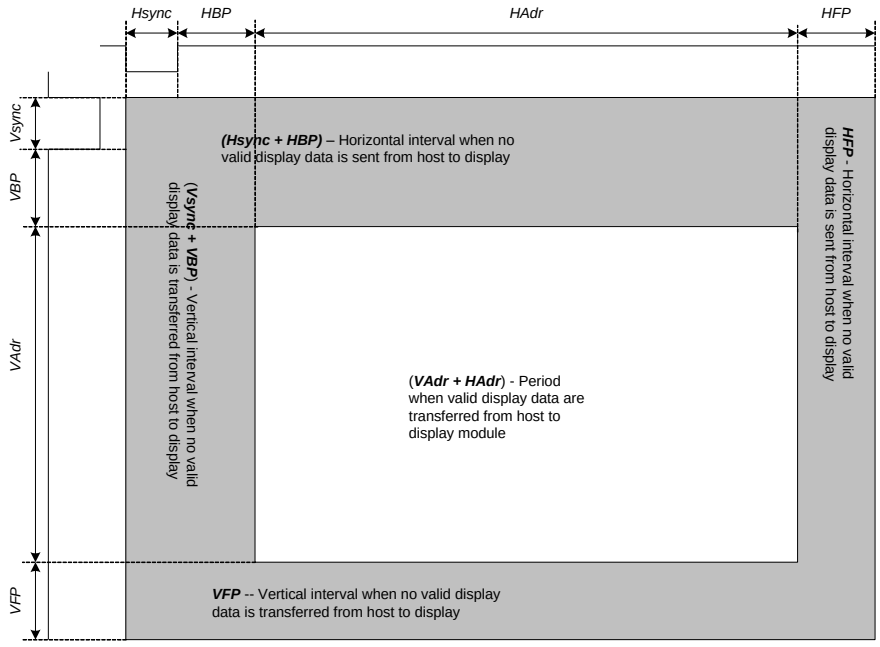
The LSB data of red/blue color depends on the EPF[1:0] setting.

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, ENABLE and DB[17:0] states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as continues internal

clock for other functions of the display module. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable (command B0h default value) and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable(command B0h default value) and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, ENABLE pin is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. DB[17:0] are used to tell what is the information of the image that is transferred on the display (When ENABLE = '0' (low) and there is a rising edge of DOTCLK). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via DB[17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first (command B0h ByPass_MODE default) then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Back Porch(ByPass mode)*	HBP(BP)		58	64	200	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Note1:The HBP setting in RGB 6/6/6 byPass mode is 3 times as much as without byPass mode. It can set HBP[7:0] in command B5h

Typical values are setting example when used with panel resolution 240 x 320 (QVGA), clock frequency 6.35MHz and frame frequency about 70Hz.

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals DOTCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

Also make sure that

(Number of DOTCLK perline) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV

Setting Example for Display Control Clock in RGB Interface Operation

Internal clock PCLKD which is generated by dividing DOTCLK..

PCDIV [5:0]: Number of DOTCLK during internal clock PCLKD's high / low period. In units of 1 clock.

PCDIV specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 615KHz is the smallest. Set PCDIV follow the restriction

(Number of PCLK in 1H) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV.

Setting Example: To set frame frequency to 70Hz:

Internal Clock

Internal Oscillation Clock: 615KHz

DIV[1:0] = 2'h0 (x 1/1)

RTN[4:0] = 5'h1b (27 clocks)

FP = 7'h2 (2 lines), BP = 7'h2 (2 lines), NL = 6'h27 (320 lines)

Frame Rate → 70.30Hz

DOTCLK

HSYNC = 10 CLK

HBP = 20 CLK

HFP=10 CLK

70Hz x (2 + 320 + 2) lines x (10 + 20 + 240 + 10) clocks = 6.35MHz

DOTCLK frequency = 6.35MHz

6.35 MHz / 615KHz = 10.32 Set PCDIV so that PCLK is divided by 10.

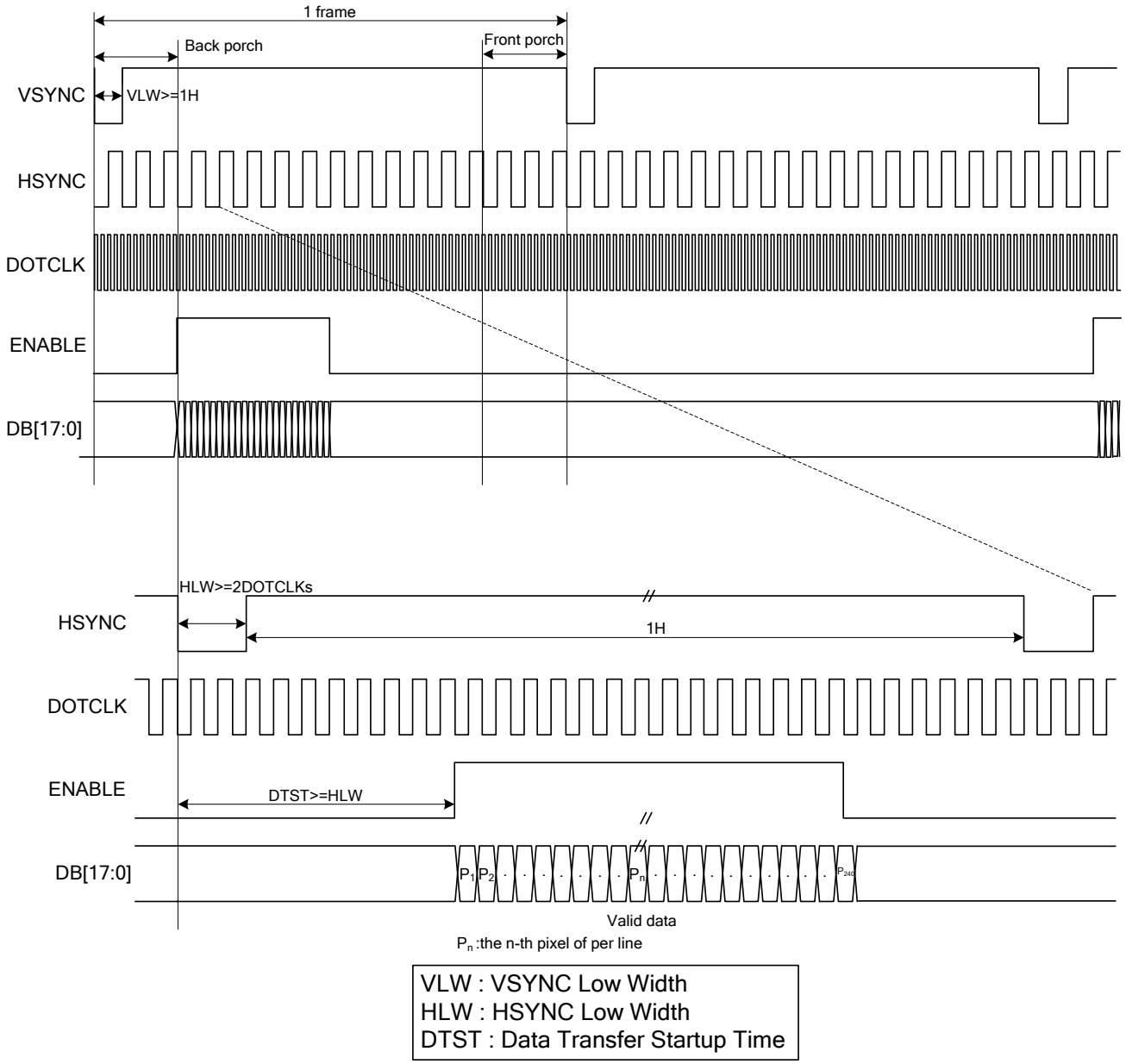
external fosc = 6.35 MHz / 10 = 635KHz

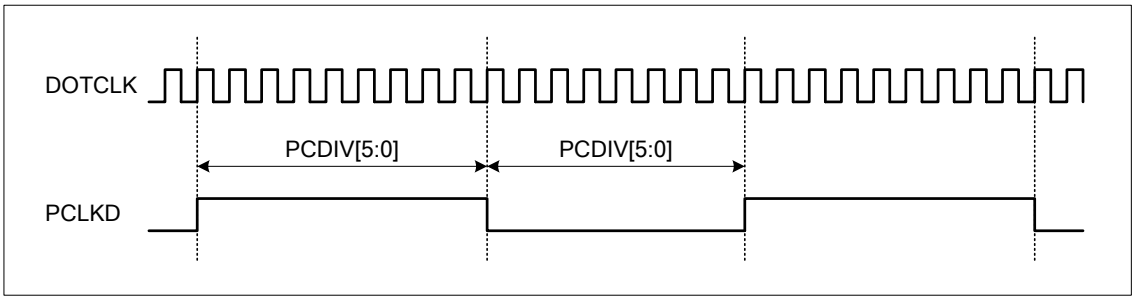
PCDIV = [6.35MHz / 635KHz) / 2] - 1 = 4

PCDIV[5:0] = 6'h04 (10 DOTCLK)

7.2.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.

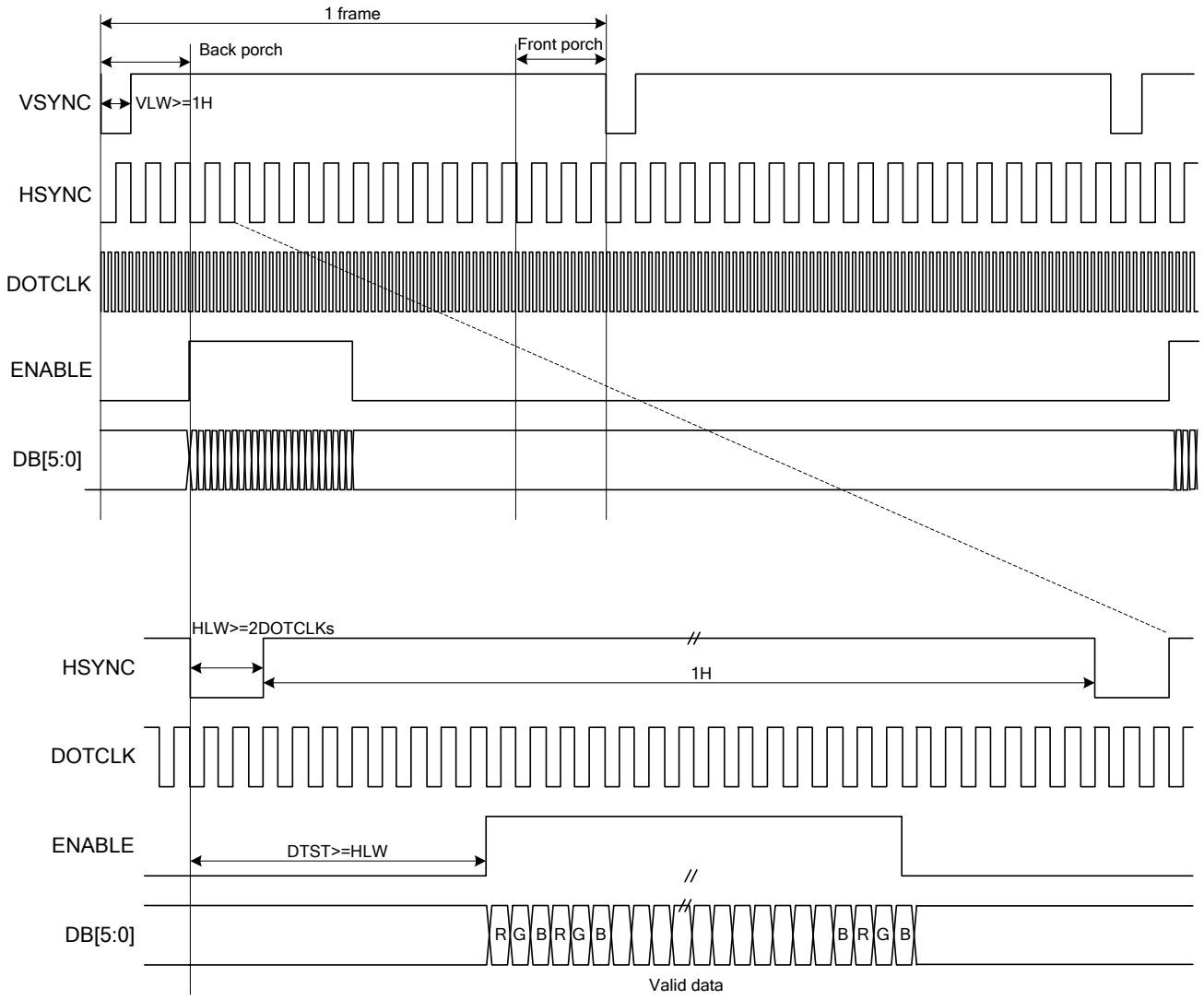




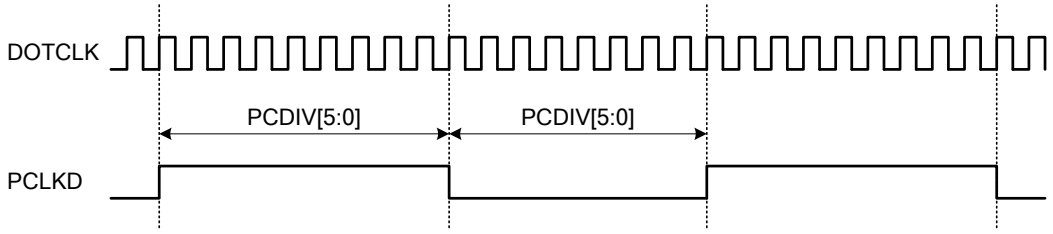
Note 1: The ENABLE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:



VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time



Note 1: The ENABLE signal is not needed when RGB interface SYNC mode is selected.

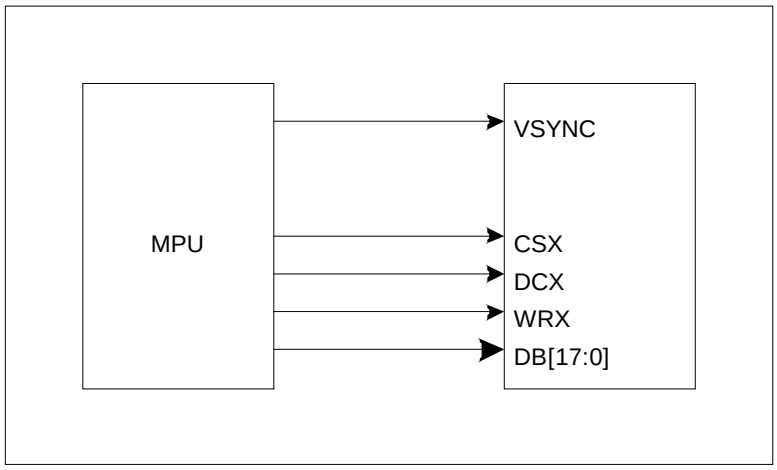
Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

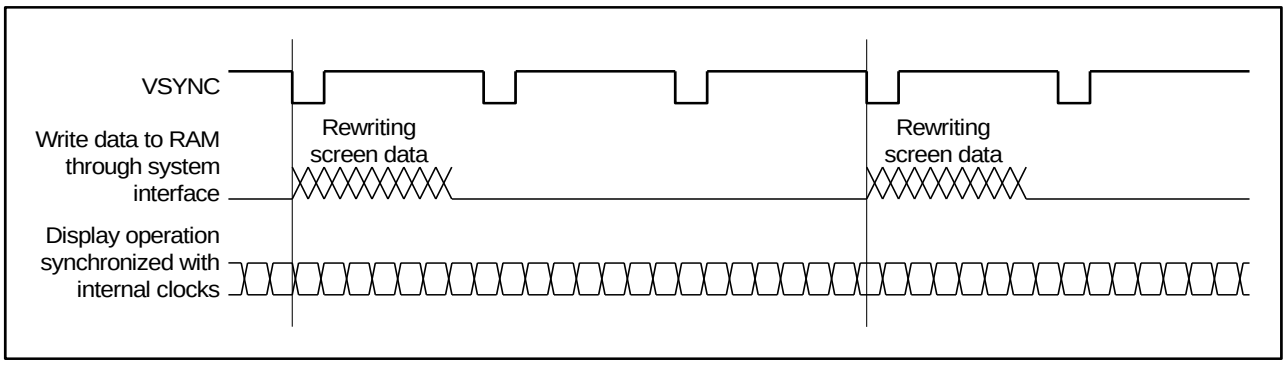
Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and ENABLE to 3 multiples of DOTCLK.

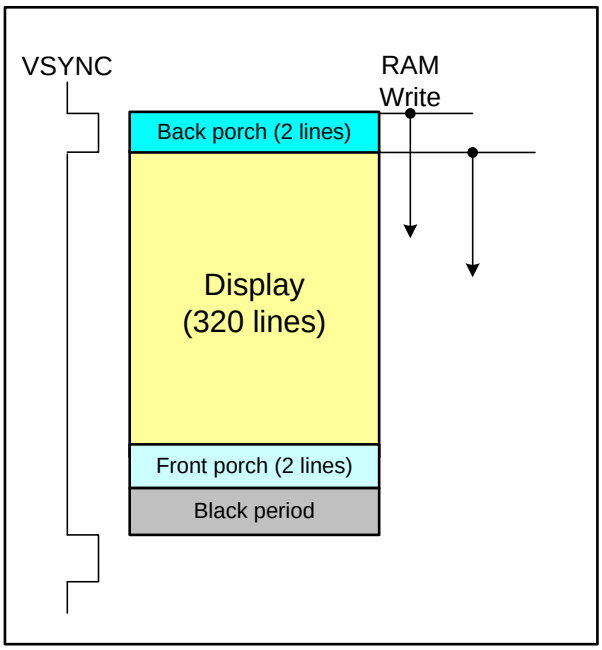
7.3. VSYNC Interface

ILI9340X supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080-Ⅰ/8080-Ⅱ system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.



In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.





The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (VFP) + BackPorch (VBP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\textit{Minimum RAM write speed [Hz]} > \frac{240 \times DisplayLines(NL)}{[BackPorch(VBP) + DisplayLines(NL) - margins] \times Clocks\ per\ line \times (1/fosc)}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 240 RGB × 320 lines

Lines: 320 lines (NL = 100111)

Back porch: 2 lines (VBP = 0000010)

Front porch: 2 lines (VFP = 0000010)

Frame frequency: 70 Hz

Frequency fluctuation: 10%

Internal oscillator clock (fosc.) [Hz] = 70 x [320+ 2 + 2] x 27 clocks x (1.1/0.9) ≒ 748KHz

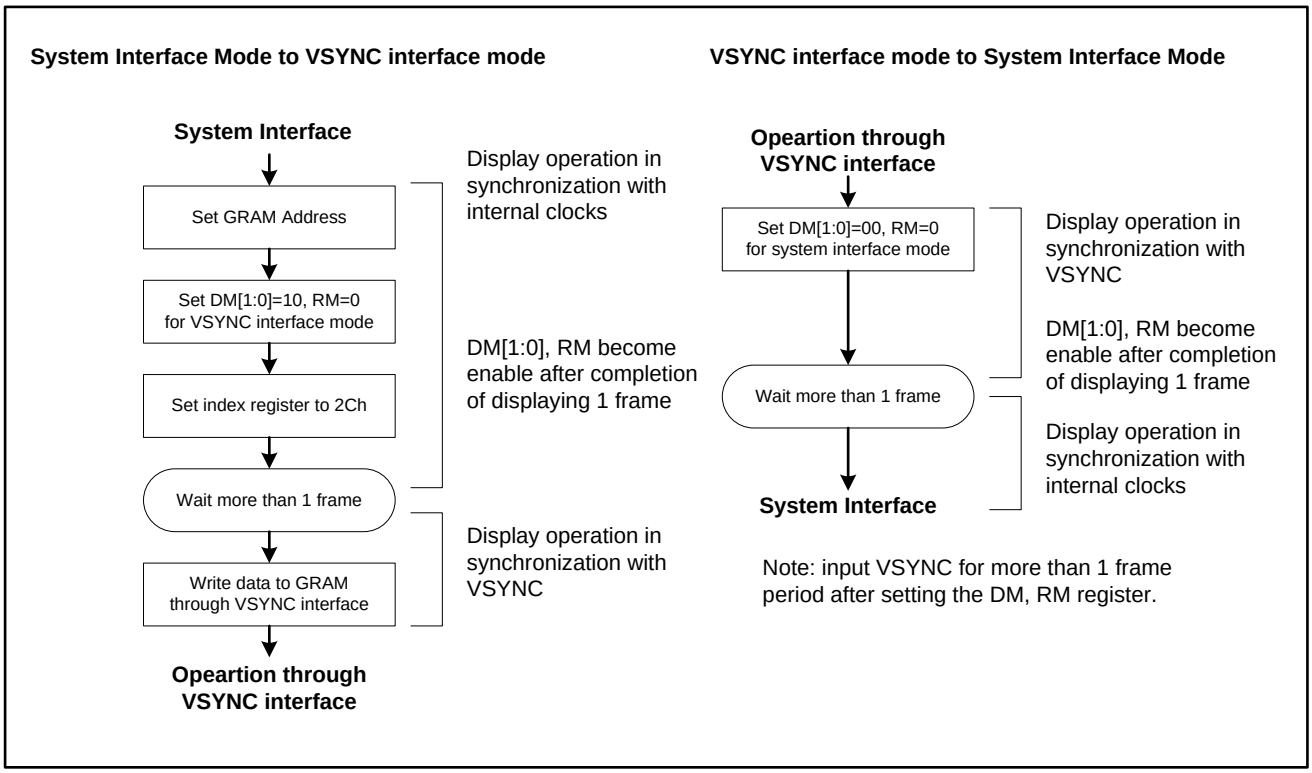
When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz] > 240 x 320 x 748K / [(2 + 320 – 2)lines x 27clocks] ≒ 6.65 MHz

The above theoretical value is calculated based on the premise that the ILI9340X starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 6.65MHz or more will guarantee the completion of GRAM write operation before the ILI9340X starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

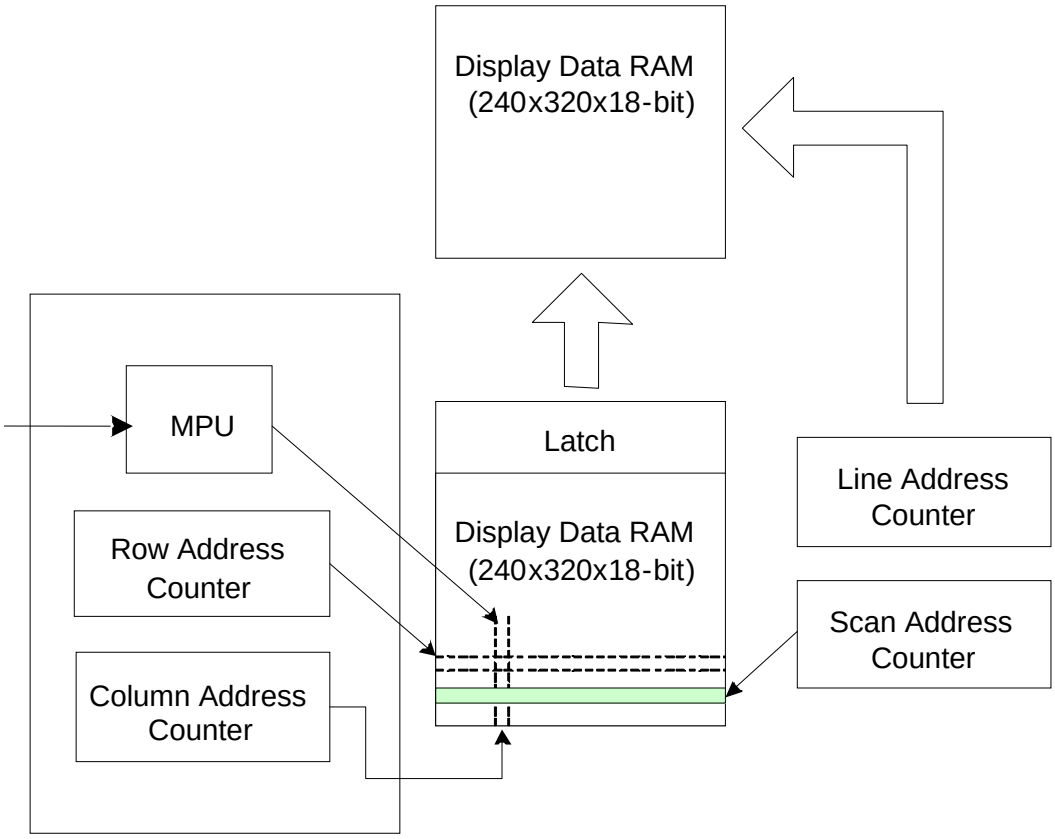
Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.



7.4. Display Data RAM (DDRAM)

ILI9340X has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

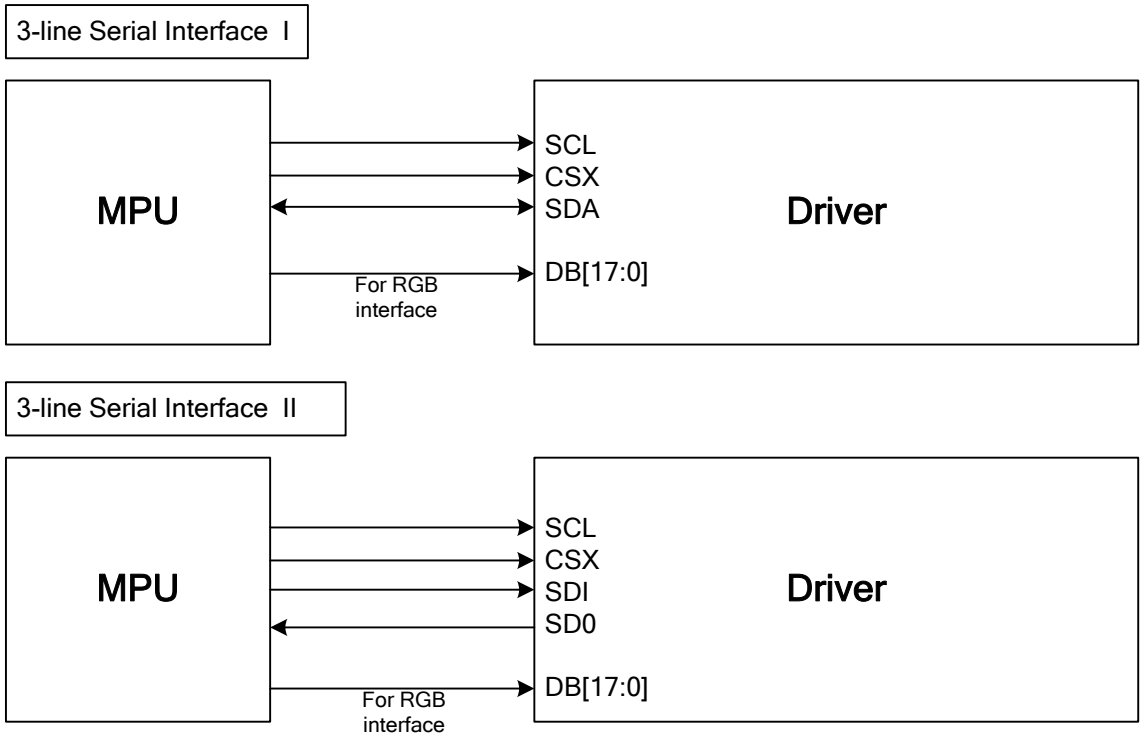


7.5. Display Data Format

ILI9340X supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

7.5.1. 3-line Serial Interface

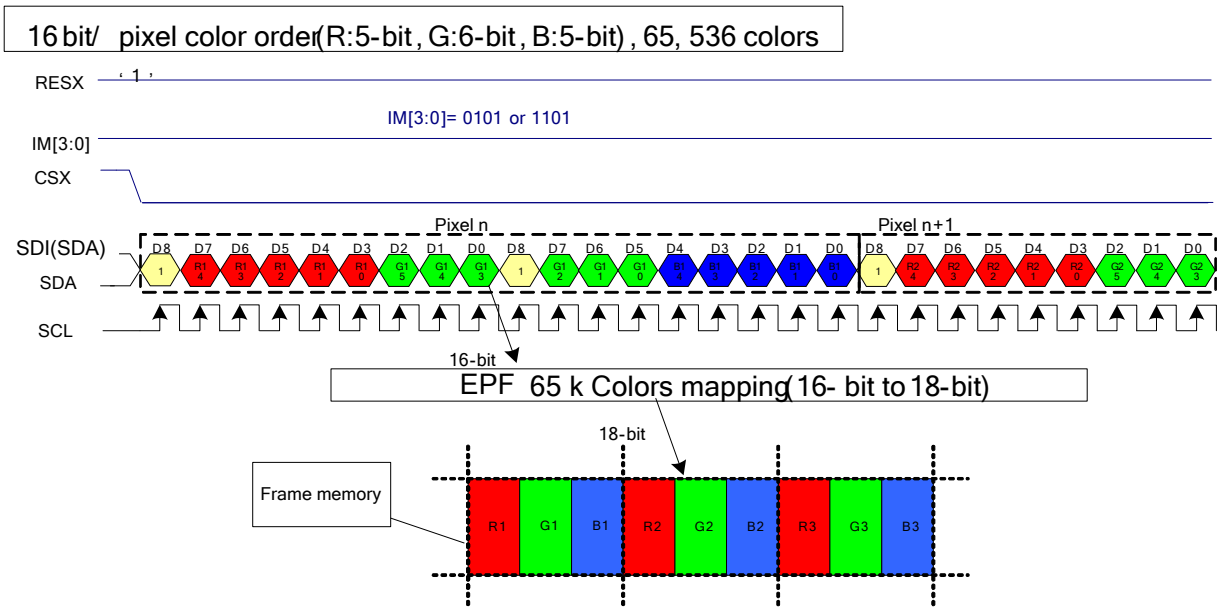
The 3-line/9-bit serial bus interface of ILI9340X can be used by setting external pin as IM [3:0] to “0101” for serial interface I or IM [3:0] to “1101” for serial interface II. The shown figure is the example of 3-line SPI interface.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

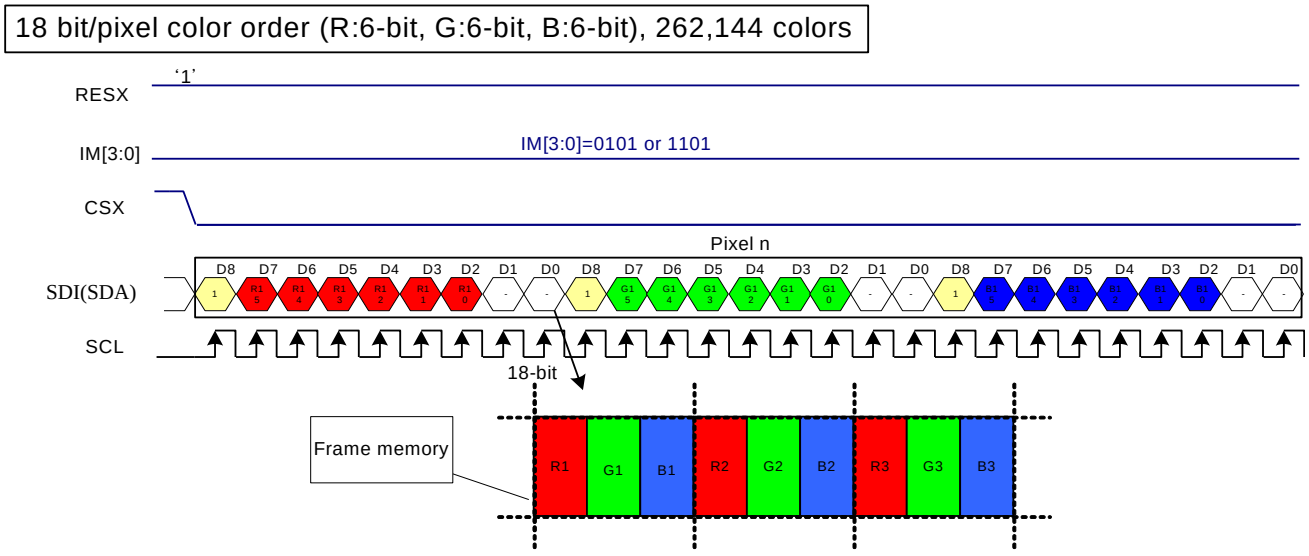


Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".



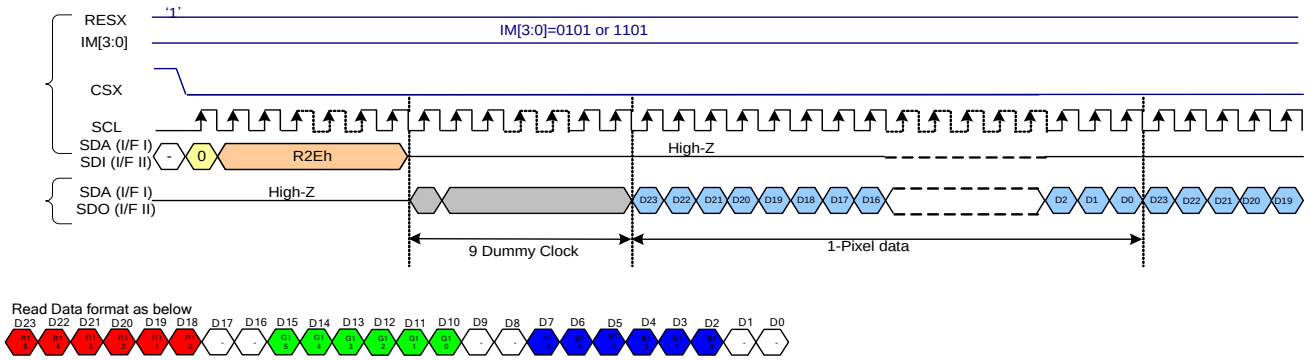
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

Read data through 3-line SPI mode

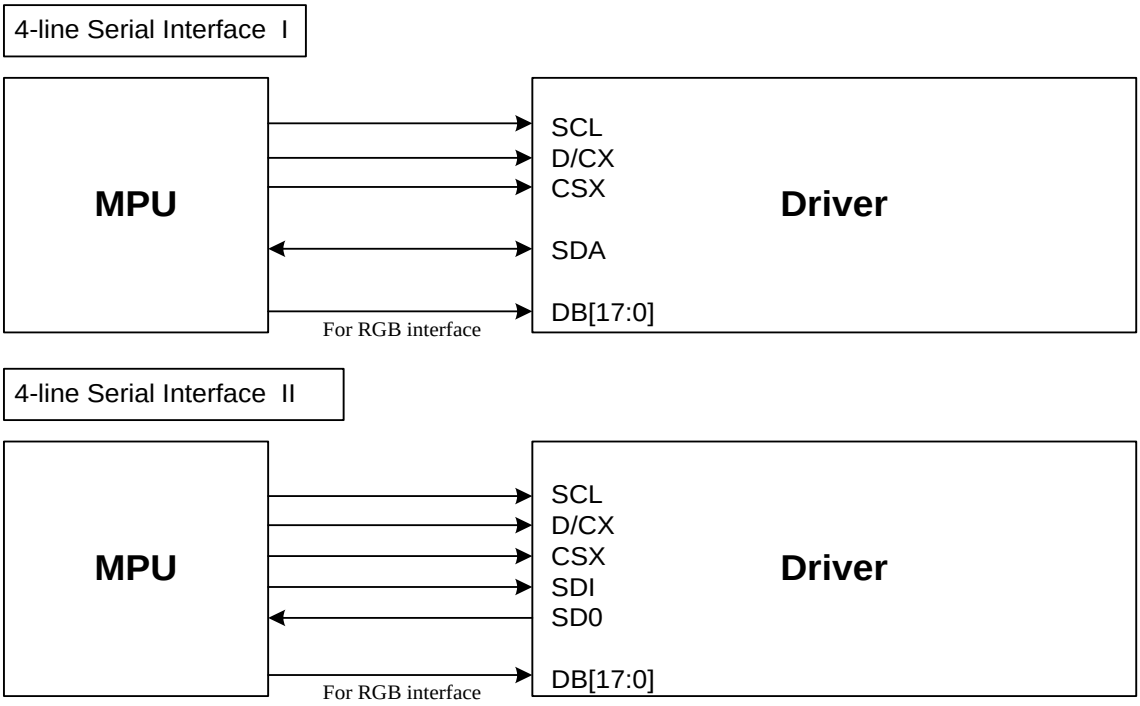


Read Data format as below

Note 1: '-'= Don't care –Can be set "0" or "1".

7.5.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of ILI9340X can be used by setting external pin as IM [3:0] to “0110” for serial interface I or IM [3:0] to “1110” for serial interface II. The shown figure is the example of 4-line SPI interface.

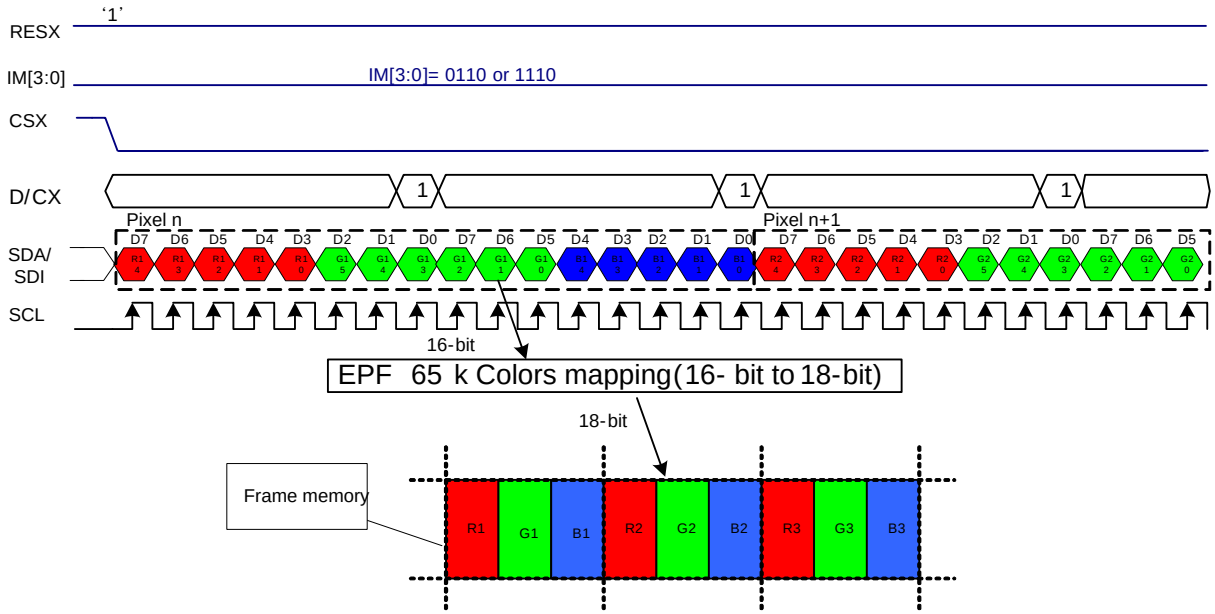


In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

16 bit/ pixel color order(R:5-bit , G:6-bit , B:5-bit) , 65, 536 colors



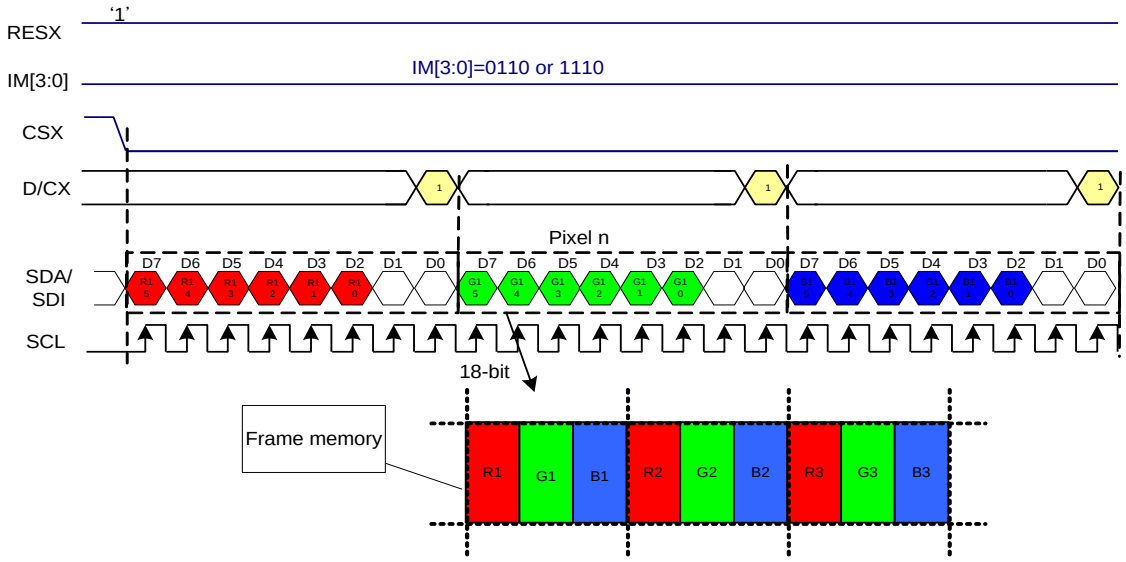
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



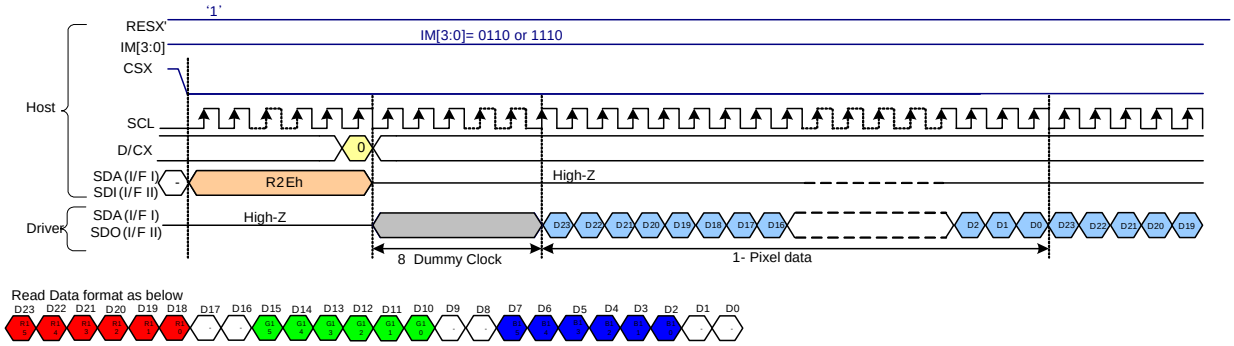
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Read data through 4- line SPI mode



Read Data format as below

Note 1: '-'= Don't care – Can be set "0" or "1".

7.5.3. 2-data-lane serial interface data format

In 2-data-lane serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k color, RGB 5, 6, 5 -bits input.

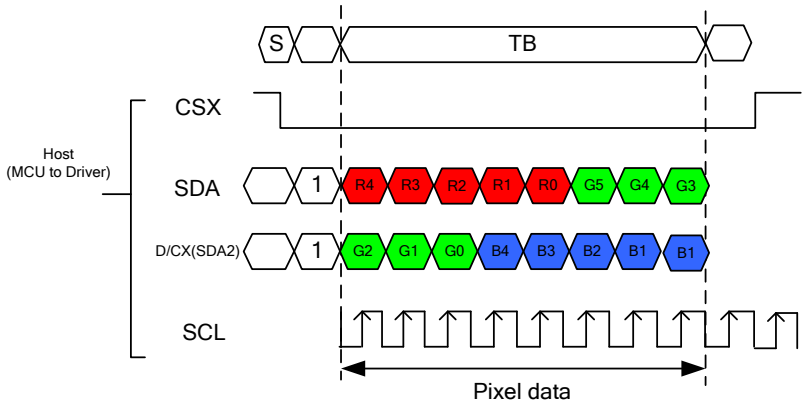
-262k color, RGB 6, 6, 6 -bits input

262k color has two kind of transfer data type.

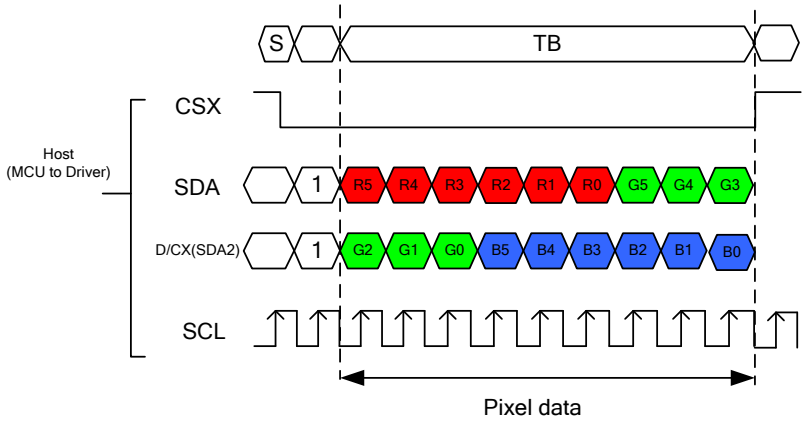
Type0: When the bits [2:1] of C6h register are sent to “01” .One pixel display data is sent by 1 time transfers.

Type1: When the bits [2:1] of C6h register are sent to “11”. Two pixels display data is sent by 3 time transfers.

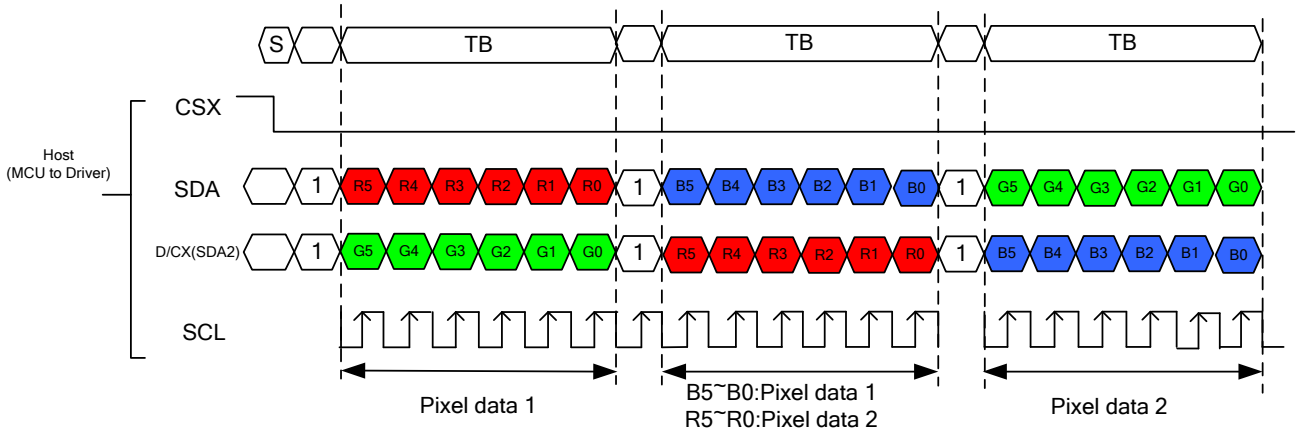
16 bit/pixel color order (R:5-bit, G:6-bit, B:5-bit), 65,536 colors



18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors,Type0 (default)

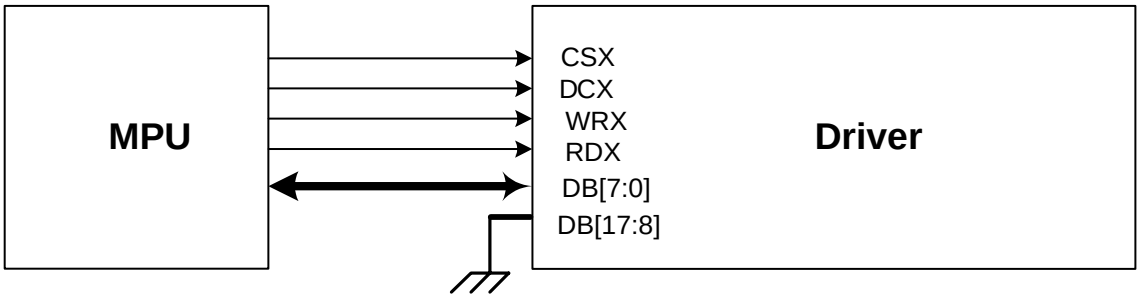


18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors,Type1



7.5.4. 8-bit Parallel MCU Interface

The 8080-Ⅰ system 8-bit parallel bus interface of ILI9340X can be used by setting external pin as IM [3:0] to "0000".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 times transfer when DBI [2:0] bits of 3Ah register are set to "101".

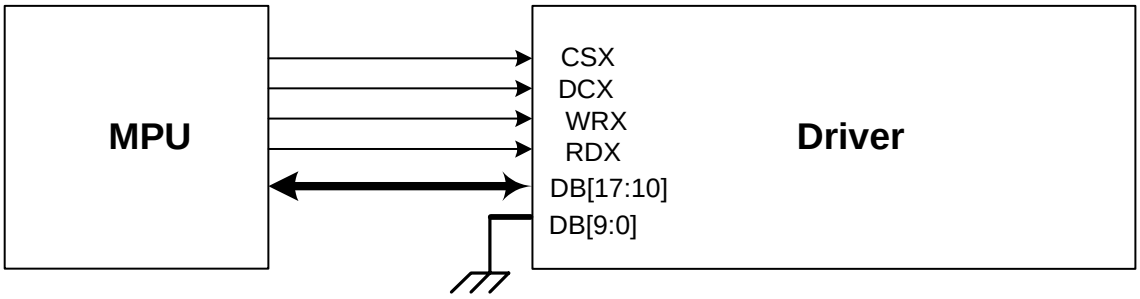
Count	0	1	2	3	4	…	477	478	479	480
DCX	0	1	1	1	1	…	1	1	1	1
DB7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
DB6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
DB5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
DB4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
DB3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
DB2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
DB1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
DB0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 times transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	…	718	719	720
DCX	0	1	1	1	…	1	1	1
DB7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
DB6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
DB5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
DB4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
DB3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
DB2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
DB1	C1				…			
DB0	C0				…			

The 8080-Ⅱ system 8-bit parallel bus interface of ILI9340X can be used by settings as IM [3:0] =”1001”. The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 times transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	4	…	477	478	479	480
DBCX	0	1	1	1	1	…	1	1	1	1
DB17	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
DB16	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
DB15	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
DB14	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
DB13	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
DB12	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
DB11	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
DB10	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

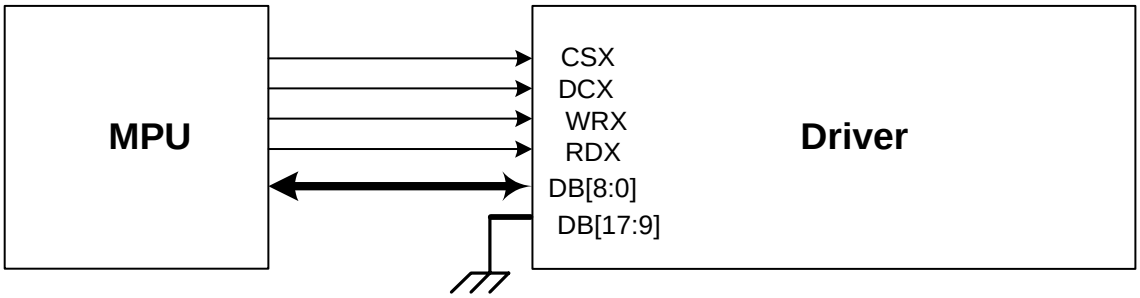
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 times transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	718	719	720
DCX	0	1	1	1	…	1	1	1
DB17	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
DB16	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
DB15	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
DB14	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
DB13	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
DB12	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
DB11	C1				…			
DB10	C0				…			

7.5.5. 9-bit Parallel MCU Interface

The 8080-Ⅰ system 9-bit parallel bus interface of ILI9340X can be selected by setting hardware pin IM [3:0] to "0010". The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 times transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	…	477	478	479	480
DCX	0	1	1	1	1	…	1	1	1	1
DB8										
DB7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
DB6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
DB5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
DB4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
DB3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
DB2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
DB1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
DB0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 times transfer, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

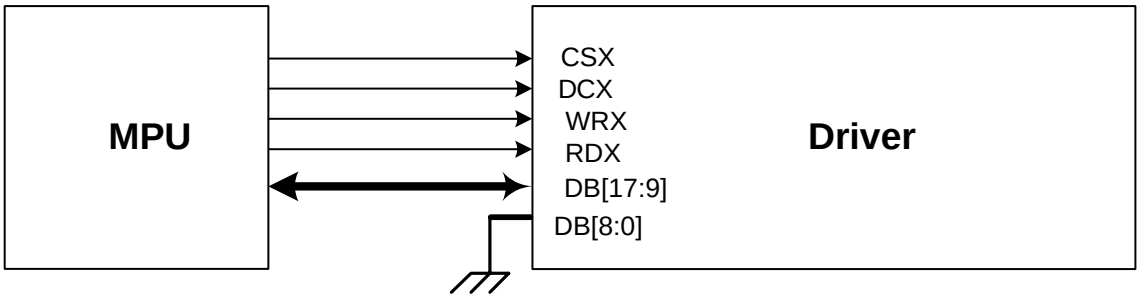
Count	0	1	2	3	4	…	478	478	479	480
DCX	0	1	1	1	1	…	1	1	1	1
DB8		0R5	0G2	1R5	1G2		238R5	238G2	239R5	239G2
DB7	C7	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
DB6	C6	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
DB5	C5	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
DB4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
DB3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
DB2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
DB1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
DB0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

One pixel (3 sub-pixels) display data is sent by 3 times transfer

MDT[1:0]="01"

Count	0	1	2	3	…	718	719	720
DCX	0	1	1	1	…	1	1	1
DB8								
DB7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
DB6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
DB5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
DB4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
DB3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
DB2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
DB1	C1				…			
DB0	C0				…			

The 8080-Ⅱ system 9-bit parallel bus interface of ILI9340X can be selected by setting hardware pin IM [3:0] to "1011". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 times transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	…	477	478	479	480
DCX	0	1	1	1	1	…	1	1	1	1
DB17	C7									
DB16	C6	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
DB15	C5	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
DB14	C4	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
DB13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
DB12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
DB11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
DB10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
DB9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 times transfer, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	4	…	478	478	479	480
DCX	0	1	1	1	1	…	1	1	1	1
DB17	C7	0R5	0G2	1R5	1G2		238R5	238G2	239R5	239G2
DB16	C6	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
DB15	C5	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
DB14	C4	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
DB13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
DB12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
DB11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
DB10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
DB9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

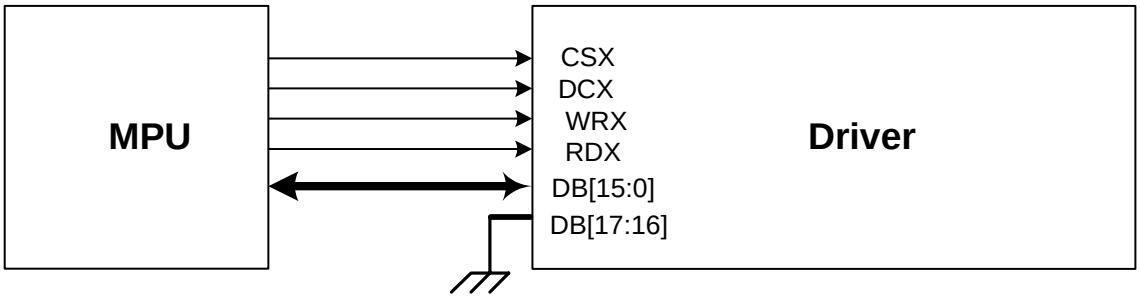
One pixel (3 sub-pixels) display data is sent by 3 times transfer

MDT[1:0]="01"

Count	0	1	2	3	…	718	719	720
DCX	0	1	1	1	…	1	1	1
DB17	C7							
DB16	C6	0R5	0G5	0B5	…	239R5	239G5	239B5
DB15	C5	0R4	0G4	0B4	…	239R4	239G4	239B4
DB14	C4	0R3	0G3	0B3	…	239R3	239G3	239B3
DB13	C3	0R2	0G2	0B2	…	239R2	239G2	239B2
DB12	C2	0R1	0G1	0B1	…	239R1	239G1	239B1
DB11	C1	0R0	0G0	0B0	…	239R0	239G0	239B0
DB10	C0				…			
DB9					…			

7.5.6. 16-bit Parallel MCU Interface

The 8080-Ⅰ system 16-bit parallel bus interface of ILI9340X can be selected by setting hardware pin IM[3:0] to "0001".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by once transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	238	239	240
DCX	0	1	1	1	…	1	1	1
DB15		0R4	1R4	2R4	…	237R4	238R4	239R4
DB14		0R3	1R3	2R3	…	237R3	238R3	239R3
DB13		0R2	1R2	2R2	…	237R2	238R2	239R2
DB12		0R1	1R1	2R1	…	237R1	238R1	239R1
DB11		0R0	1R0	2R0	…	237R0	238R0	239R0
DB10		0G5	1G5	2G5	…	237G5	238G5	239G5
DB9		0G4	1G4	2G4	…	237G4	238G4	239G4
DB8		0G3	1G3	2G3	…	237G3	238G3	239G3
DB7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
DB6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
DB5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
DB4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
DB3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
DB2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
DB1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
DB0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

Two pixels (6 sub-pixel) display data are sent by 3 times transfer when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	…	358	359	360
DCX	0	1	1	1	…	1	1	1
DB15		0R5	0B5	1G5	…	238R5	238B5	239G5
DB14		0R4	0B4	1G4	…	238R4	238B4	239G4
DB13		0R3	0B3	1G3	…	238R3	238B3	239G3
DB12		0R2	0B2	1G2	…	238R2	238B2	239G2
DB11		0R1	0B1	1G1	…	238R1	238B1	239G1
DB10		0R0	0B0	1G0	…	238R0	238B0	239G0
DB9					…			
DB8					…			
DB7	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
DB6	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
DB5	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
DB4	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
DB3	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
DB2	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
DB1	C1				…			
DB0	C0				…			

One pixel (3 sub-pixels) display data is sent by 2 times transfer

MDT[1:0]="01"

Count	0	1	2	3		…	357	358	479	480
DCX	0	1	1	1		…		1	1	1
DB15		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
DB14		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
DB13		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
DB12		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
DB11		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
DB10		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
DB9						…				
DB8						…				
DB7	C7	0G5		1G5		…	238G5		239G5	
DB6	C6	0G4		1G4		…	238G4		239G4	
DB5	C5	0G3		1G3		…	238G3		239G3	
DB4	C4	0G2		1G2		…	238G2		239G2	
DB3	C3	0G1		1G1		…	238G1		239G1	
DB2	C2	0G0		1G0		…	238G0		239G0	
DB1	C1					…				
DB0	C0					…				

MDT[1:0]=”10”

One pixel (3 sub-pixels) display data is sent by 2 times transfer

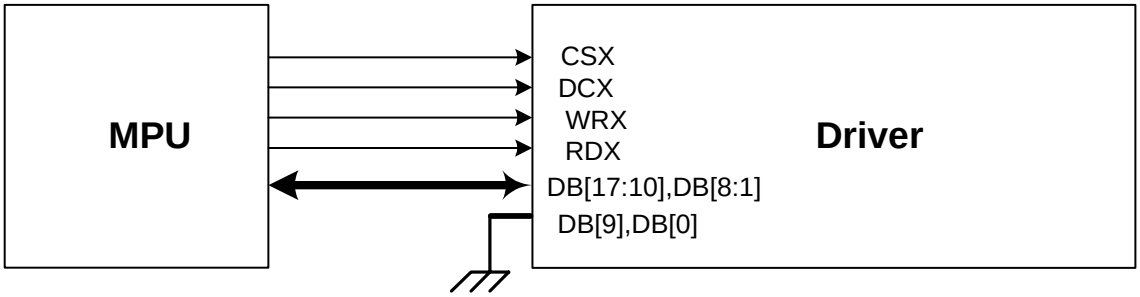
Count	0	1	2	3		…	357	358	479	480
DCX	0	1	1	1		…		1	1	1
DB15		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
DB14		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
DB13		0R3		1R3		…	238R3		239R3	
DB12		0R2		1R2		…	238R2		239R2	
DB11		0R1		1R1		…	238R1		239R1	
DB10		0R0		1R0		…	238R0		239R0	
DB9		0G5		1G5		…	238G5		239G5	
DB8		0G4		1G4		…	238G4		239G4	
DB7	C7	0G3		1G3		…	238G3		239G3	
DB6	C6	0G2		1G2		…	238G2		239G2	
DB5	C5	0G1		1G1		…	238G1		239G1	
DB4	C4	0G0		1G0		…	238G0		239G0	
DB3	C3	0B5		1B5		…	238B5		239B5	
DB2	C2	0B4		1B4		…	238B4		239B4	
DB1	C1	0B3		1B3		…	238B3		239B3	
DB0	C0	0B2		1B2		…	238B2		239B2	

MDT[1:0]=”11”

One pixel (3 sub-pixels) display data is sent by 2 times transfer

Count	0	1	2	3		…	357	358	479	480
DCX	0	1	1	1		…		1	1	1
DB15			0R3		1R3	…		238R3		239R3
DB14			0R2		1R2	…		238R2		239R2
DB13			0R1		1R1	…		238R1		239R1
DB12			0R0		1R0	…		238R0		239R0
DB11			0G5		1G5	…		238G5		239G5
DB10			0G4		1G4	…		238G4		239G4
DB9			0G3		1G3	…		238G3		239G3
DB8			0G2		1G2	…		238G2		239G2
DB7	C7		0G1		1G1	…		238G1		239G1
DB6	C6		0G0		1G0	…		238G0		239G0
DB5	C5		0B5		1B5	…		238B5		239B5
DB4	C4		0B4		1B4	…		238B4		239B4
DB3	C3		0B3		1B3	…		238B3		239B3
DB2	C2		0B2		1B2	…		238B2		239B2
DB1	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
DB0	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

The 8080-Ⅱ system 16-bit parallel bus interface of ILI9340X can be selected by settings IM [3:0] =”1000”. The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by once transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	…	238	239	240
DCX	0	1	1	1	…	1	1	1
DB17		0R4	1R4	2R4	…	237R4	238R4	239R4
DB16		0R3	1R3	2R3	…	237R3	238R3	239R3
DB15		0R2	1R2	2R2	…	237R2	238R2	239R2
DB14		0R1	1R1	2R1	…	237R1	238R1	239R1
DB13		0R0	1R0	2R0	…	237R0	238R0	239R0
DB12		0G5	1G5	2G5	…	237G5	238G5	239G5
DB11		0G4	1G4	2G4	…	237G4	238G4	239G4
DB10		0G3	1G3	2G3	…	237G3	238G3	239G3
DB8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
DB7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
DB6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
DB5	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
DB4	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
DB3	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
DB2	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
DB1	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

Two pixels (6 sub-pixel) display data are sent by 3 times transfers when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	…	358	359	360
DCX	0	1	1	1	…	1	1	1
DB17		0R5	0B5	1G5	…	238R5	238B5	239G5
DB16		0R4	0B4	1G4	…	238R4	238B4	239G4
DB15		0R3	0B3	1G3	…	238R3	238B3	239G3
DB14		0R2	0B2	1G2	…	238R2	238B2	239G2
DB13		0R1	0B1	1G1	…	238R1	238B1	239G1
DB12		0R0	0B0	1G0	…	238R0	238B0	239G0
DB11					…			
DB10					…			
DB8	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
DB7	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
DB6	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
DB5	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
DB4	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
DB3	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
DB2	C1				…			
DB1	C0				…			

One pixel (3 sub-pixels) display data is sent by 2 times transfer

MDT[1:0]="01"

Count	0	1	2	3		…	357	358	479	480
DCX	0	1	1	1		…		1	1	1
DB17		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
DB16		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
DB15		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
DB14		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
DB13		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
DB12		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
DB11						…				
DB10						…				
DB8	C7	0G5		1G5		…	238G5		239G5	
DB7	C6	0G4		1G4		…	238G4		239G4	
DB6	C5	0G3		1G3		…	238G3		239G3	
DB5	C4	0G2		1G2		…	238G2		239G2	
DB4	C3	0G1		1G1		…	238G1		239G1	
DB3	C2	0G0		1G0		…	238G0		239G0	
DB2	C1					…				
DB1	C0					…				

One pixel (3 sub-pixels) display data is sent by 2 times transfer

MDT[1:0]="10"

Count	0	1	2	3		…	357	358	479	480
DCX	0	1	1	1		…		1	1	1
DB17		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
DB16		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
DB15		0R3		1R3		…	238R3		239R3	
DB14		0R2		1R2		…	238R2		239R2	
DB13		0R1		1R1		…	238R1		239R1	
DB12		0R0		1R0		…	238R0		239R0	
DB11		0G5		1G5		…	238G5		239G5	
DB10		0G4		1G4		…	238G4		239G4	
DB8	C7	0G3		1G3		…	238G3		239G3	
DB7	C6	0G2		1G2		…	238G2		239G2	
DB6	C5	0G1		1G1		…	238G1		239G1	
DB5	C4	0G0		1G0		…	238G0		239G0	
DB4	C3	0B5		1B5		…	238B5		239B5	
DB3	C2	0B4		1B4		…	238B4		239B4	
DB2	C1	0B3		1B3		…	238B3		239B3	
DB1	C0	0B2		1B2		…	238B2		239B2	

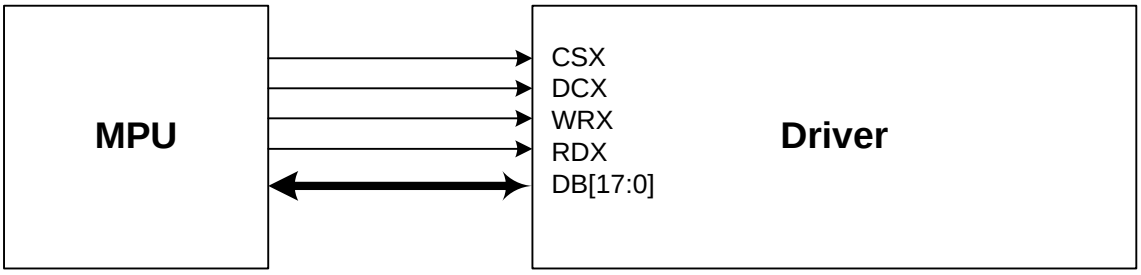
One pixel (3 sub-pixels) display data is sent by 2 times transfer

MDT[1:0]="11"

Count	0	1	2	3		…	357	358	479	480
DCX	0	1	1	1		…		1	1	1
DB17			0R3		1R3	…		238R3		239R3
DB16			0R2		1R2	…		238R2		239R2
DB15			0R1		1R1	…		238R1		239R1
DB14			0R0		1R0	…		238R0		239R0
DB13			0G5		1G5	…		238G5		239G5
DB12			0G4		1G4	…		238G4		239G4
DB11			0G3		1G3	…		238G3		239G3
DB10			0G2		1G2	…		238G2		239G2
DB8	C7		0G1		1G1	…		238G1		239G1
DB7	C6		0G0		1G0	…		238G0		239G0
DB6	C5		0B5		1B5	…		238B5		239B5
DB5	C4		0B4		1B4	…		238B4		239B4
DB4	C3		0B3		1B3	…		238B3		239B3
DB3	C2		0B2		1B2	…		238B2		239B2
DB2	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
DB1	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

7.5.7. 18-bit Parallel MCU Interface

The 8080-Ⅰ system 18-bit parallel bus interface of ILI9340X can be selected by setting hardware pin IM[3:0] to "0011".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by once transfer when DBI [2:0] bits of 3Ah register are set to "101".

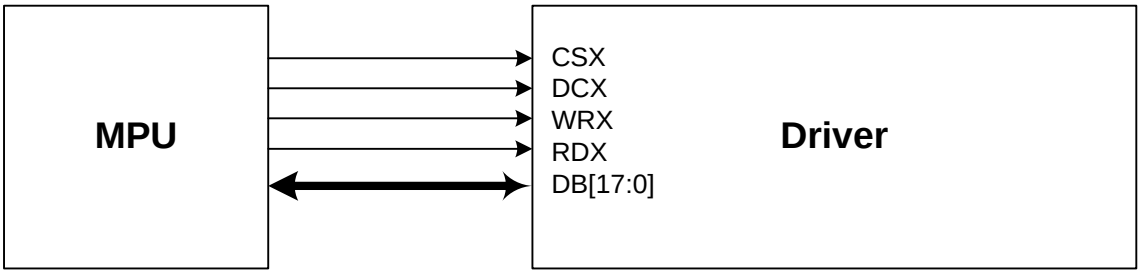
Count	0	1	2	3	…	238	239	240
DCX	0	1	1	1	…	1	1	1
DB17								
DB16								
DB15		0R4	1R4	2R4	…	237R4	238R4	239R4
DB14		0R3	1R3	2R3	…	237R3	238R3	239R3
DB13		0R2	1R2	2R2	…	237R2	238R2	239R2
DB12		0R1	1R1	2R1	…	237R1	238R1	239R1
DB11		0R0	1R0	2R0	…	237R0	238R0	239R0
DB10		0G5	1G5	2G5	…	237G5	238G5	239G5
DB9		0G4	1G4	2G4	…	237G4	238G4	239G4
DB8		0G3	1G3	2G3	…	237G3	238G3	239G3
DB7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
DB6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
DB5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
DB4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
DB3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
DB2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
DB1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
DB0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by once transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	238	239	240
DCX	0	1	1	1	…	1	1	1
DB17		0R5	1R5	2R5	…	237R5	238R5	239R5
DB16		0R4	1R4	2R4	…	237R4	238R4	239R4
DB15		0R3	1R3	2R3	…	237R3	238R3	239R3
DB14		0R2	1R2	2R2	…	237R2	238R2	239R2
DB13		0R1	1R1	2R1	…	237R1	238R1	239R1
DB12		0R0	1R0	2R0	…	237R0	238R0	239R0
DB11		0G5	1G5	2G5	…	237G5	238G5	239G5
DB10		0G4	1G4	2G4	…	237G4	238G4	239G4
DB9		0G3	1G3	2G3	…	237G3	238G3	239G3
DB8		0G2	1G2	2G2	…	237G2	238G2	239G2
DB7	C7	0G1	1G1	2G1	…	237G1	238G1	239G1
DB6	C6	0G0	1G0	2G0	…	237G0	238G0	239G0
DB5	C5	0B5	1B5	2B5	…	237B5	238B5	239B5
DB4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
DB3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
DB2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
DB1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
DB0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

The 8080-Ⅱ system 18-bit parallel bus interface mode can be selected by settings IM [3:0] ="1010". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by once transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	238	239	240
DCX	0	1	1	1	…	1	1	1
DB17								
DB16								
DB15		0R4	1R4	2R4	…	237R4	238R4	239R4
DB14		0R3	1R3	2R3	…	237R3	238R3	239R3
DB13		0R2	1R2	2R2	…	237R2	238R2	239R2
DB12		0R1	1R1	2R1	…	237R1	238R1	239R1
DB11		0R0	1R0	2R0	…	237R0	238R0	239R0
DB10		0G5	1G5	2G5	…	237G5	238G5	239G5
DB9		0G4	1G4	2G4	…	237G4	238G4	239G4
DB8	C7	0G3	1G3	2G3	…	237G3	238G3	239G3
DB7	C6	0G2	1G2	2G2	…	237G2	238G2	239G2
DB6	C5	0G1	1G1	2G1	…	237G1	238G1	239G1
DB5	C4	0G0	1G0	2G0	…	237G0	238G0	239G0
DB4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
DB3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
DB2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
DB1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
DB0		0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

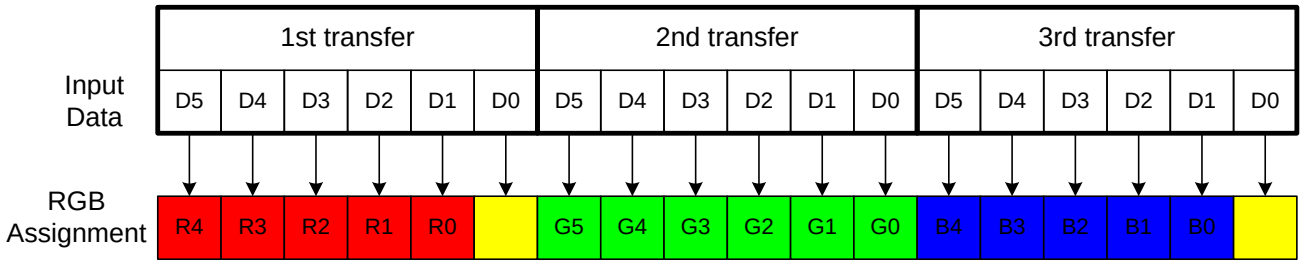
One pixel (3 sub-pixels) display data is sent by once transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	238	239	240
DCX	0	1	1	1	…	1	1	1
DB17		0R5	1R5	2R5	…	237R5	238R5	239R5
DB16		0R4	1R4	2R4	…	237R4	238R4	239R4
DB15		0R3	1R3	2R3	…	237R3	238R3	239R3
DB14		0R2	1R2	2R2	…	237R2	238R2	239R2
DB13		0R1	1R1	2R1	…	237R1	238R1	239R1
DB12		0R0	1R0	2R0	…	237R0	238R0	239R0
DB11		0G5	1G5	2G5	…	237G5	238G5	239G5
DB10		0G4	1G4	2G4	…	237G4	238G4	239G4
DB9		0G3	1G3	2G3	…	237G3	238G3	239G3
DB8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
DB7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
DB6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
DB5	C4	0B5	1B5	2B5	…	237B5	238B5	239B5
DB4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
DB3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
DB2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
DB1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
DB0		0B0	1B0	2B0	…	237B0	238B0	239B0

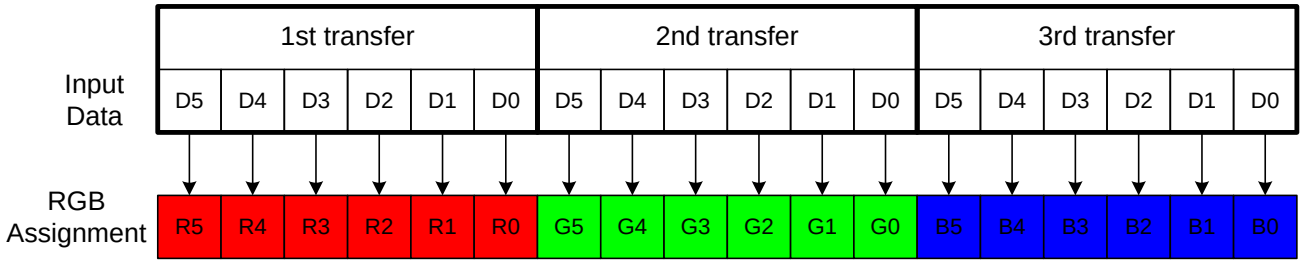
7.5.8. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the DPI [2:0] bit to “110”. When RCM [1:0] are set to “10” and ENABLE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[5:0]) according to the ENABLE signal when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via DB[5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)



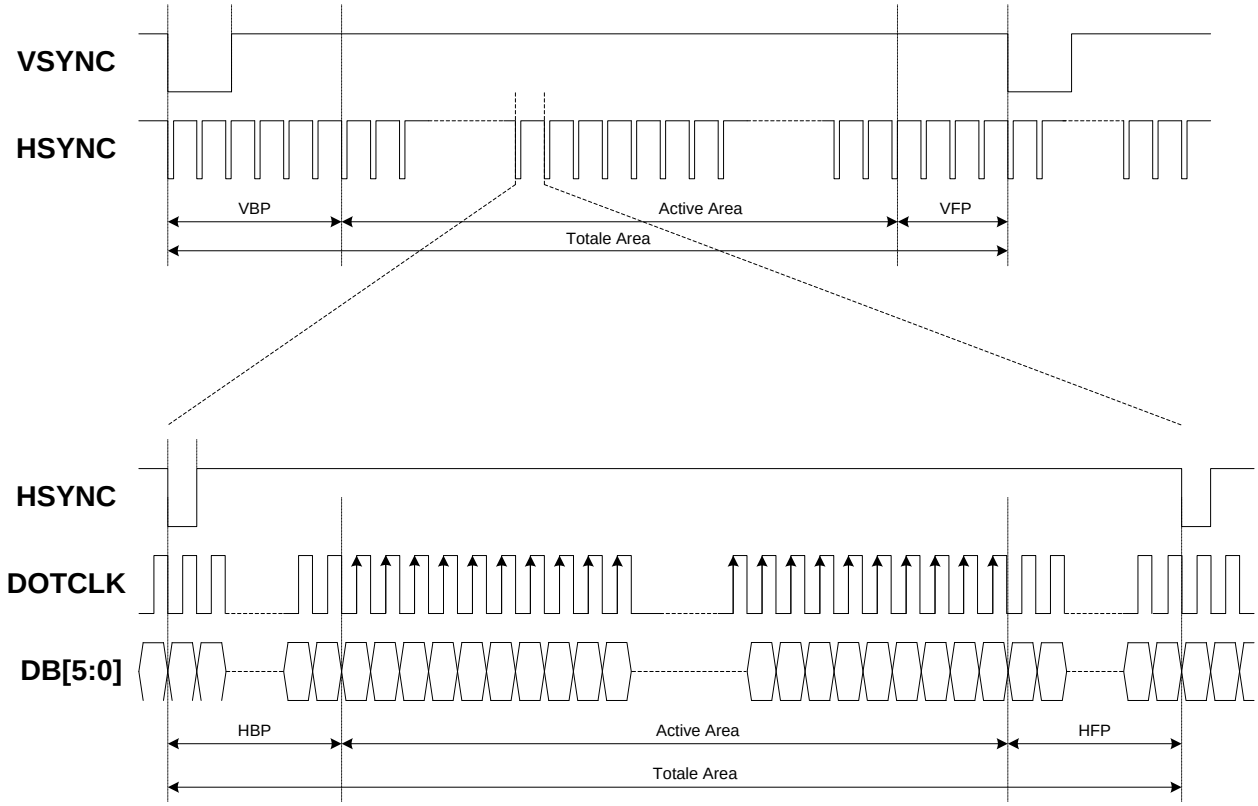
262K color: 18-bit/pixel (RGB 6-6-6 bits input)



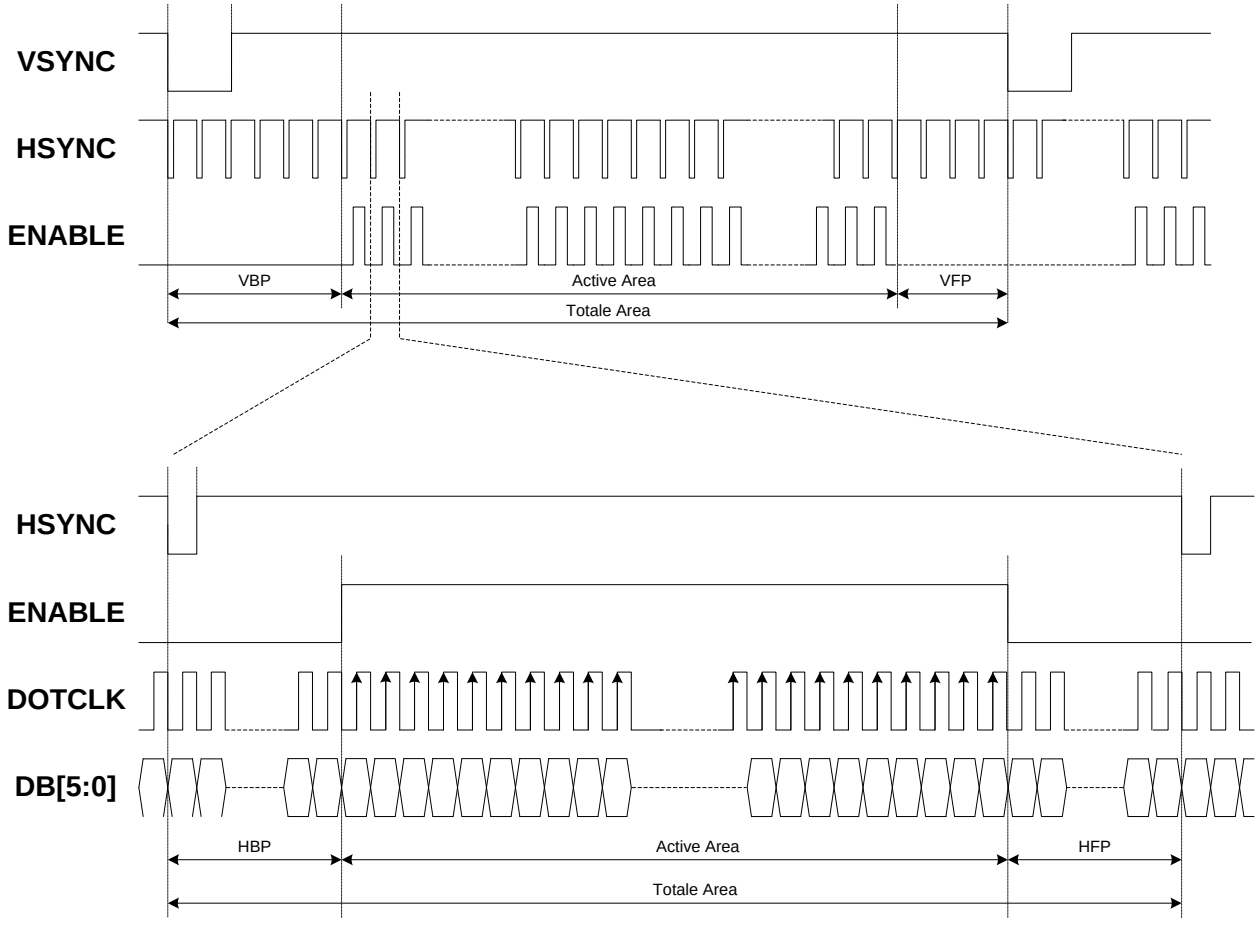
ILI9340X has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

SYNC Mode, RCM[1:0]="11"

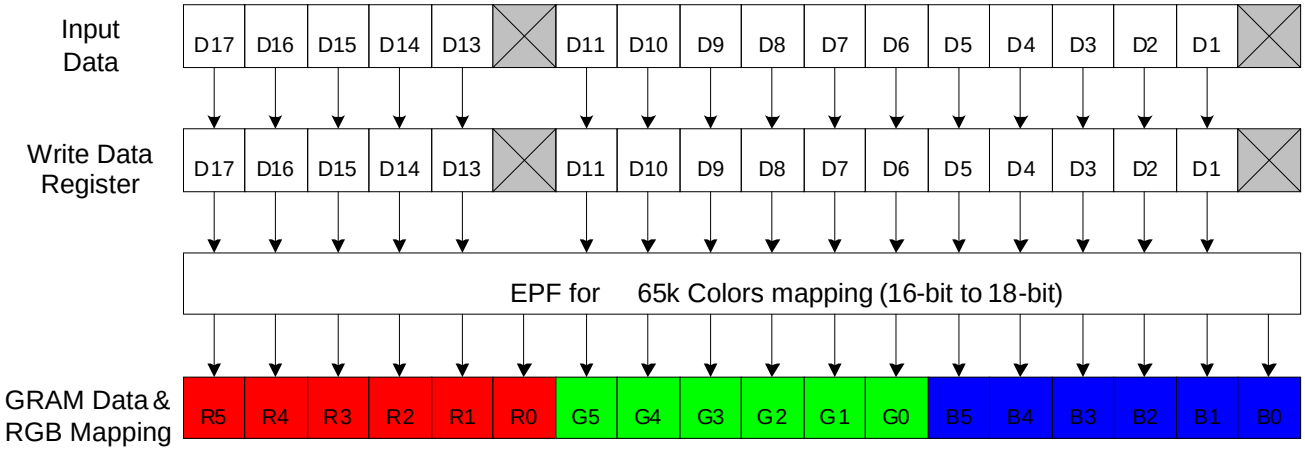


DE Mode, RCM[1:0]="10"



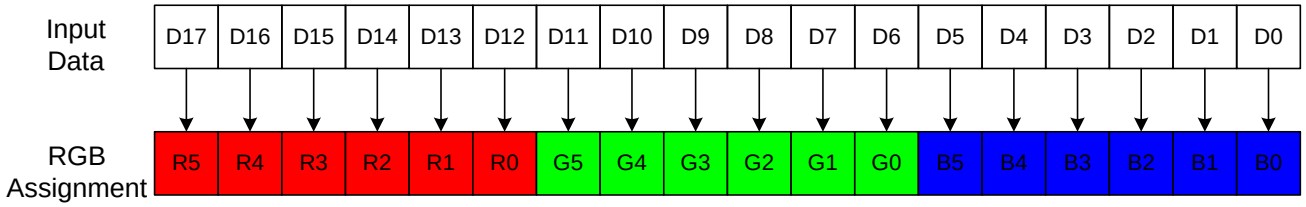
7.5.9. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (DB[17:13] & DB[11:1]) according to the ENABLE signal. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via DB[17:13] and DB[11:1] according to the VFP/VBP and HFP/HBP settings. The unused DB12 and DB0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.



7.5.10. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the ENABLE signal when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via DB[17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.



8. Command

8.1. Command List

Description of Level 1 Command													
Command Function	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NOP	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Read Display Identification Information	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1 [7:0]								E3
	1	↑	1	XX	ID2 [7:0]								00
	1	↑	1	XX	ID3 [7:0]								00
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D31	D30	D29	D28	D27	D26	D25	D24	00
	1	↑	1	XX	D23	D22	D21	D20	D19	D18	D17	D16	61
	1	↑	1	XX	D15	D14	D13	D12	D11	D10	D9	D8	00
	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00
Read Display Power Mode	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D7	D6	D5	D4	D3	D2	0	0	08
Read Display MADCTL	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D7	D6	D5	D4	D3	D2	0	0	00
Read Display Pixel Format	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	DPI [2:0]			0	DBI [2:0]			06
Read Display Image Format	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D7	0	D5	0	0	D2	D1	D0	00
Read Display Signal Mode	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D7	D6	D5	D4	D3	D2	0	0	00
Read Display Self-Diagnostic Result	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D7	D6	0	0	0	0	0	0	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep Out	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode On	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode On	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion Off	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion On	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Gamma Set	0	1	↑	XX	0	0	1	0	0	1	1	0	26h
	1	1	↑	XX	0	0	0	0	0	0	0	GC	01
Display Off	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display On	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	XX
	1	1	↑	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	XX
	1	1	↑	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	XX
	1	1	↑	XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	XX
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	XX
	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	XX
	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	XX
	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	XX

Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D1 [17:0]									XX
	1	1	↑	Dx [17:0]									XX
	1	1	↑	Dn [17:0]									XX
Memory Read	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D1 [17:0]									XX
	1	↑	1	Dx [17:0]									XX
	1	↑	1	Dn [17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR [15:8]								00
	1	1	↑	XX	SR [7:0]								00
	1	1	↑	XX	ER [15:8]								01
	1	1	↑	XX	ER [7:0]								3F
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA [15:8]								00
	1	1	↑	XX	TFA [7:0]								00
	1	1	↑	XX	VSA [15:8]								01
	1	1	↑	XX	VSA [7:0]								40
	1	1	↑	XX	BFA [15:8]								00
	1	1	↑	XX	BFA [7:0]								00
Tearing Effect Line Off	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line On	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	0	0	0	0	0	0	0	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP [15:8]								00
	1	1	↑	XX	VSP [7:0]								00
Idle Mode Off	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode On	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	0	DPI [2:0]			0	DBI [2:0]			66
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	0	0	0	0	0	0	0	STS [8]	00
	1	1	↑	XX	STS[7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	0	0	0	0	0	0	GTS[8]	00
	1	↑	1	XX	GTS[7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00
Read CTRL Display	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	00
Write Color Enhancement Control	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
	1	1	↑	XX	CE[3:0]				0	0	0	0	00
Read Color Enhancement Control	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	CE[3:0]				0	0	0	0	00

Read Automatic Brightness Control Self-Diagnostic Result	0	1	↑	XX	0	1	1	0	1	0	0	0	68H
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D7	D6	X	X	X	X	X	X	00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1 [7:0]								E3
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID2 [7:0]								00
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID3 [7:0]								00

Description of Level 2 Command													
Command Function	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	ByPass_MODE	RCM [1:0]		0	VSPL	HSPL	DPL	EPL	40
Frame Rate Control (In Normal Mode)	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
	1	1	↑	XX	0	0	0	0	0	0	DIVA [1:0]		00
	1	1	↑	XX	0	0	0	RTNA [4:0]					1F
Frame Rate Control (In Idle Mode)	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
	1	1	↑	XX	0	0	0	0	0	0	DIVB [1:0]		02
	1	1	↑	XX	0	0	0	RTNB [4:0]					1F
Frame Rate Control (In Partial Mode)	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
	1	1	↑	XX	0	0	0	0	0	0	DIVC [1:0]		00
	1	1	↑	XX	0	0	0	RTNC [4:0]					1F
Display Inversion Control	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
	1	1	↑	XX	DINVA[1:0]		0	0	0	0	0	0	80
	1	1	↑	XX	DINVB[1:0]		0	0	0	0	0	0	00
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	VFP [7:0]								02
	1	1	↑	XX	VBP [7:0]								02
	1	1	↑	XX	0	0	0	HFP [4:0]					0A
	1	1	↑	XX	HBP [7:0]								14
Display Function Control	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XX	0	0	0	0	PTG [1:0]		PT [1:0]		0A
	1	1	↑	XX	1	GS	SS	SM	ISC [3:0]				02
	1	1	↑	XX	0	0	NL [5:0]						27
	1	1	↑	XX	0	0	PCDIV [5:0]						04
VCOM/VDV/VRH Control (Power Control VREF2)	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
	1	1	↑	XX	0	VCOM[6:0]							30
	1	1	↑	XX	0	0	VRH[5:0]						0B
	1	1	↑	XX	0	0	VDV[5:0]						20
VGH/VGL/DDVDH/DDVDL (Power Control 1)	0	1	↑	XX	1	0	1	1	1	0	1	1	BBh
	1	1	↑	XX	0	VGH SEL			0	VGL SEL			33h
	1	1	↑	XX	0	DDVDH SEL			0	DDVDL SEL			34h
2 lane SPI selection	0	1	↑	XX	1	1	0	0	0	1	1	0	C6h
	1	1	↑	XX	0	0	0	0	0	TYPE	SPI2LANE	0	00
Level 3 Command Eable Control	0	1	↑	XX	1	1	0	0	1	1	1	1	CFh
	1	1	↑	XX	0	0	0	0	0	1	0	0	04
	1	1	↑	XX	0	0	0	0	0	0	0	EXTC	00
Read ID4	0	↑	1	XX	1	1	0	1	0	1	0	1	D5h
	1	↑	1	XX	0	0	0	0	0	0	0	0	00
	1	↑	1	XX	1	0	0	1	0	0	1	1	93
	1	↑	1	XX	0	1	0	0	0	0	0	0	40

Entry mode set	0	1	↑	XX	1	1	0	1	0	1	1	0	D6h
	1	1	↑	XX	0	0	0	0	0	0	DSTB	GAS	00
Get External Register by SPI	0	1	↑	XX	1	1	0	1	1	0	0	1	D9h
	1	1	↑	XX	0	0	0	ENSPI	SPI_EXT_ORD [3:0]				00
Digital Gamma Control 1	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
1st Parameter	1	1	↑	XX	RCA0[7:0]								XX
:	1	1	↑	XX	RCAn[7:0]								XX
64th Parameter	1	1	↑	XX	RCA63[7:0]								XX
Digital Gamma Control 2	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
1st Parameter	1	1	↑	XX	BCA0[7:0]								XX
:	1	1	↑	XX	BCAn[7:0]								XX
64th Parameter	1	1	↑	XX	BCA63[7:0]								XX
Positive Gamma Correction	0	1	↑	XX	1	1	1	0	0	1	0	0	E4h
	1	1	↑	XX	0	0	0	0	VP0 [3:0]				00
	1	1	↑	XX	0	0	VP1 [5:0]						05
	1	1	↑	XX	0	0	VP2 [5:0]						12
	1	1	↑	XX	0	0	0	0	VP4 [3:0]				09
	1	1	↑	XX	0	0	0	VP6 [4:0]					17
	1	1	↑	XX	0	0	0	0	VP13 [3:0]				08
	1	1	↑	XX	0	VP20 [6:0]							40
	1	1	↑	XX	VP36 [3:0]				VP27 [3:0]				55
	1	1	↑	XX	0	VP43 [6:0]							50
	1	1	↑	XX	0	0	0	0	VP50 [3:0]				04
	1	1	↑	XX	0	0	0	VP57 [4:0]					0A
	1	1	↑	XX	0	0	0	0	VP59 [3:0]				07
	1	1	↑	XX	0	0	VP61 [5:0]						21
	1	1	↑	XX	0	0	VP62 [5:0]						24
	1	1	↑	XX	0	0	0	0	VP63 [3:0]				0D

Negative Gamma Correction	0	1	↑	XX	1	1	1	0	0	1	0	1	E5h
	1	1	↑	XX	0	0	0	0	VN0 [3:0]				00
	1	1	↑	XX	0	0	VN1 [5:0]						05
	1	1	↑	XX	0	0	VN2 [5:0]						11
	1	1	↑	XX	0	0	0	0	VN4 [3:0]				09
	1	1	↑	XX	0	0	0	VN6 [4:0]					17
	1	1	↑	XX	0	0	0	0	VN13 [3:0]				09
	1	1	↑	XX	0	VN20 [6:0]							40
	1	1	↑	XX	VN36 [3:0]				VN27 [3:0]				46
	1	1	↑	XX	0	VN43 [6:0]							4E
	1	1	↑	XX	0	0	0	0	VN50 [3:0]				08
	1	1	↑	XX	0	0	0	VN57 [4:0]					0F
	1	1	↑	XX	0	0	0	0	VN59 [3:0]				0C
	1	1	↑	XX	0	0	VN61 [5:0]						21
	1	1	↑	XX	0	0	VN62 [5:0]						25
	1	1	↑	XX	0	0	0	0	VN63 [3:0]				0D
MADCTL EOR	0	1	↑	XX	1	1	1	0	1	1	0	0	ECh
	1	1	↑	XX	MY_EOR	MX_EOR	MV_EOR	ML_EOR	BGR_EOR	0	0	REV	49
LED_EN LED_PWM	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
	1	1	↑	XX	0	1	0	1	0	0	0	0	50
	1	1	↑	XX	0	LED_EN_OEB	LED_EN_OUT	LED_PWM_OEB	LED_PWM_OUT	0	0	0	00
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
	1	1	↑	XX	0	0	EPF[1:0]		0	0	MDT[1:0]		00
	1	1	↑	XX	0	0	ENDIAN	0	DM[1:0]		RM	RIM	00

NV Momory Write	0	1	↑	XX	1	1	1	1	1	1	0	1	FDh
	1	1	↑	XX	PGM_ADR[7:0]								XX
	1	1	↑	XX	PGM_ADR[15:8]								XX
	1	1	↑	XX	PGM_DATA[7:0]								XX
NV Momory Protation Key	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
	1	1	↑	XX	KEY[23:16]								55
	1	1	↑	XX	KEY[15:8]								AA
	1	1	↑	XX	KEY[7:0]								66
NV Momory Status Read	0	1	↑	XX	1	1	1	1	1	1	1	1	FFh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	MADCTL_CNT[1:0]		ID3_CNT[1:0]		ID2_CNT[1:0]		ID1CNT[1:0]		XX
	1	↑	1	XX	OTP BUSY	0	0	GAMMA MARK	0	VMF_MARK[2:0]			XX

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to CF and D0 to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP (00h).

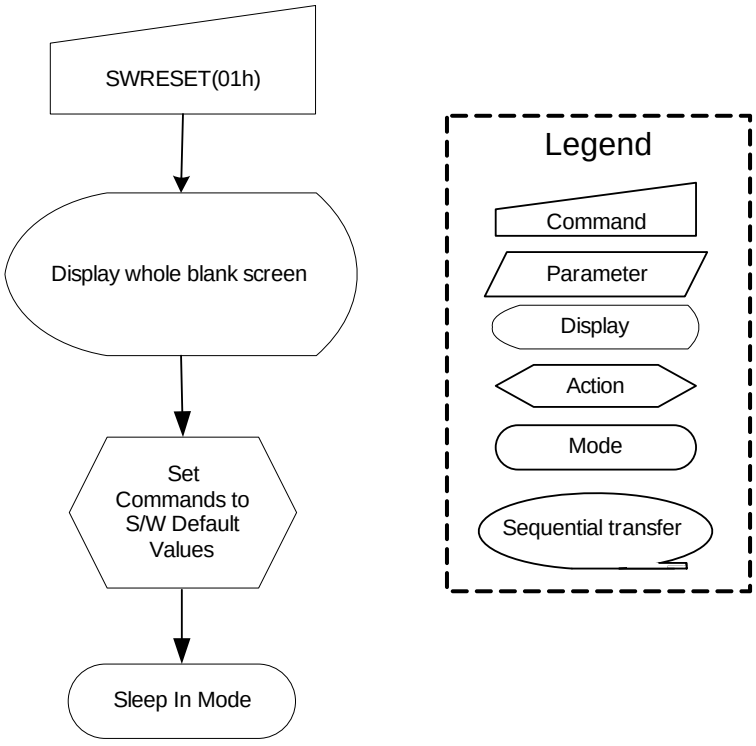
Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9340X is in Sleep Out mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep In mode and Sleep Out mode.

8.2. Description of Level 1 Command

8.2.1. NOP (00h)

<table>
<tr><th>00h</th><th colspan="13">NOP (No Operation)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter.</td></tr>
<tr><td>Description</td><td colspan="13">This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">None</td></tr>
</table>

8.2.2. Software Reset (01h)

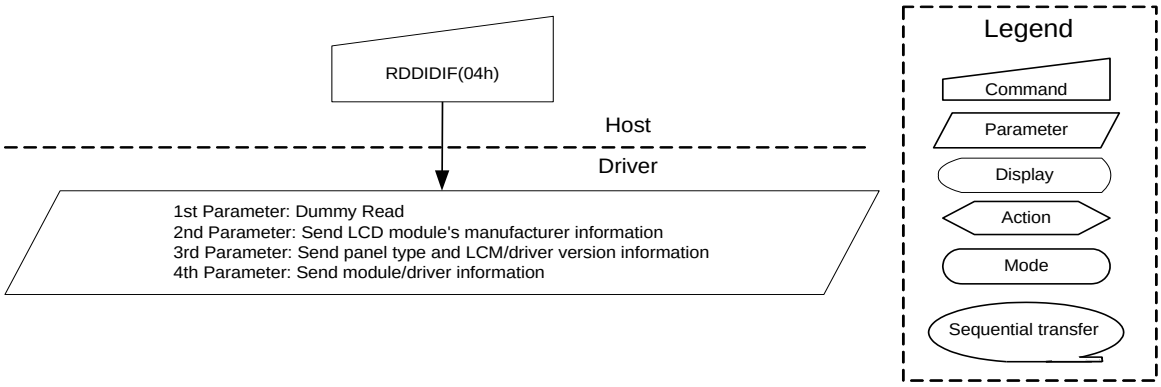
01h	SWRESET												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Parameter	No Parameter.												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command X = Don't care.												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Normal Mode On, Idle Mode On, Sleep Out — Yes Partial Mode On, Idle Mode Off, Sleep Out — Yes Partial Mode On, Idle Mode On, Sleep Out — Yes Sleep In — Yes												
Default	Status: Power On Sequence — Default Value: N/A SW Reset — N/A HW Reset — N/A												
Flow Chart													

8.2.3. Read display identification information (04h)

04h	RDDIDIF (Read Display Identification Information)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	ID1 [7:0]								E3
3rd Parameter	1	↑	1	XX	ID2 [7:0]								00
4th Parameter	1	↑	1	XX	ID3 [7:0]								00
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (ID1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (ID2 [7:0]): LCD module/driver version ID. The 4th parameter (ID3 [7:0]): LCD module/driver ID.												
Restriction													
Register Availability													
Default													
Flow Chart													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	OTP Value
SW Reset	OTP Value
HW Reset	OTP Value



8.2.4. Read Display Status (09h)

09h	RDDST (Read Display Status)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D31	D30	D29	D28	D27	D26	D25	D24	00
3rd Parameter	1	↑	1	XX	D23	D22	D21	D20	D19	D18	D17	D16	61
4th Parameter	1	↑	1	XX	D15	D14	D13	D12	D11	D10	D9	D8	00
5th Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	0	Booster Off
		1	Booster On
D30	Row address order	0	Top to Bottom (When MADCTL D7='0')
		1	Bottom to Top (When MADCTL D7='1')
D29	Column address order	0	Left to Right (When MADCTL D6='0').
		1	Right to Left (When MADCTL D6='1').
D28	Row/column exchange	0	Normal Mode (When MADCTL D5='0').
		1	Reverse Mode (When MADCTL D5='1').
D27	Vertical refresh	0	LCD Refresh Top to Bottom (When MADCTL D4='0')
		1	LCD Refresh Bottom to Top (When MADCTL D4='1').
D26	RGB/BGR order	0	RGB (When MADCTL D3='0')
		1	BGR (When MADCTL D3='1')
D25	Horizontal refresh order	0	LCD Refresh Left to Right (When MADCTL D2='0')
		1	LCD Refresh Right to Left (When MADCTL D2='1')
D24	Not used	0	---
D23	Not used	0	---
D22	Interface color pixel format definition	101	16-bit/pixel
D21			
D20		110	18-bit/pixel
D19	Idle mode On/Off	0	Idle Mode Off
		1	Idle Mode On
D18	Partial mode On/Off	0	Partial Mode Off
		1	Partial Mode On.
D17	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode.
D16	Display normal mode On/Off	0	Display Normal Mode Off.
		1	Display Normal Mode On.
D15	Vertical scrolling status	0	Scroll Off
D14	Not used	0	---
D13	Inversion status	0	Not defined
D12	All pixel On	0	Not defined
D11	All pixel Off	0	Not defined
D10	Display On/Off	0	Display is Off
		1	Display is On
D9	Tearing effect line On/Off	0	Tearing Effect Line Off
		1	Tearing Effect On
D[8:6]	Gamma curve selection	000	GC0
		001	Not defined
		010	Not defined
		011	Not defined
		other	Not defined
D5	Tearing effect line mode	0	Mode 1, V-Blanking only

			1	Mode 2, both H-Blanking and V-Blanking.
	D4	Not used	0	---
	D3	Not used	0	---
	D2	Not used	0	---
	D1	Not used	0	---
	D0	Not used	0	---

X = Don't care

Restriction

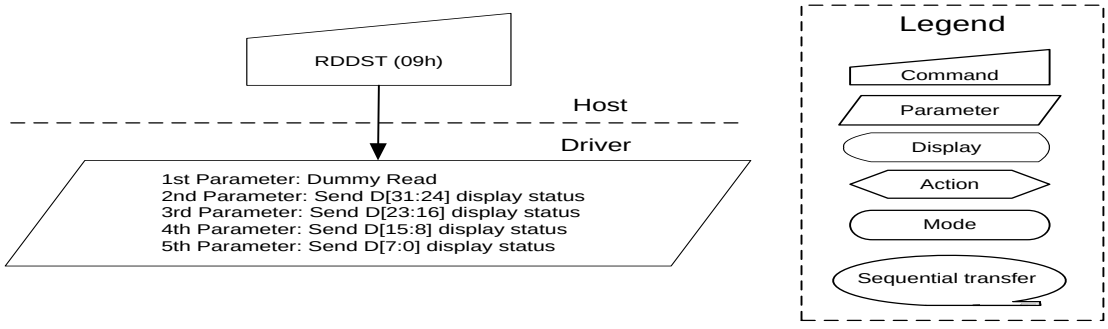
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	32'h00610000h
SW Reset	32'h00610000h
HW Reset	32'h00610000h

Flow Chart



8.2.5. Read Display Power Mode (0Ah)

0Ah	RDDPM (Read Display Power Mode)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	0	0	08

Description

This command indicates the current status of the display as described in the table below::

Bit	Value	Description	Comment
D7	0	Booster Off or has a fault.	---
	1	Booster On and working OK	---
D6	0	Idle Mode Off.	---
	1	Idle Mode On.	---
D5	0	Partial Mode Off.	---
	1	Partial Mode On.	---
D4	0	Sleep In Mode	---
	1	Sleep Out Mode	---
D3	0	Display Normal Mode Off.	---
	1	Display Normal Mode On	---
D2	0	Display is Off.	---
	1	Display is On	---
D1	--	Not Defined	Set to '0'
D0	--	Not Defined	Set to '0'

X = Don't care

Restriction

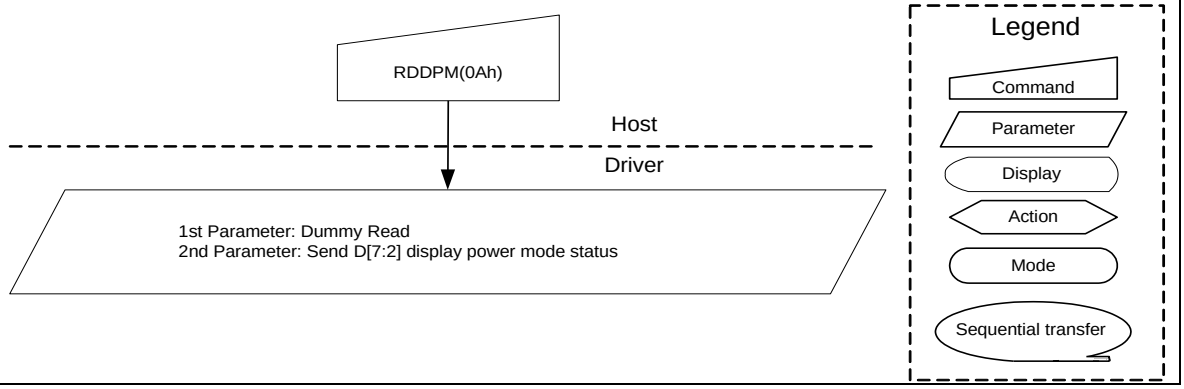
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h08h
SW Reset	8'h08h
HW Reset	8'h08h

Flow Chart



8.2.6. Read Display MADCTL (0Bh)

0Bh	RDDMADCTL (Read Display MADCTL)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	0	0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Value	Description	Comment
D7	0	Top to Bottom (When MADCTL D7='0').	---
	1	Bottom to Top (When MADCTL D7='1').	---
D6	0	Left to Right (When MADCTL D6='0')	---
	1	Right to Left (When MADCTL D6='1')	---
D5	0	Normal Mode (When MADCTL D5='0').	---
	1	Reverse Mode (When MADCTL D5='1')	---
D4	0	LCD Refresh Top to Bottom (When MADCTL D4='0')	---
	1	LCD Refresh Bottom to Top (When MADCTL D4='1').	---
D3	0	RGB (When MADCTL D3='0')	---
	1	BGR (When MADCTL D3='1').	---
D2	0	LCD Refresh Left to Right (When MADCTL D2='0').	---
	1	LCD Refresh Right to Left (When MADCTL D2='1').	---
D1	--	Not Defined	Set to '0'
D0	--	Not Defined	Set to '0'

X = Don't care

Restriction

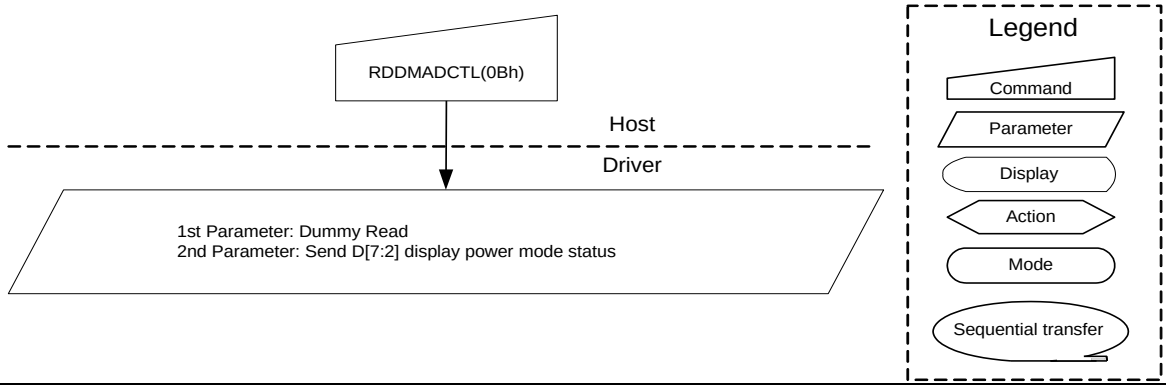
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	No Change
HW Reset	8'h00h

Flow Chart



8.2.7. Read Display Pixel Format (0Ch)

0Ch	RDDCOLMOD (Read Display Pixel Format)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	0	DPI [2:0]			0	DBI [2:0]			06

Description

This command indicates the current status of the display as described in the table below:

DPI [2:0]			RGB Interface Format
0	0	0	Reserved
0		1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

X = Don't care

Restriction

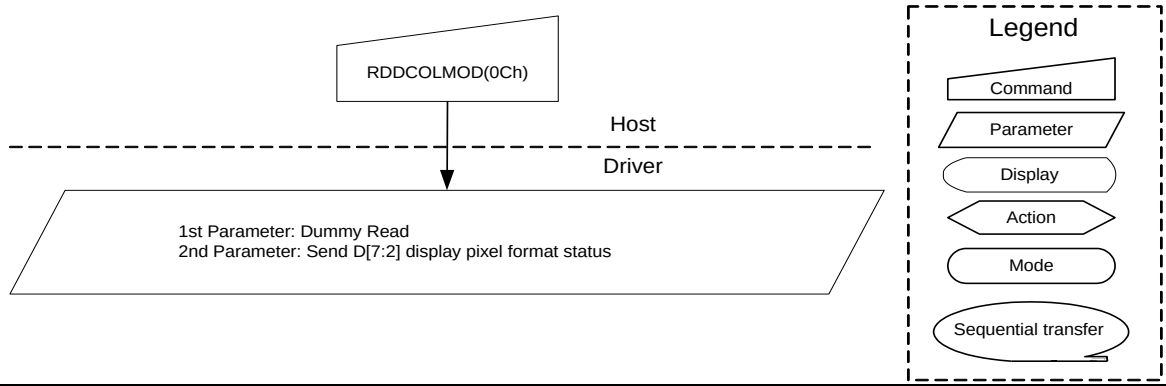
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DPI [2:0]	DBI [2:0]
Power On Sequence	3'b000	3'b110
SW Reset	No Change	No Change
HW Reset	3'b000	3'b110

Flow Chart



8.2.8. Read Display Image Format (0Dh)

0Dh	RDDIM (Read Display Image Mode)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	D7	0	D5	0	0	D2	D1	D0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Value	Description
D7	0	Vertical Scrolling is Off
	1	Vertical Scrolling is On
D5	0	Inversion is Off.
	1	Inversion is On.
D2	0	Gamma curve 1 (G2.2)
D1	0	
D0	0	

X = Don't care

Restriction

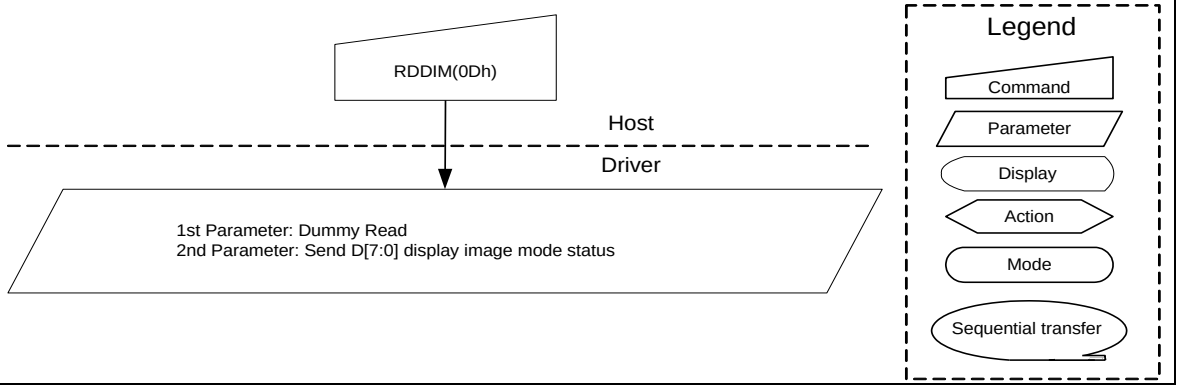
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.9. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	0	0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Value	Description
D7	0	Tearing ef ect line Off
	1	Tearing effect line On
D6	0	Tearing effect line mode 1
	1	Tearing effect line mode 2
D5	0	Horizontal sync. (RGB interface) Off
	1	Horizontal sync. (RGB interface) On
D4	0	Vertical sync. (RGB interface) Off
	1	Vertical sync. (RGB interface) On
D3	0	Pixel clock (DOTCLK, RGB interface) Off
	1	Pixel clock (DOTCLK, RGB interface) On
D2	0	Data enable (DE, RGB interface) Off
	1	Data enable (DE, RGB interface) On
D1	0	Reserved
D0	0	Reserved

X = Don't care

Restriction

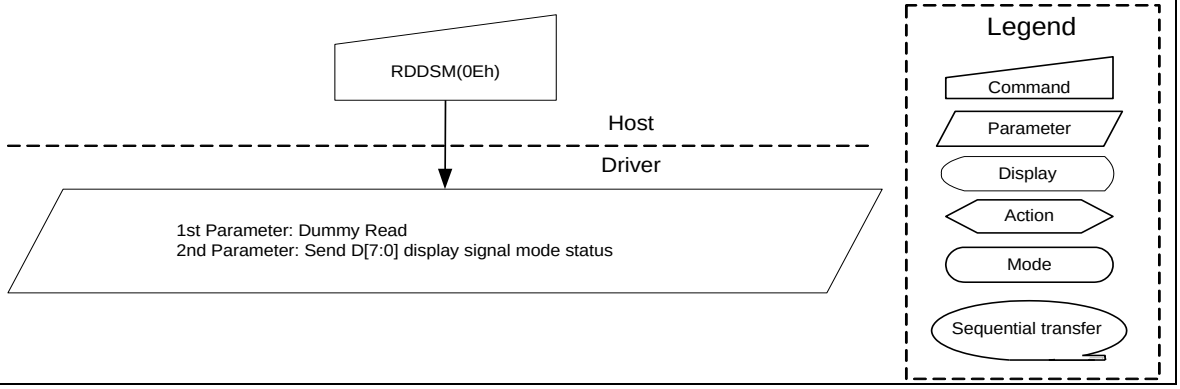
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.10. Read Display Self-Diagnostic Result (0Fh)

0Fh	RDDSDR (Read Display Self-Diagnostic Result)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	0	0	0	0	0	0	00

Description

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values loading work properly.
D6	Functionality Detection	Invert the D6 bit if the display is functionality
D5	Not Used	'0'
D4	Not Used	'0'
D3	Not Used	'0'
D2	Not Used	'0'
D1	Not Used	'0'
D0	Not Used	'0'

Restriction

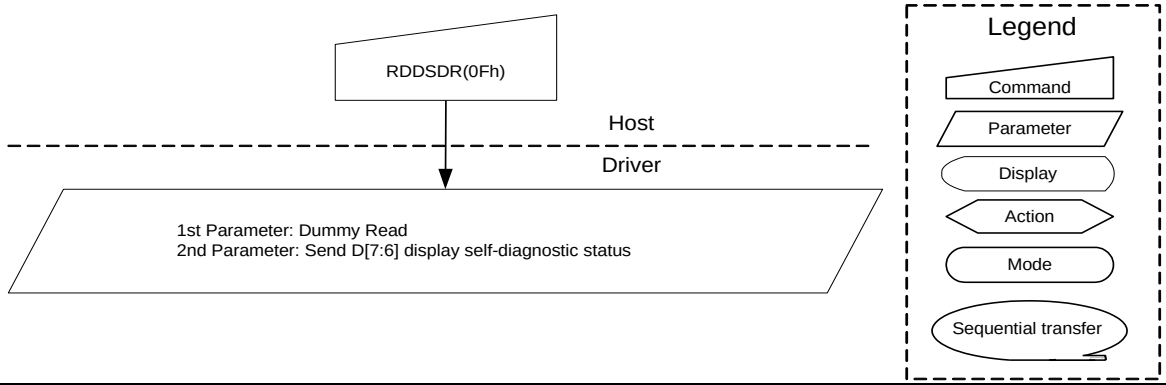
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.11. Enter Sleep Mode (10h)

10h	SLPIN (Enter Sleep Mode)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Parameter	No Parameter												
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. Out → Blank → STOP MCU interface and memory are still working and the memory keeps its contents. X = Don't care												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												

Register Availability

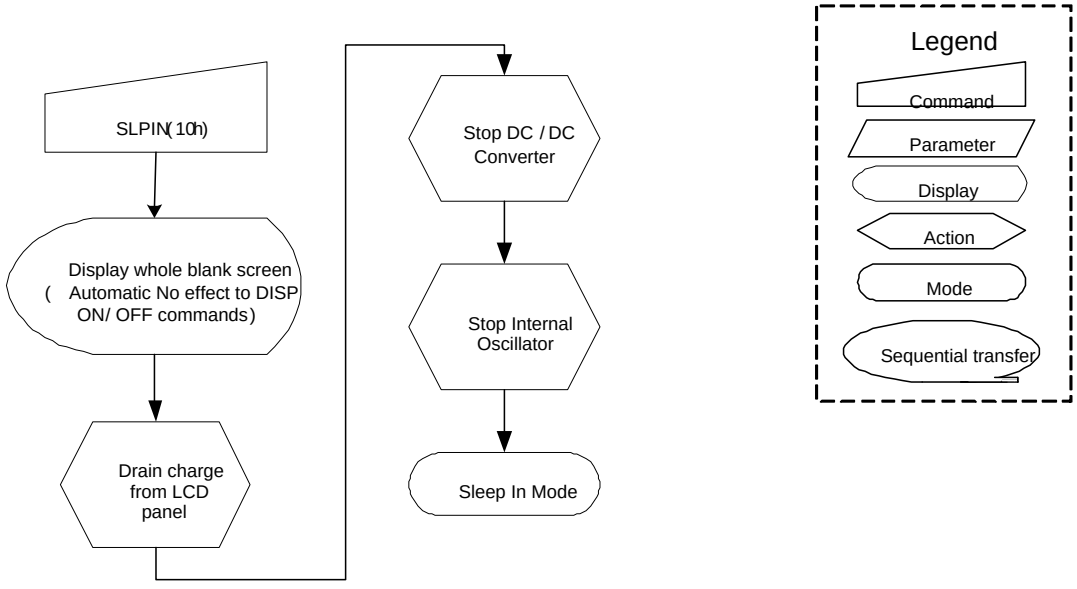
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

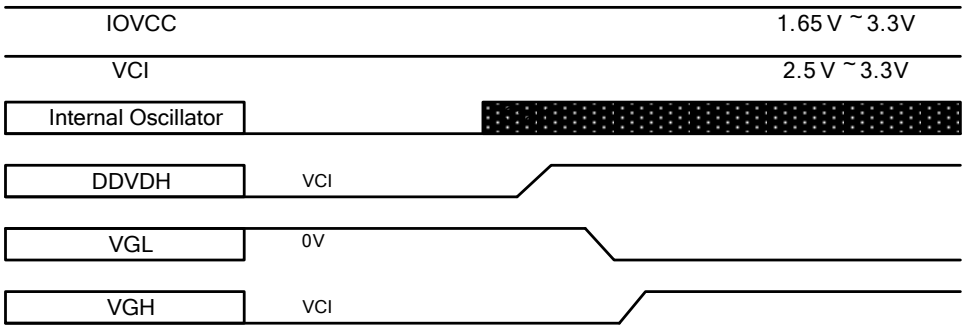
Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow Chart

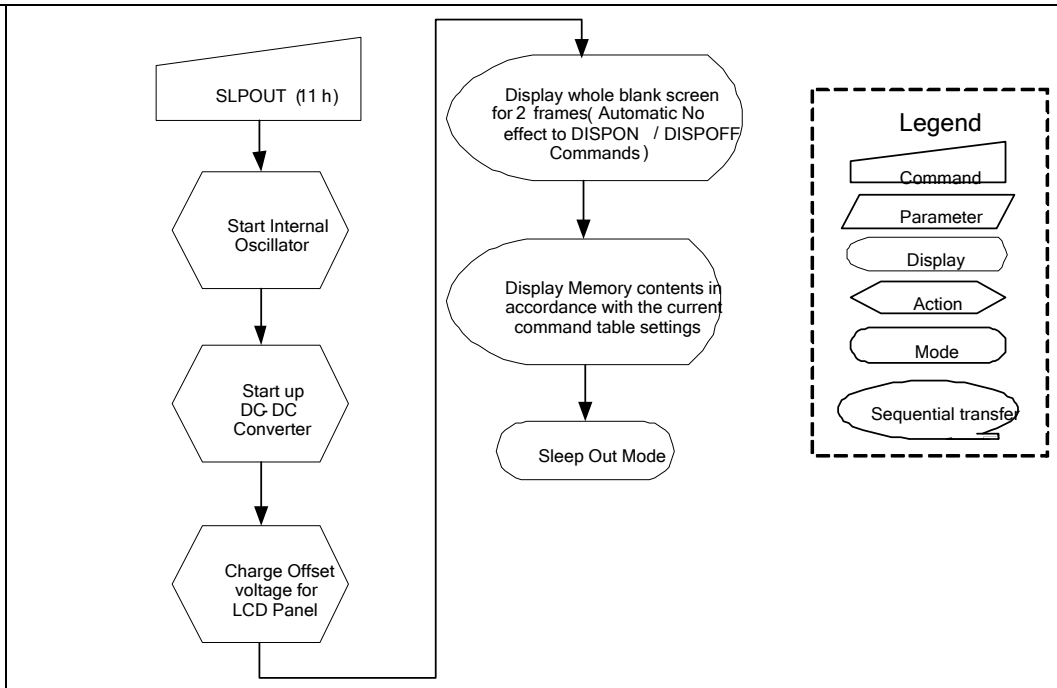
It takes 120msec to get into Sleep In mode after SLPIN command issued.



8.2.12. Sleep Out (11h)

<table>
<tr><th>11h</th><th colspan="13">SLPOUT (Sleep Out)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.
In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the clock circuits stabilize. The display module loads all display supplier’s factory default values to the registers during this 120msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>SW Reset</td><td>Sleep In Mode</td></tr><tr><td>HW Reset</td><td>Sleep In Mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">It takes 120msec to become Sleep Out mode after SLPOUT command issued.</td></tr>
</table>



8.2.13. Partial Mode On (12h)

<table>
<tr><th>12h</th><th colspan="12">PTLOn (Partial Mode On)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command turns on partial mode. The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>SW Reset</td><td>Normal Display Mode On</td></tr><tr><td>HW Reset</td><td>Normal Display Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">See Partial Area (30h)</td></tr>
</table>

8.2.14. Normal Display Mode On (13h)

<table>
<tr><th>13h</th><th colspan="13">NORON (Normal Display Mode On)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>SW Reset</td><td>Normal Display Mode On</td></tr><tr><td>HW Reset</td><td>Normal Display Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

8.2.15. Display Inversion Off (20h)

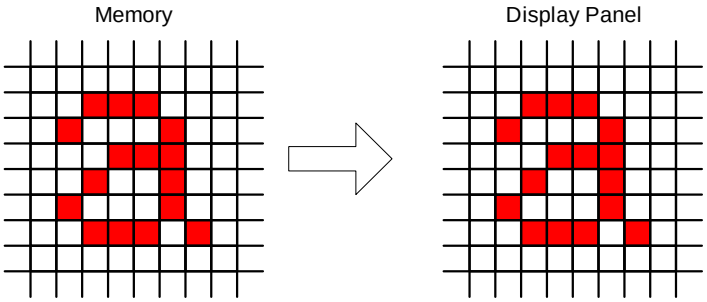
20h	DINVOFF (Display Inversion Off)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter												

Description

This command is used to recover from display inversion mode.

This command makes no change of the content of frame memory.

This command doesn't change any other status.



X = Don't care

Restriction

This command has no effect when module is already in Display Inversion Off mode.

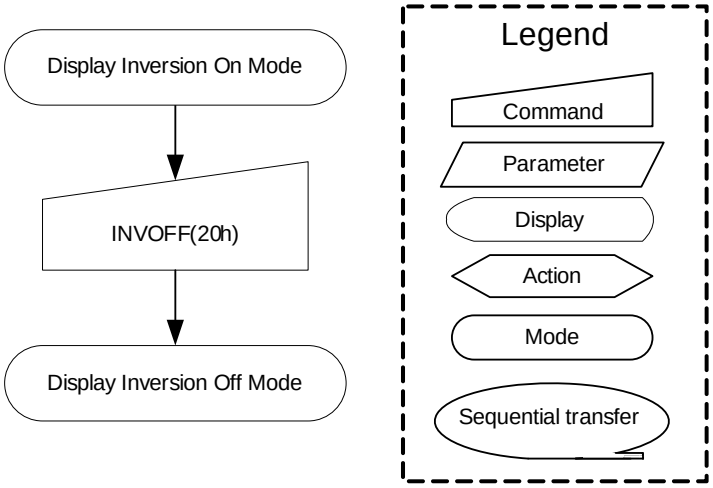
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

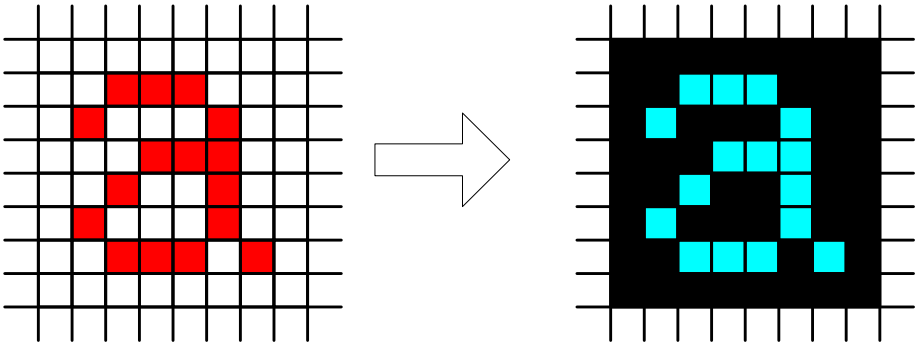
Default

Status	Default Value
Power On Sequence	Display Inversion Off
SW Reset	Display Inversion Off
HW Reset	Display Inversion Off

Flow Chart



8.2.16. Display Inversion On (21h)

21h	DINVON (Display Inversion On)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter												
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion Off command (20h) should be written.  X = Don't care												
Restriction	This command has no effect when module is already in Display Inversion ON mode												

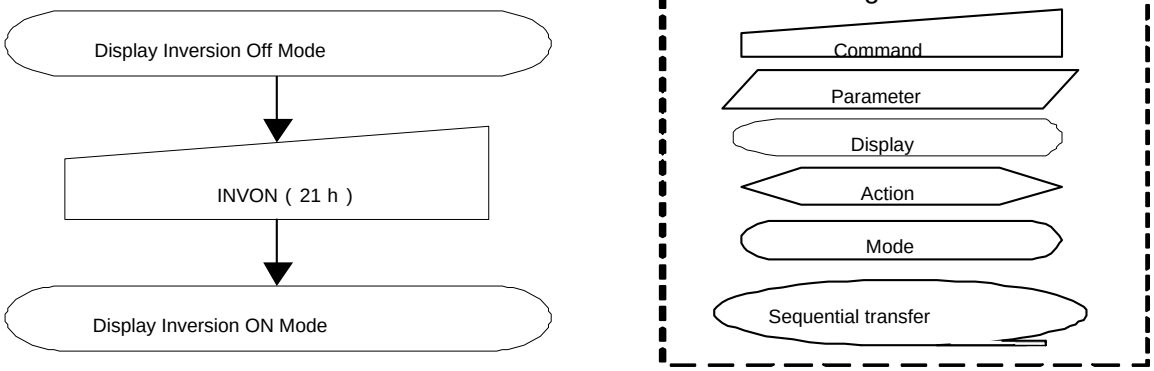
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
SW Reset	Display Inversion Off
HW Reset	Display Inversion Off

Flow Chart



8.2.17. Gamma Set (26h)

26h	GAMSET (Gamma Set)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	1	1	0	26h
Parameter	1	1	↑	XX	0	0	0	0	0	0	0	GC[0]	01

Description

This command is used to select the desired Gamma curve for the current display. Just one gamma curves can be selected.

The curve is selected by setting the appropriate bit in the parameter as described in the Table:

GC[0]	Curve Selected
1h	Gamma curve 1 (G2.2)

Note: All other values are undefined.

X = Don't care

Restriction

Values of GC [0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

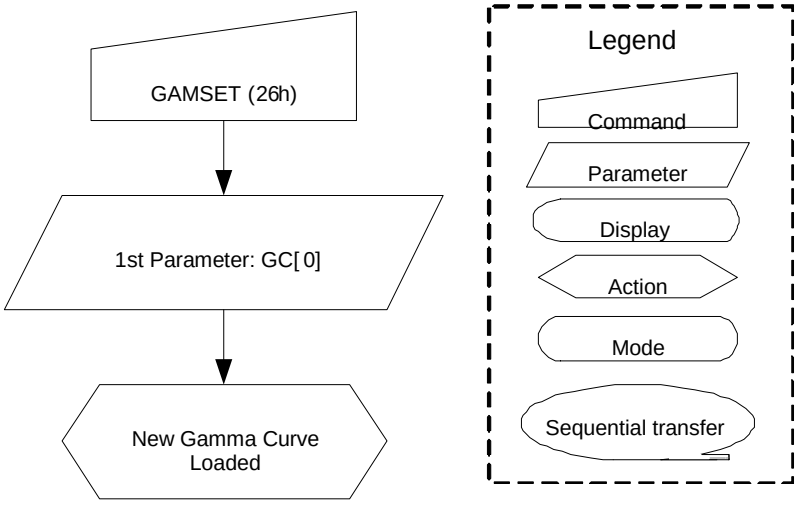
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

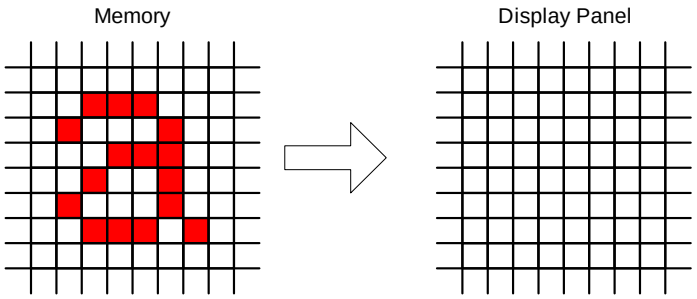
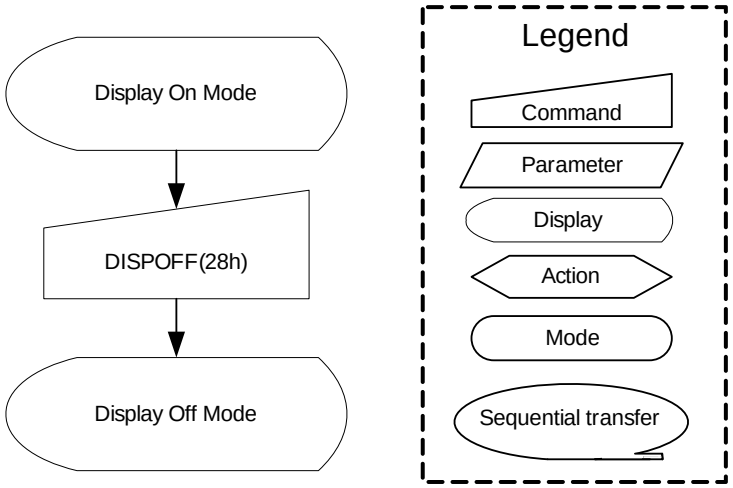
Default

Status	Default Value
Power On Sequence	8'h01h
SW Reset	8'h01h
HW Reset	8'h01h

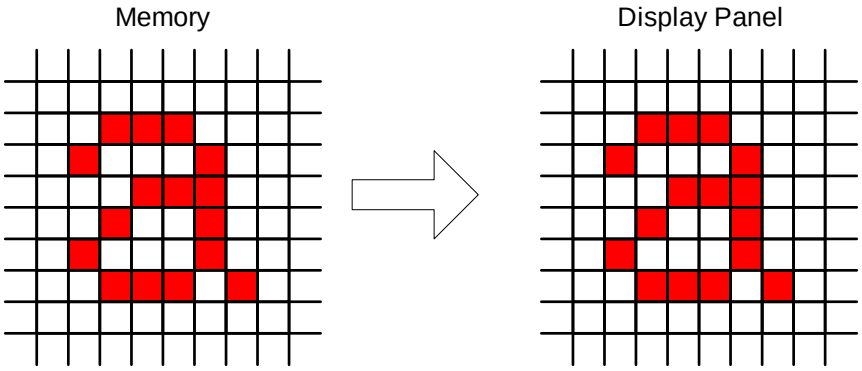
Flow Chart



8.2.18. Display Off (28h)

<table>
<tr><th>28h</th><th colspan="13">DISPOFF (Display Off)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into Display Off mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
 
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in Display Off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>SW Reset</td><td>Display Off</td></tr><tr><td>HW Reset</td><td>Display Off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

8.2.19. Display On (29h)

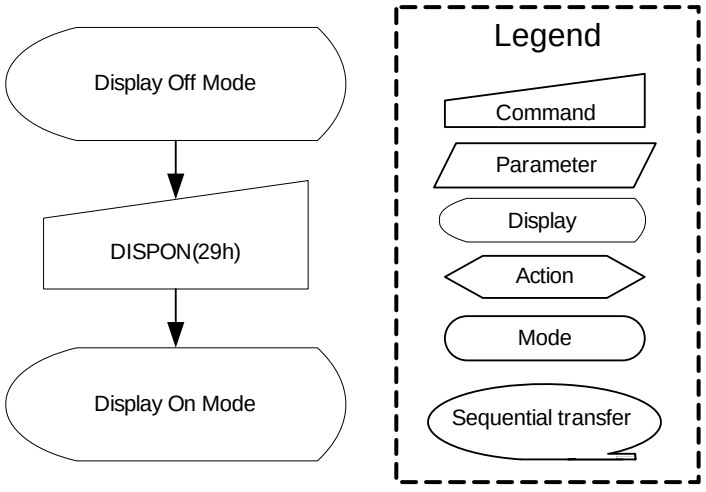
29h	DISPON (Display On)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Parameter	No Parameter												
Description	This command is used to recover from Display Off mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status  X = Don't care.												
Restriction	This command has no effect when module is already in Display On mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart

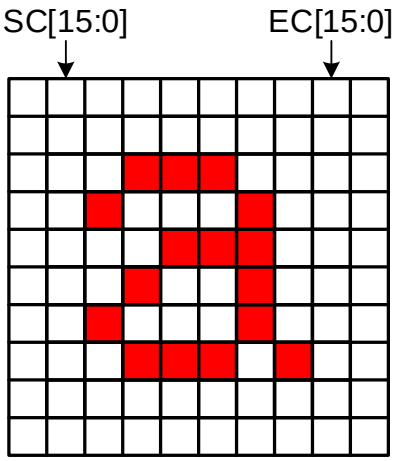


8.2.20. Column Address Set (2Ah)

2Ah	CASET (Column Address Set)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	**Note1**
2ndParameter	1	1	↑	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd Parameter	1	1	↑	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	**Note1**
4th Parameter	1	1	↑	XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



X = Don't care

Restriction

SC [15:0] always must be equal to or less than EC [15:0].

Note 1: When SC [15:0] or EC [15:0] is greater than 00EFh (When MADCTL's D5 = 0) or 013Fh (When MADCTL's D5 = 1), data of out of range will be ignored

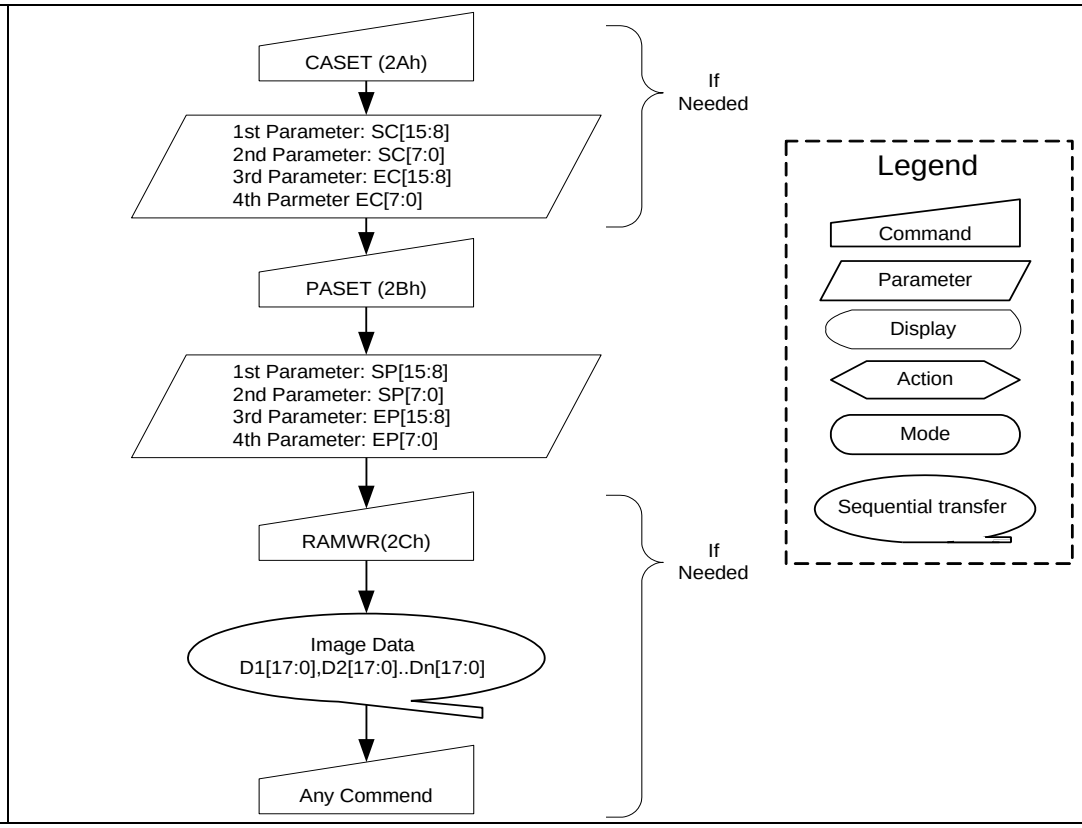
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC [15:0]=0000h	EC [15:0]=00EFh
SW Reset	SC [15:0]=0000h	If MADCTL's D5 = 0: EC [15:0]=00EFh If MADCTL's D5 = 1: EC [15:0]=013Fh
HW Reset	SC [15:0]=0000h	EC [15:0]=00EFh

Flow Chart

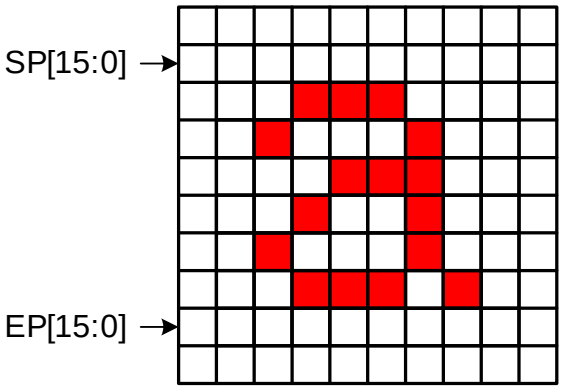


8.2.21. Page Address Set (2Bh)

2Bh	PASET (Page Address Set)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
1st Parameter	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	**Note1**
2ndParameter	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rdParameter	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	**Note1**
4th Parameter	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



X = Don't care

Restriction

SP [15:0] always must be equal to or less than EP [15:0]

Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL's D5 = 0) or 00EFh (When MADCTL's D5 = 1), data of out of range will be ignored.

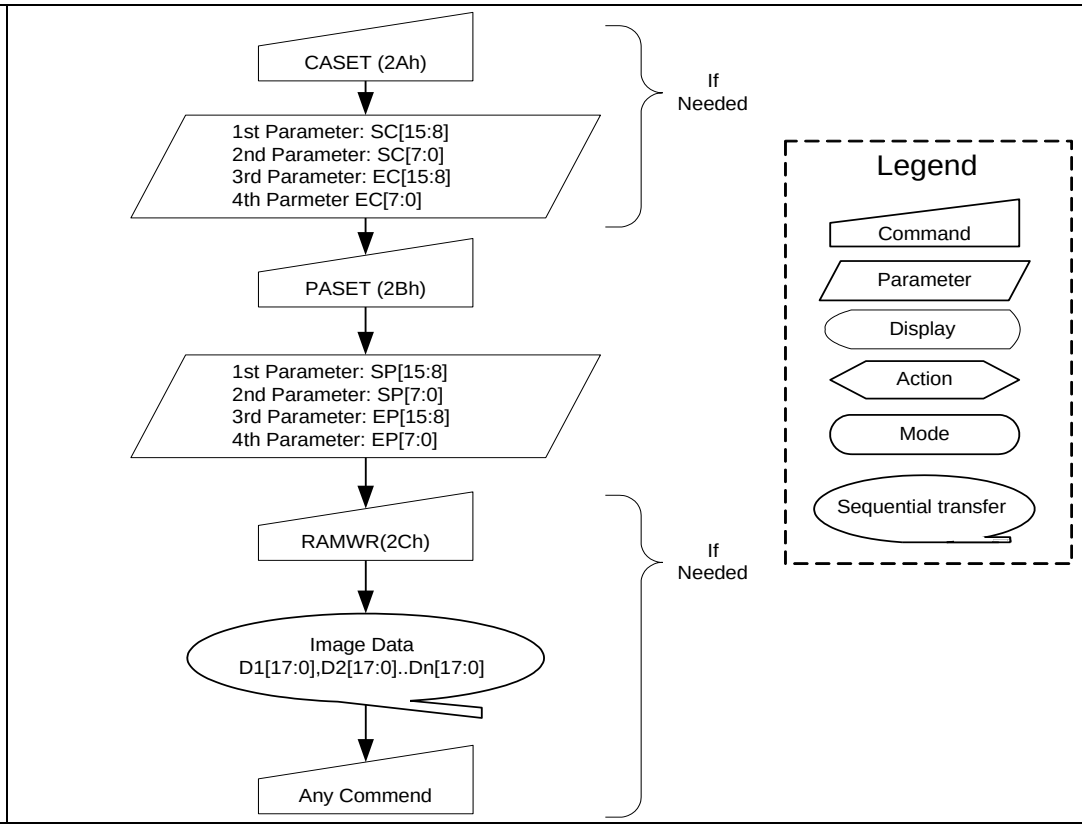
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP [15:0]=0000h	EP [15:0]=013Fh
SW Reset	SP [15:0]=0000h	If MADCTL's D5 = 0: EP [15:0]=013Fh If MADCTL's D5 = 1: EP [15:0]=00EFh
HW Reset	SP [15:0]=0000h	EP [15:0]=013Fh

Flow Chart



8.2.22. Memory Write (2Ch)

2Ch	RAMWR (Memory Write)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
1st Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
Nth Parameter	1	1	↑	Dn [17:0]									XX
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.												
Restriction	In all color modes, there is no restriction on length of parameters.												

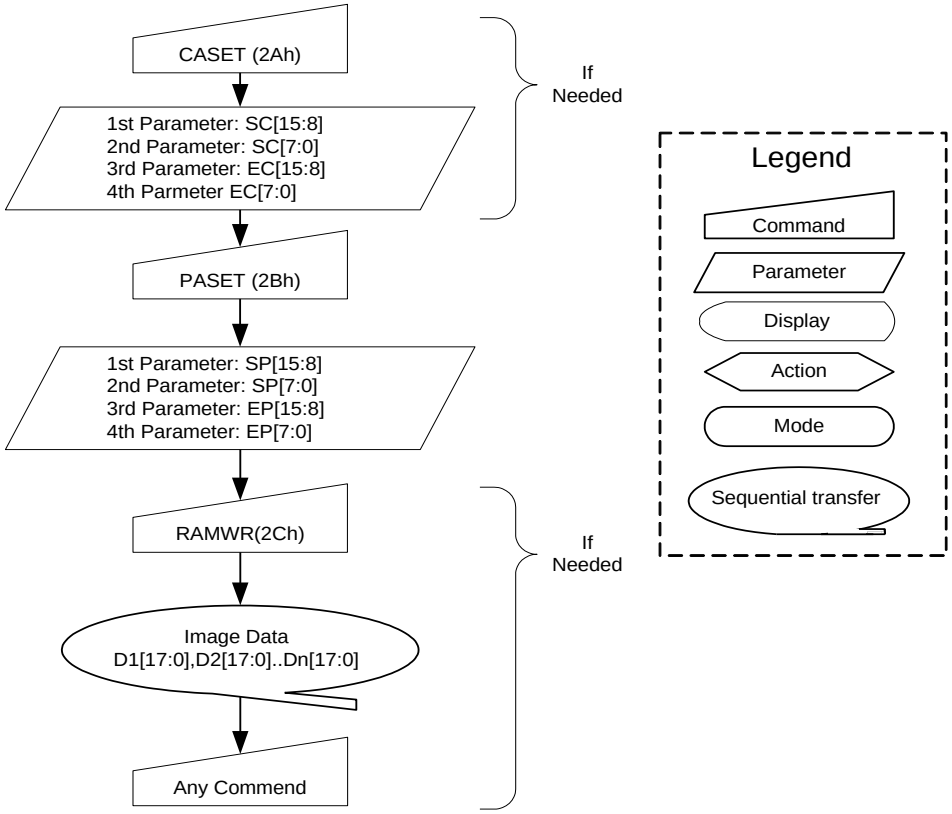
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart



8.2.23. Memory Read (2Eh)

2Eh	RAMRD (Memory Read)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
1st Parameter	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
(N+1)th Parameter	1	1	↑	Dn [17:0]									XX

Description

This command transfers image data from ILI9340X's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.

If Memory Access control D5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If Memory Access Control D5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

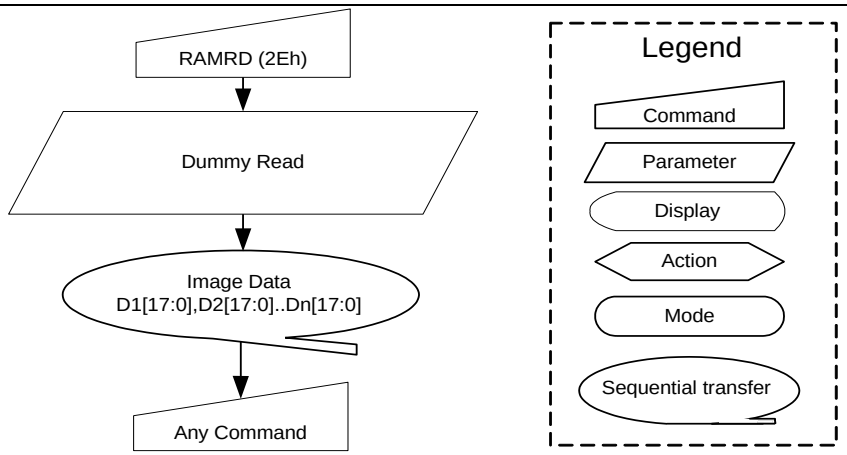
There is no restriction on length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart	

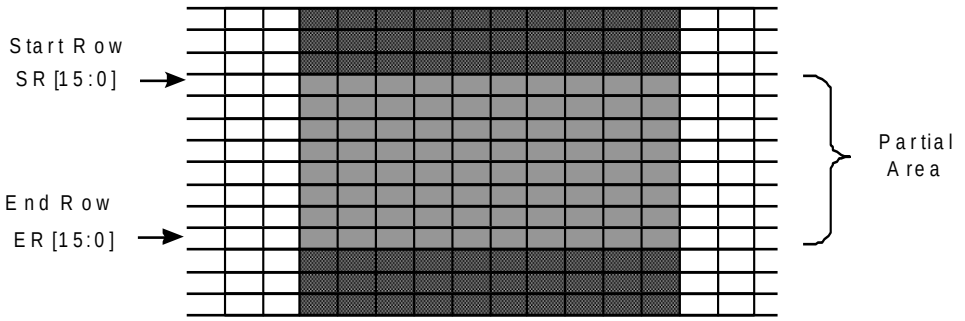
8.2.24. Partial Area (30h)

30h	PLTAR (Partial Area)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR[15:8]								00
2nd Parameter	1	1	↑	XX	SR[7:0]								00
3rd Parameter	1	1	↑	XX	ER[15:8]								01
4th Parameter	1	1	↑	XX	ER[7:0]								3F

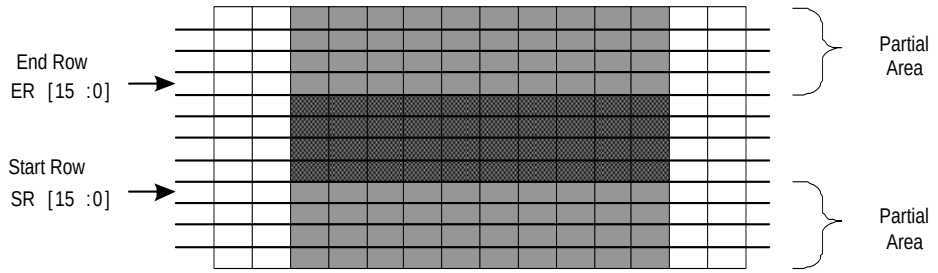
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

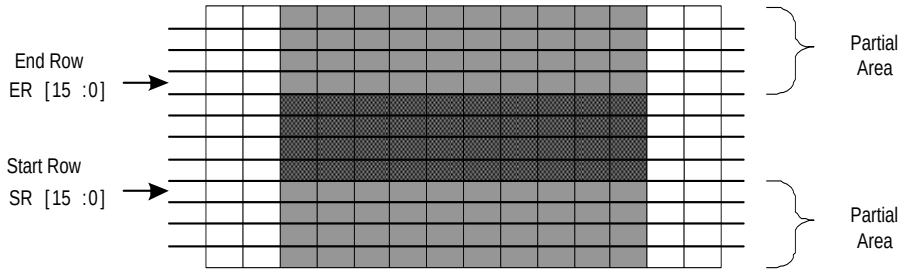
If End Row>Start Row when MADCTL D4=0:-



If End Row>Start Row when MADCTL D4=1:-



If End Row<Start Row when MADCTL D4=0:-



If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction	SR [15…0] and ER [15…0] cannot be 0000h nor exceed 013Fh.

Register Availability

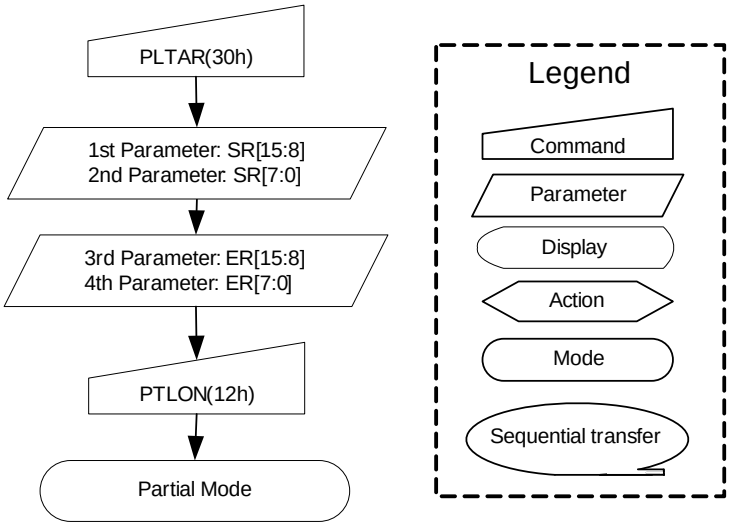
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

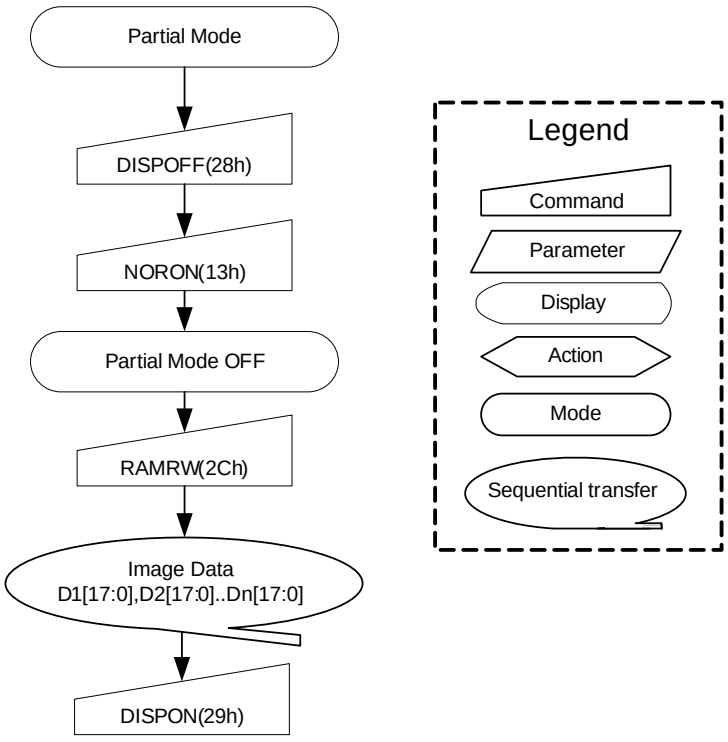
Status	Default Value	
	SR [15:0]	ER [15:0]
Power On Sequence	16'h0000h	16'h013Fh
SW Reset	16'h 0000h	16'h 013Fh
HW Reset	16'h 0000h	16'h 013Fh

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



8.2.25. Vertical Scrolling Definition (33h)

33h	VSCRDEF (Vertical Scrolling Definition)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								00
2nd Parameter	1	1	↑	XX	TFA [7:0]								00
3rd Parameter	1	1	↑	XX	VSA [15:8]								01
4th Parameter	1	1	↑	XX	VSA [7:0]								40
5th Parameter	1	1	↑	XX	BFA [15:8]								00
6th Parameter	1	1	↑	XX	BFA [7:0]								00

Description

This command defines the display vertical scrolling area.

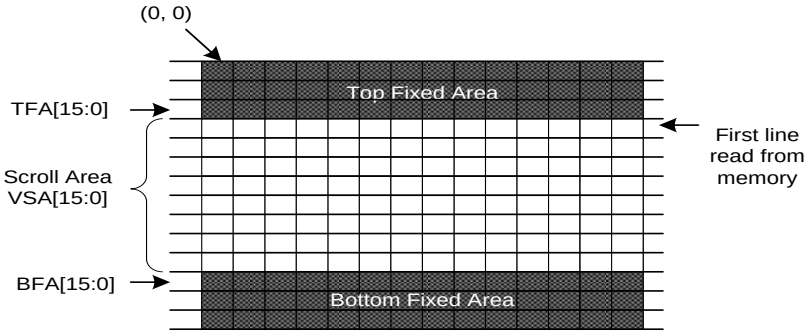
Memory Access Control (36h) D4 = 0:

The 1st & 2nd parameter, TFA[15:0], describe the Top Fixed Area in number of lines from the top of the Frame Memory. The top of the Frame Memory and top of the display device are aligned.

The 3rd & 4th parameter, VSA[15:0], describe the height of the Vertical Scrolling Area in number of lines of the Frame Memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[15:0], describe the Bottom Fixed Area in number of lines from the bottom of the Frame Memory. The bottom of the Frame Memory and bottom of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



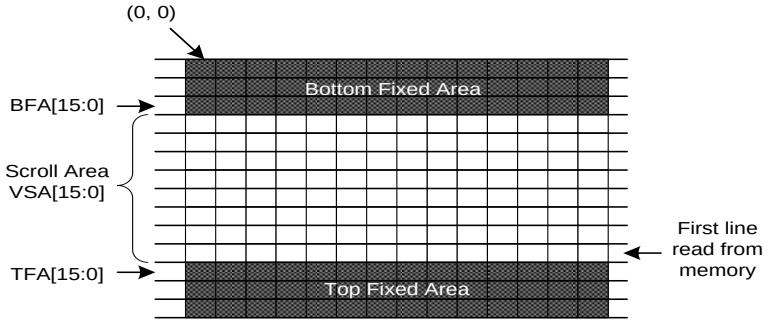
Memory Access Control (36h) D4 = 1:

The 1st & 2nd parameter, TFA[15:0], describe the Top Fixed Area in number of lines from the bottom of the Frame Memory. The bottom of the Frame Memory and bottom of the display device are aligned.

The 3rd & 4th parameter, VSA[15:0], describe the height of the Vertical Scrolling Area in number of lines of the Frame Memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[15:0], describe the Bottom Fixed Area in number of lines from the top of the Frame Memory. The top of the Frame Memory and top of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Restriction

Register Availability

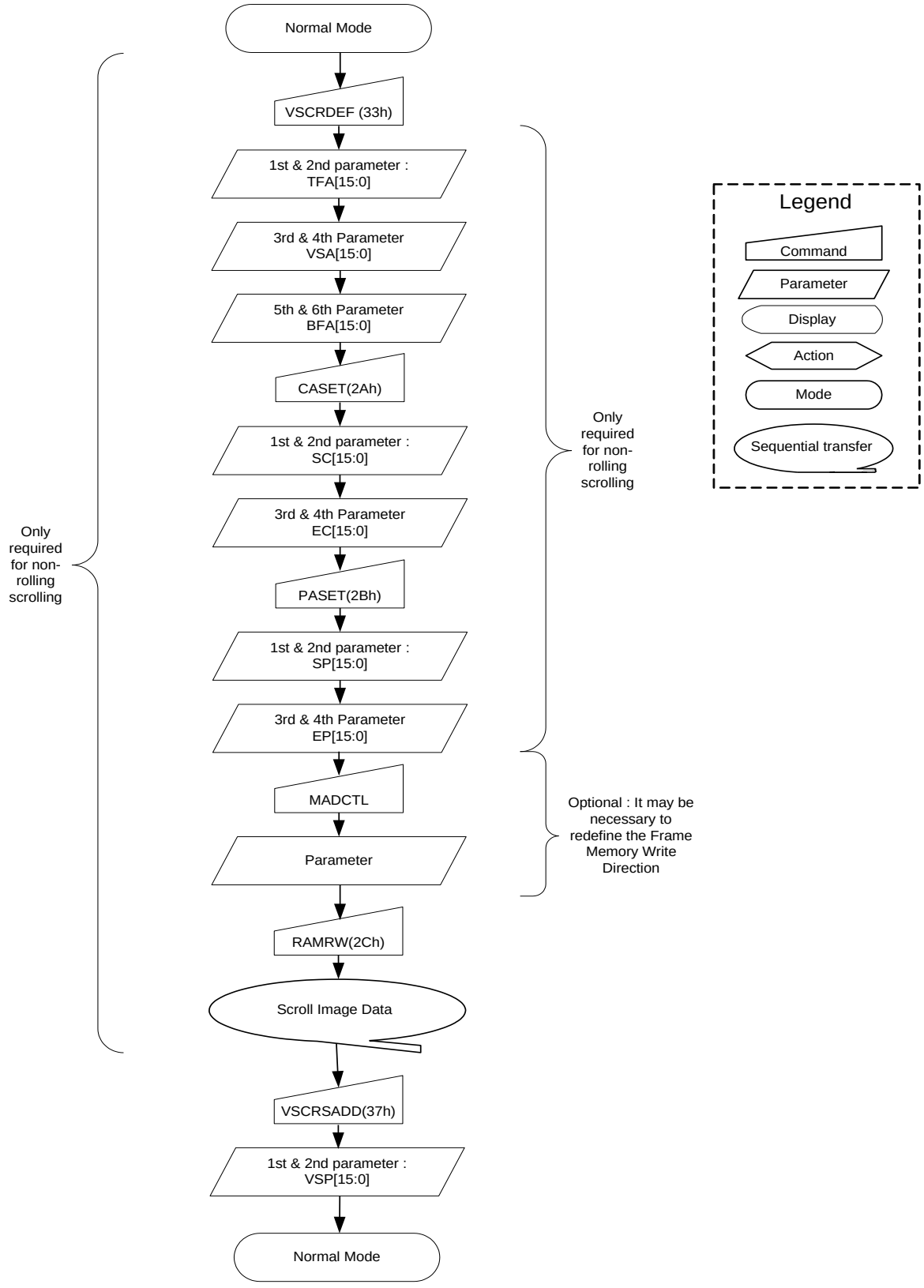
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	TFA [15:0]	VSA [15:0]	BFA [15:0]
Power On Sequence	16'h0000h	16'h0140h	16'h0000h
SW Reset	16'h0000h	16'h0140h	16'h0000h
HW Reset	16'h0000h	16'h0140h	16'h0000h

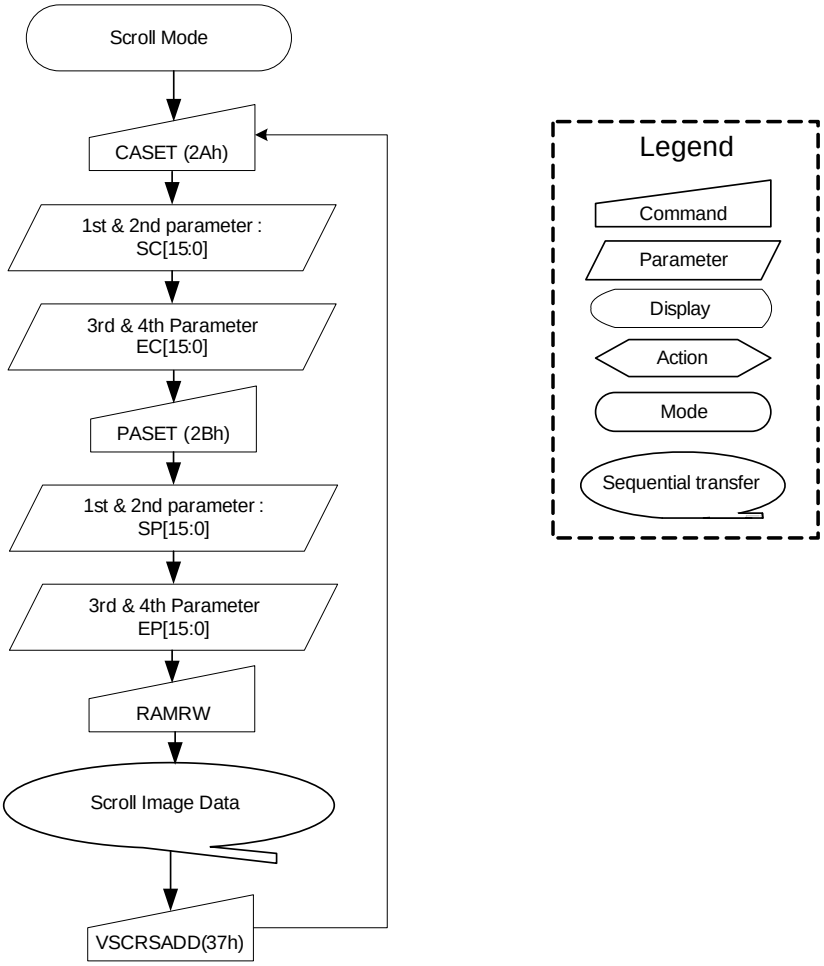
Flow Chart

1. To enter Vertical Scroll Mode :

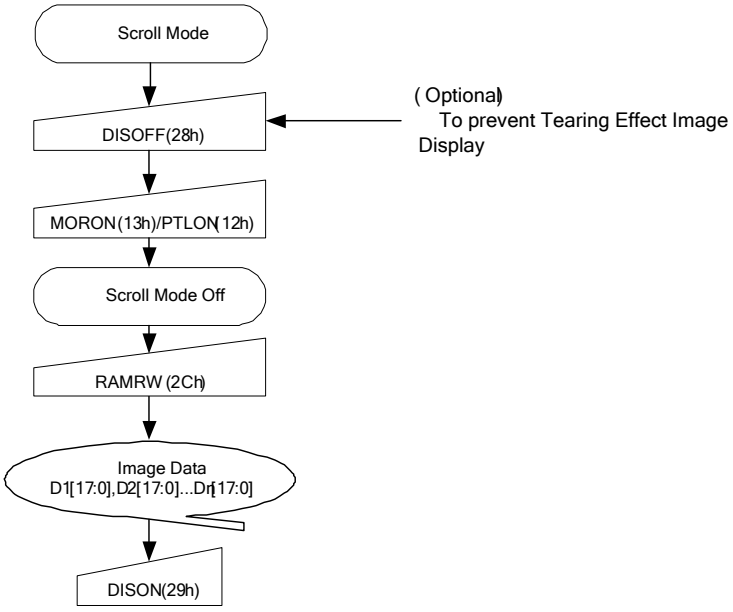


Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll :



3.To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

8.2.26. Tearing Effect Line Off (34h)

34h	TEOFF (Tearing Effect Line Off)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Parameter	No Parameter												
Description	This command is used to turn Off (Active Low) the Tearing Effect output signal from the TE signal line. X = Don't care.												
Restriction	This command has no effect when Tearing Effect output is already Off.												

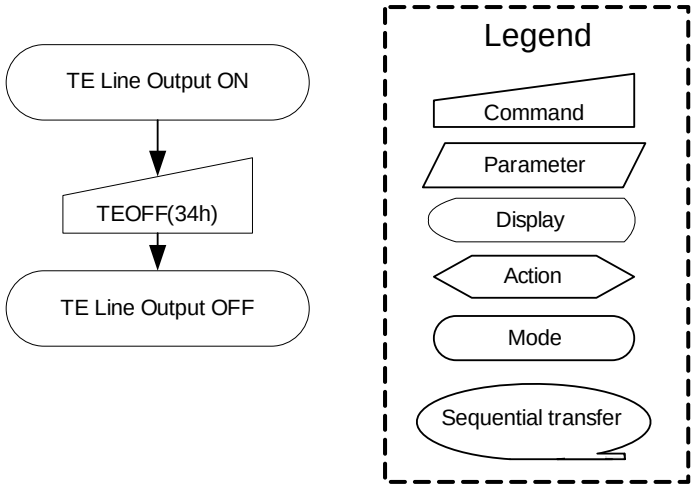
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
SW Reset	Off
HW Reset	Off

Flow Chart



8.2.27. Tearing Effect Line On (35h)

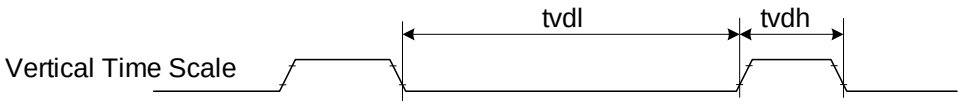
35h	TEON (Tearing Effect Line On)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
Parameter	1	1	↑	XX	0	0	0	0	0	0	0	M	00

Description

This command is used to turn on the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit D4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When **M=0**:

The Tearing Effect Output line consists of V-Blanking information only:



When **M=1**:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X = Don't care.

Restriction

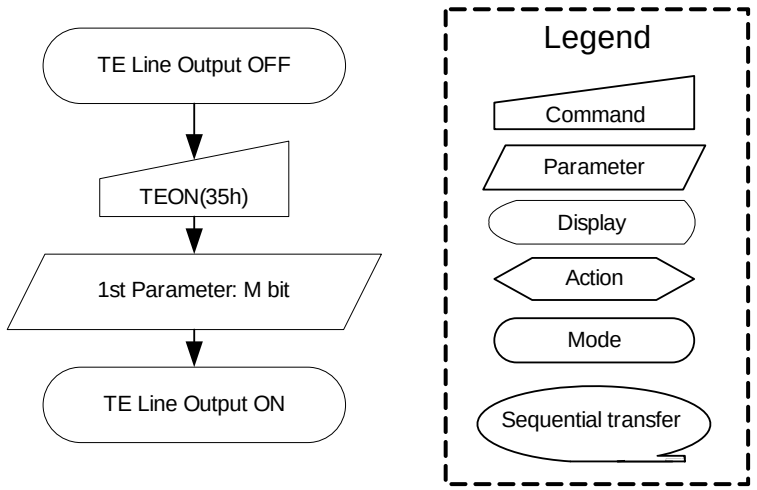
This command has no effect when Tearing Effect output is already on.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
SW Reset	Off
HW Reset	Off

Flow Chart	

8.2.28. Memory Access Control (36h)

36h	MADCTL (Memory Access Control)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00

Description

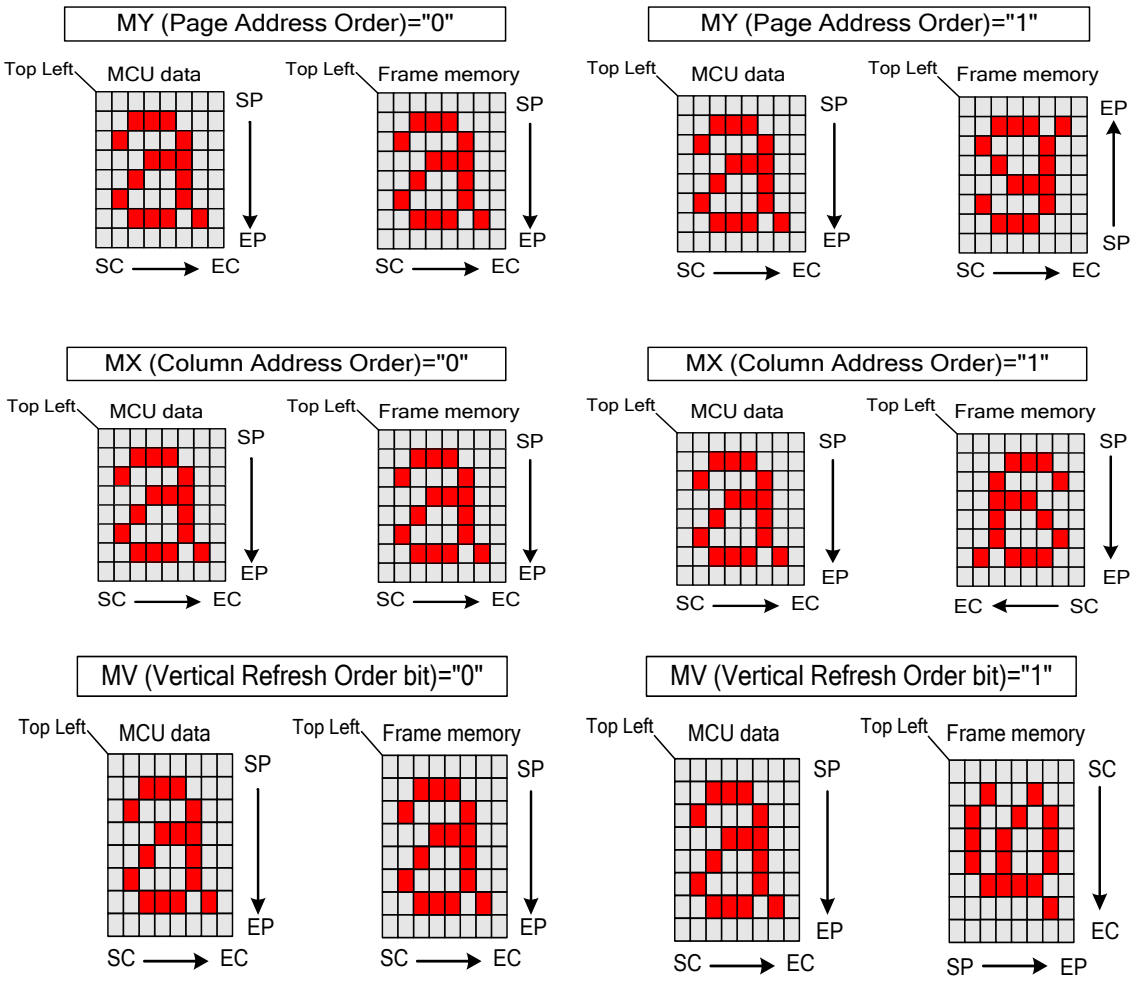
This command defines read/write scanning direction of frame memory.

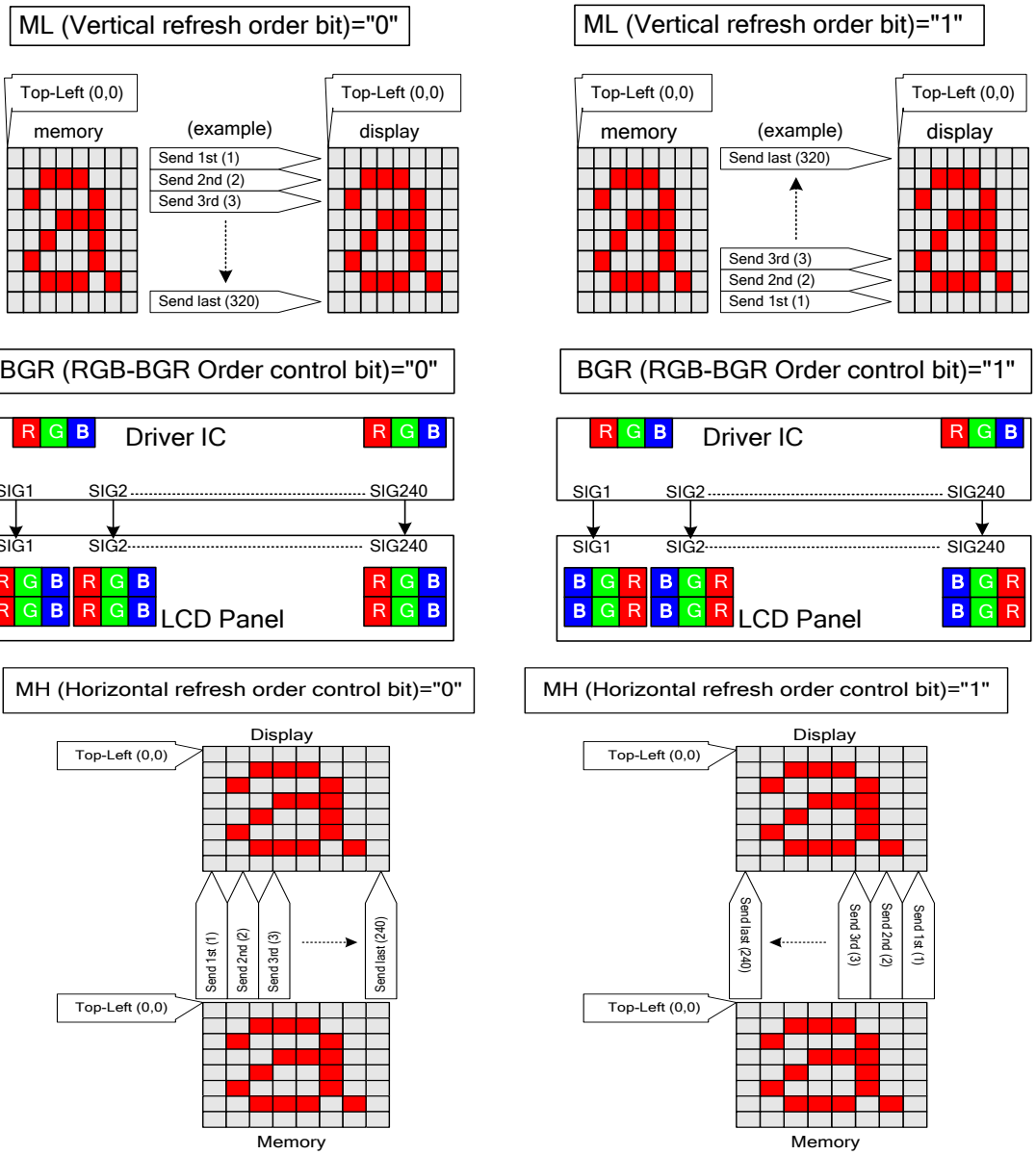
This command makes no change on the other driver status.

Bit	Name	Description
MY	Row Address Order	These 3 bits control MCU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.

X = Don't care.





Note: Top-Left (0,0) means a physical memory location.

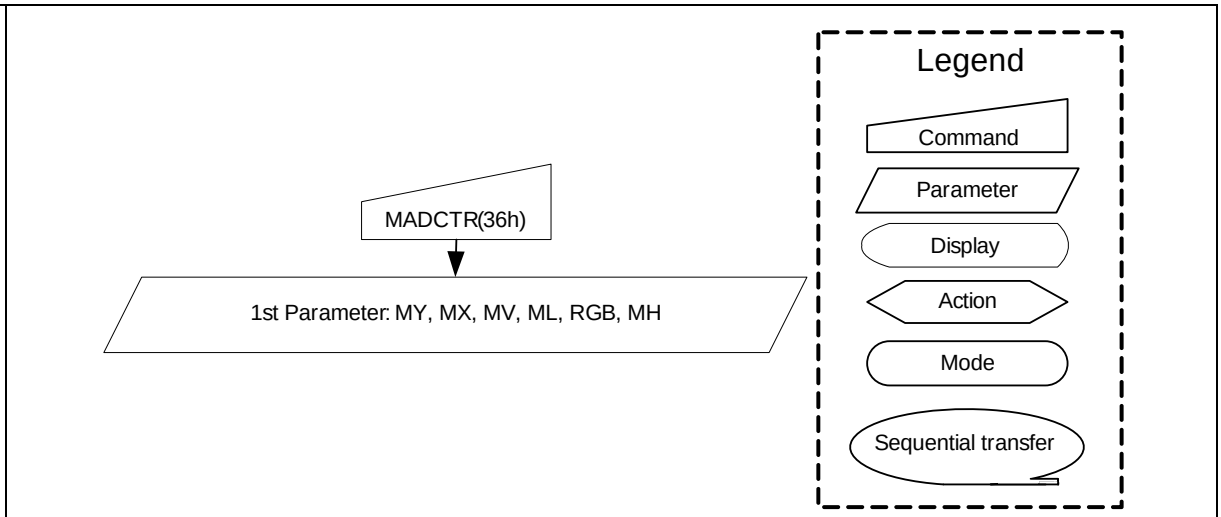
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	No change
HW Reset	8'h00h

Flow Chart	

8.2.29. Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	↑	1	XX	VSP [15:8]								00
2nd Parameter	1	↑	1	XX	VSP [7:0]								00

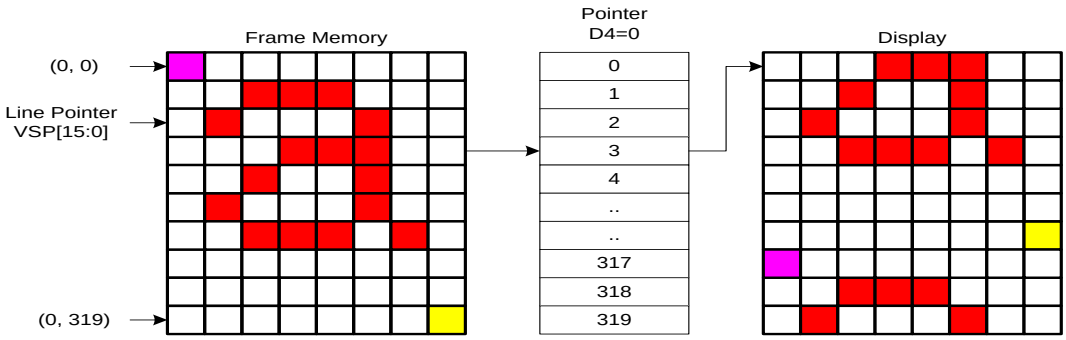
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL D4=0

Example:

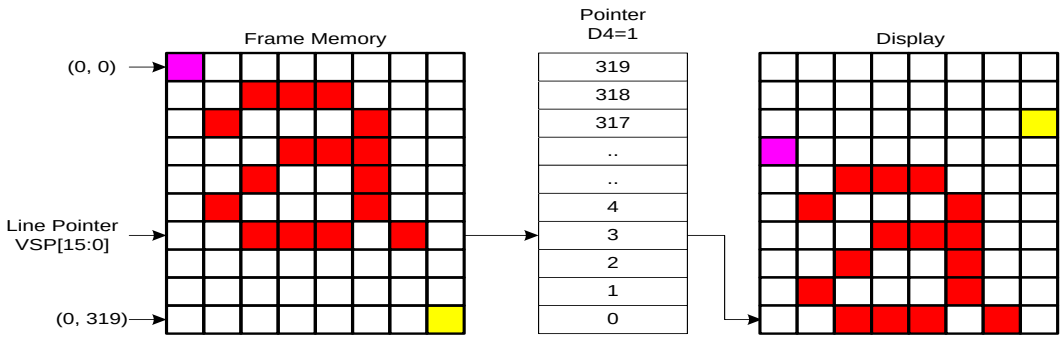
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.



When MADCTL D4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.



Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

(2) This command is ignored when the ILI9340X enters Partial mode.

X = Don't care

Restriction

<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

8.2.30. Idle Mode Off (38h)

38h	IDMOFF (Idle Mode Off)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Parameter	No Parameter												
Description	This command is used to recover from Idle Mode On. In the Idle Mode Off, LCD can display maximum 262,144 colors. X = Don't care.												
Restriction	This command has no effect when module is already in Idle Mode Off.												

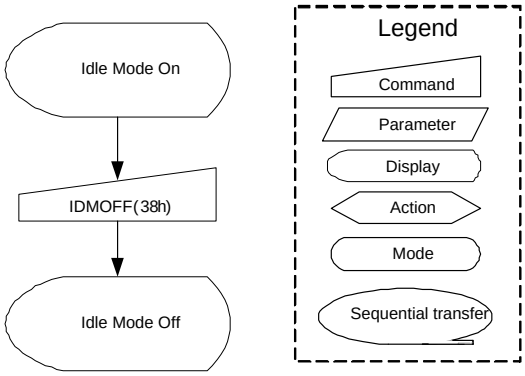
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



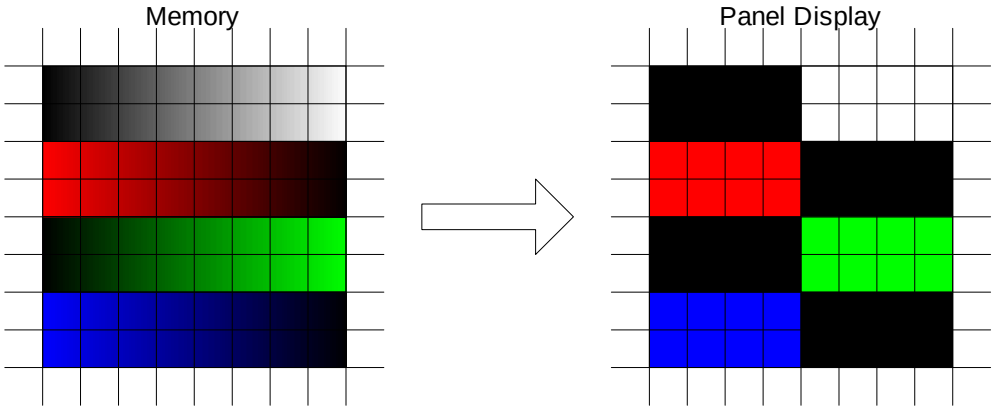
8.2.31. Idle Mode On (39h)

39h	IDMON (Idle Mode On)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Parameter	No Parameter												

Description

This command is used to enter into Idle Mode On.

In the Idle Mode On, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Memory Contents vs. Display Color			
	$R_5\ R_4\ R_3\ R_2\ R_1\ R_0$	$G_5\ G_4\ G_3\ G_2\ G_1\ G_0$	$B_5\ B_4\ B_3\ B_2\ B_1\ B_0$
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X = Don't care.

Restriction

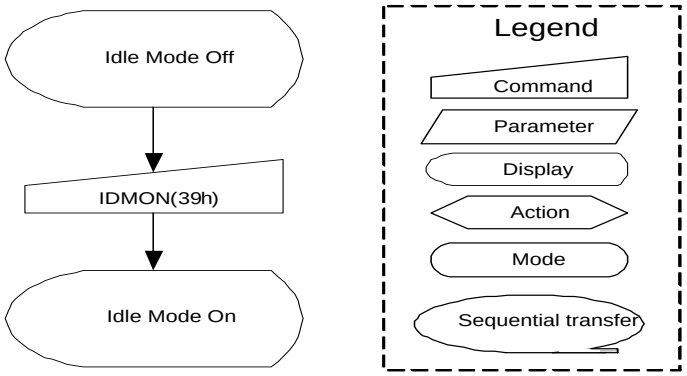
This command has no effect when module is already in Idle Mode On.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart	

8.2.32. COLMOD: Pixel Format Set (3Ah)

3Ah	PIXSET (Pixel Format Set)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
Parameter	1	1	↑	XX	0	DPI [2:0]			0	DBI [2:0]			66

Description

This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.

DPI [2:0]			RGB Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

If using RGB Interface must selection serial interface .

X = Don't care

Restriction

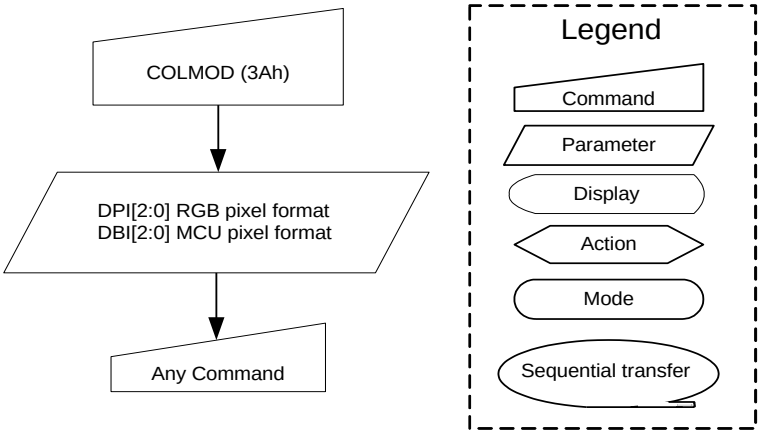
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DPI [2:0]	DBI [2:0]
Power On Sequence	3'b110	3'b110
SW Reset	No Change	No Change
HW Reset	3'b110	3'b110

Flow Chart

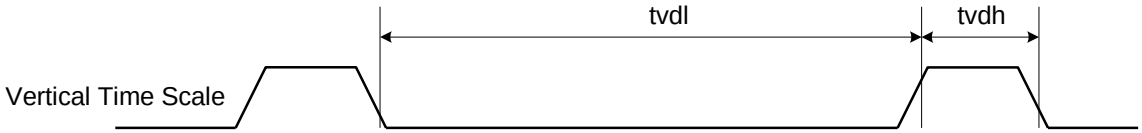


8.2.33. Set Tear Scan Line (44h)

44h	Set_Tear_Scanline												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	0	STS [8]	00
2nd Parameter	1	1	↑	XX	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	00

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line STS. The TE signal is not affected by changing Memory Access Control bit D4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.



Note that Set Tear Scan Line with STS = 0 is equivalent to Tearing Effect Line On with M = 0.

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

-

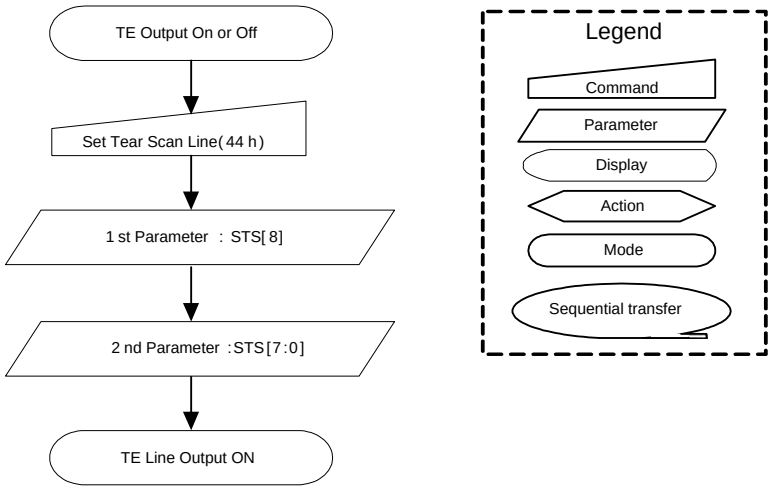
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	STS [8:0]=0000h
SW Reset	STS [8:0]=0000h
HW Reset	STS [8:0]=0000h

Flow Chart



8.2.34. Get Scan Line (45h)

45h	Get_Scanline												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	0	0	0	0	0	0	0	GTS [8]	00
3rd Parameter	1	↑	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00

Description

The display returns the current scan line, GTS, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.

When in Sleep Mode, the value returned by Get Scan Line is undefined.

Restriction

None

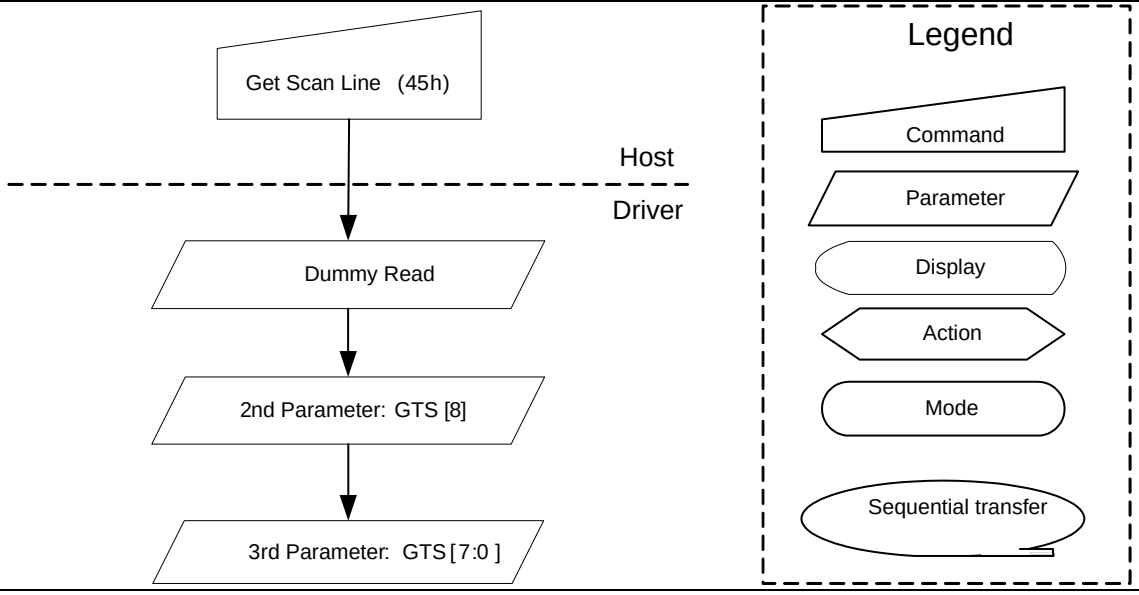
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GTS [8:0]
Power On Sequence	GTS [8:0]=0000h
SW Reset	GTS [8:0]=0000h
HW Reset	GTS [8:0]=0000h

Flow Chart



8.2.35. Write Color Enhancement Control (55h)

55h	WRCEC (Write Color Enhancement Control)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
Parameter	1	1	↑	XX	CE[3:0]				0	0	0	0	00

Description

This command is used to set parameters for image content based adaptive brightness control functionality and Color boosting functionality.

The first 4 different modes are for content adaptive image functionality, which are defined in the table below.

CE[3:0]: Color Enhancement select.

CE[3:0]				Description	CE Ratio Range
0	0	0	0	CE Off	-
1	0	0	0	CE On: Low enhancement	1.75 ~ 2.00
1	0	0	1	CE On: Medium enhancement	2.25 ~ 2.75
1	0	1	1	CE On: High enhancement	3.00 ~ 3.25

Restriction

None

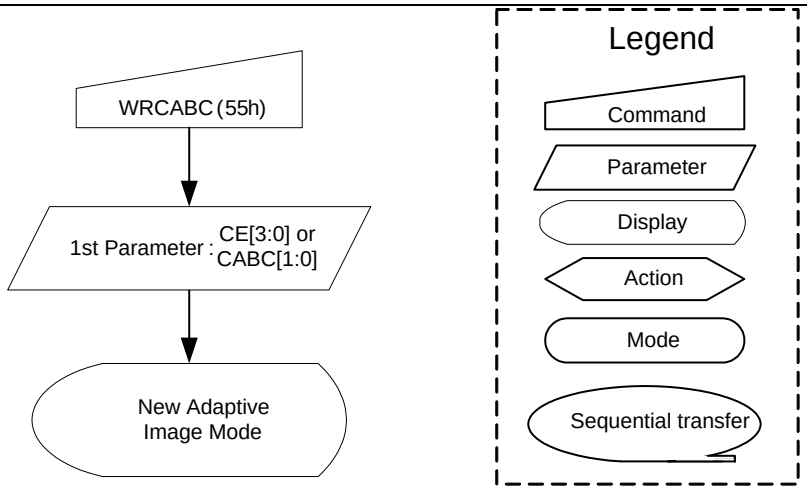
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CE[3:0]
Power On Sequence	4'b0000
SW Reset	4'b0000
HW Reset	4'b0000

Flow Chart



8.2.36. Read Color Enhancement Control (56h)

56h	RDCEC (Read Color Enhancement Control)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	CE[3:0]				0	0	0	0	00

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

It is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

CE[3:0]: Color Enhancement select.

CE[3:0]				Description	CE Ratio Range
0	0	0	0	CE Off	-
1	0	0	0	CE On: Low enhancement	1.75 ~ 2.00
1	0	0	1	CE On: Medium enhancement	2.25 ~ 2.75
1	0	1	1	CE On: High enhancement	3.00 ~ 3.25

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.

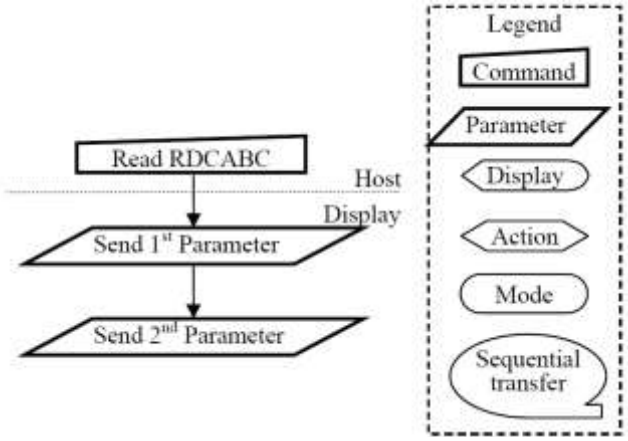
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CE[3:0]
Power On Sequence	4'b0000
SW Reset	4'b0000
HW Reset	4'b0000

Flow Chart



8.2.37. Read Automatic Brightness Control Self-Diagnostic Result (68h)

68h	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	1	0	1	0	0	0	68h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	D7	D6	0	0	0	0	0	0	00

Description

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values lo ding work properly.
D6	Functionality Detection	Invert the D6 bit if the display is functionality
D5	Not Used	'0'
D4	Not Used	'0'
D3	Not Used	'0'
D2	Not Used	'0'
D1	Not Used	'0'
D0	Not Used	'0'

Restriction

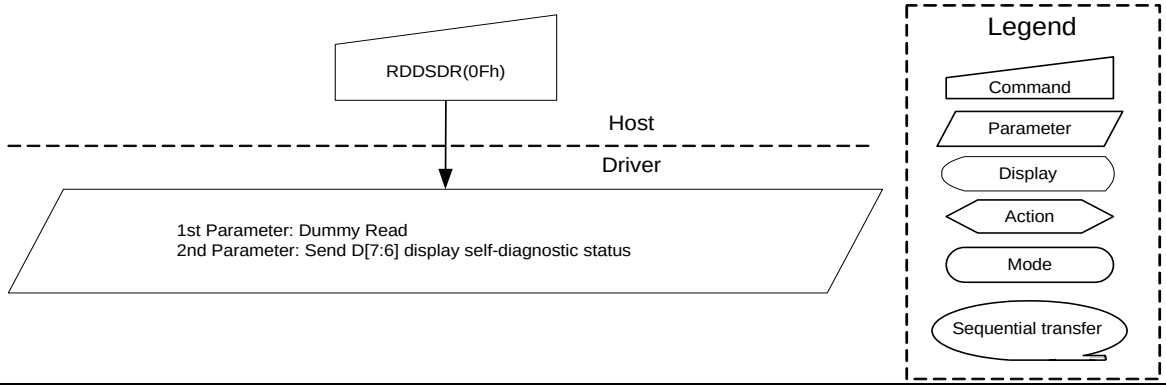
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.38. Read ID1 (DAh)

DAh	RDID1 (Read ID1)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	ID1 [7:0]								E3
Description	This read byte identifies the LCD module's manufacturer ID and it is specified by User The 1st parameter is dummy data. The 2nd parameter is LCD module's manufacturer ID. X = Don't care												
Restriction													

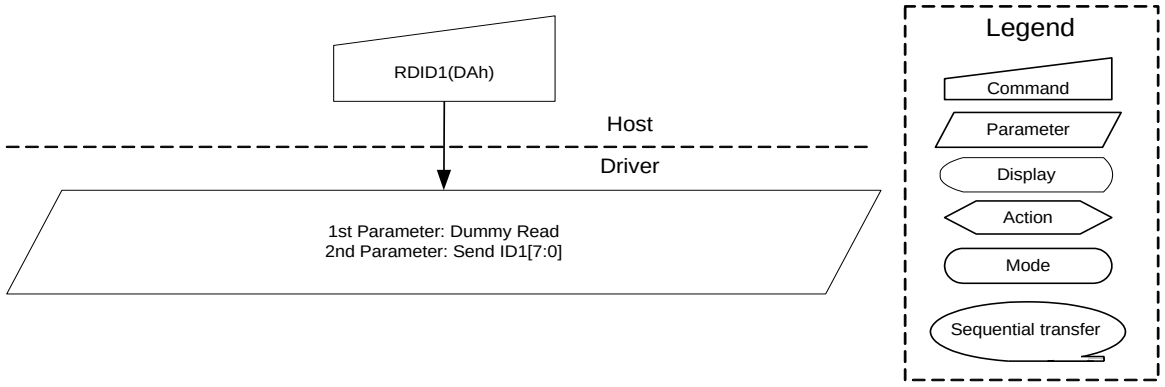
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	8'hE3h	OTP value
SW Reset	8'hE3h	OTP value
HW Reset	8'hE3h	OTP value

Flow Chart



8.2.39. Read ID2 (DBh)

DBh	RDID2 (Read ID2)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2ndParameter	1	↑	1	XX	ID2 [7:0]								00
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 00h to FFh. The ID2 can be programmed by MTP function. X = Don't care												
Restriction													

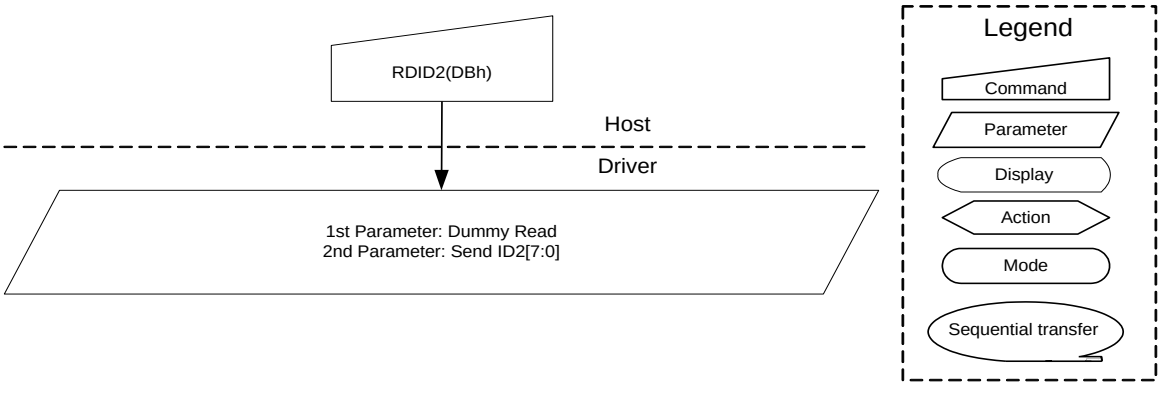
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	8'h00h	OTP value
SW Reset	8'h00h	OTP value
HW Reset	8'h00h	OTP value

Flow Chart



8.2.40. Read ID3 (DCh)

DCh	RDID3 (Read ID3)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	ID3 [7:0]								00
Description	This read byte identifies the LCD module/driver and It is specified by User. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver ID. The ID3 can be programmed by MTP function. X = Don't care												
Restriction													

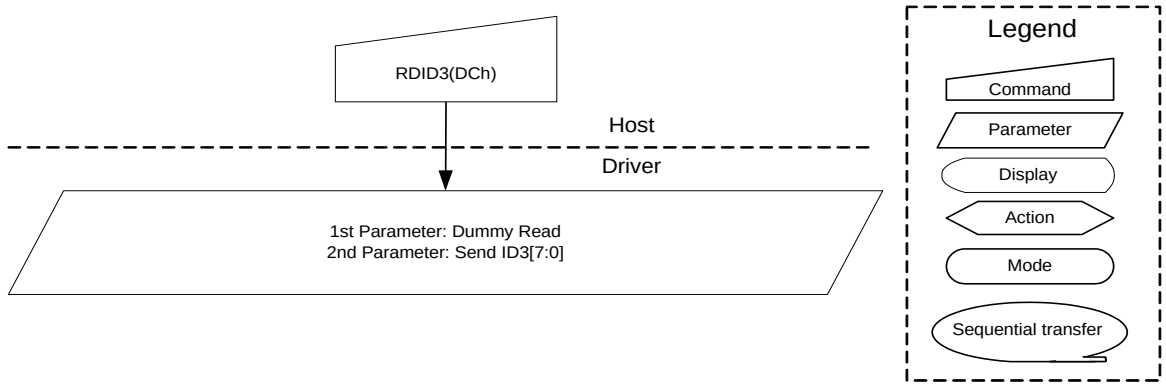
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	8'h00h	OTP value
SW Reset	8'h00h	OTP value
HW Reset	8'h00h	OTP value

Flow Chart



8.3. Description of Level 2 Command

8.3.1. RGB Interface Signal Control (B0h)

B0h	IFMODE (Interface Mode Control)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
Parameter	1	1	↑	XX	ByPass_MODE	RCM [1:0]		0	VSPL	HSPL	DPL	EPL	40

Description

Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.

EPL: ENABLE polarity ("0"= High enable for RGB interface, "1"= Low enable for RGB interface)

DPL: DOTCLK polarity set ("0"= data fetched at the rising time, "1"= data fetched at the falling time)

HSPL: HSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)

VSPL: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)

RCM [1:0]: RGB interface selection (refer to the RGB interface section).

RCM[1:0]		Description
1	0	DE Mode
1	1	SYNC Mode

ByPass_MODE: Select display data path whether Memory or Direct to Shift register when RGB Interface is used.

ByPass_MODE	Display Data Path
0	Direct to Shift Register (**default**)
1	Memory

Restriction

EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	ByPass_MODE	RCM [1:0]	VSPL	HSPL	DPL	EPL
Power On Sequence	1'b0	2'b10	1'b0	1'b0	1'b0	1'b0
SW Reset	1'b0	2'b10	1'b0	1'b0	1'b0	1'b0
HW Reset	1'b0	2'b10	1'b0	1'b0	1'b0	1'b0

8.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h	FRMCTR1 (Frame Rate Control (In Normal Mode / Full colors))												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVA [1:0]		00
2nd Parameter	1	1	↑	XX	0	0	0	RTNA [4:0]					1F

Description

Formula to calculate frame frequency:

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line} \times \text{Division ratio} \times (\text{Lines} + \text{VBP} + \text{VFP})}$$

fosc : internal oscillator frequency(Oscillator/26)

Clocks per line : RTNA setting

Division ratio : DIVA setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

RTNA [4:0]					Frame Rate (Hz)
1	0	0	0	0	inhibit
1	0	0	0	1	inhibit
1	0	0	1	0	inhibit
1	0	0	1	1	inhibit
1	0	1	0	0	inhibit
1	0	1	0	1	inhibit
1	0	1	1	0	inhibit
1	0	1	1	1	81

RTNA [4:0]					Frame Rate (Hz)
1	1	0	0	0	78
1	1	0	0	1	75
1	1	0	1	0	72
1	1	0	1	1	69
1	1	1	0	0	67
1	1	1	0	1	64
1	1	1	1	0	62
1	1	1	1	1	60

DIVA [1:0] : division ratio for internal clocks for Normal Display Mode On..

DIVA [1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2

RTNA [4:0] :It is used to set 1H (line) period for Normal Display Mode On.

RTNA [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNA [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNA [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction	EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIVA [1:0]	RTNA [4:0]
Power On Sequence	2'h00h	5'h1Fh
SW Reset	2'h00h	5'h1Fh
HW Reset	2'h00h	5'h1Fh

8.3.3. Frame Rate Control (In Idle Mode/8 colors) (B2h)

B2h	FRMCTR2 (Frame Rate Control (In Idle Mode / 8 colors))												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVB [1:0]		02
2ndParameter	1	1	↑	XX	0	0	0	RTNB [4:0]					1F

Description

Formula to calculate frame frequency

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line} \times \text{Division ratio} \times (\text{Lines} + \text{VBP} + \text{VFP})}$$

fosc : internal oscillator frequency(Oscillator/26)

Clocks per line : RTNB setting

Division ratio : DIVB setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

RTNB [4:0]					Frame Rate (Hz)
1	0	0	0	0	inhibit
1	0	0	0	1	inhibit
1	0	0	1	0	inhibit
1	0	0	1	1	inhibit
1	0	1	0	0	inhibit
1	0	1	0	1	inhibit
1	0	1	1	0	inhibit
1	0	1	1	1	20

RTNB [4:0]					Frame Rate (Hz)
1	1	0	0	0	20
1	1	0	0	1	19
1	1	0	1	0	18
1	1	0	1	1	17
1	1	1	0	0	17
1	1	1	0	1	16
1	1	1	1	0	16
1	1	1	1	1	15

DIVB [1:0]: division ratio for internal clocks for Idle Mode On.

DIVB [1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4

RTNB [4:0]: It is used to set 1H (line) period for Idle Mode On.

RTNB [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNB [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNB [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction	EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIVB [1:0]	RTNB [4:0]
Power On Sequence	2'h02h	5'h1Fh
SW Reset	2'h02h	5'h1Fh
HW Reset	2'h02h	5'h1Fh

8.3.4. Frame Rate control (In Partial Mode/Full Colors) (B3h)

B3h	FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors))												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVC [1:0]		00
2ndParameter	1	1	↑	XX	0	0	0	RTNC [4:0]					1F

Description

Formula to calculate frame frequency:

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line} \times \text{Division ratio} \times (\text{Lines} + \text{VBP} + \text{VFP})}$$

fosc : internal oscillator frequency(Oscillator/26)

Clocks per line : RTNC setting

Division ratio : DIVC setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

RTNC [4:0]					Frame Rate (Hz)
1	0	0	0	0	inhibit
1	0	0	0	1	inhibit
1	0	0	1	0	inhibit
1	0	0	1	1	inhibit
1	0	1	0	0	inhibit
1	0	1	0	1	inhibit
1	0	1	1	0	inhibit
1	0	1	1	1	81

RTNC [4:0]					Frame Rate (Hz)
1	1	0	0	0	78
1	1	0	0	1	75
1	1	0	1	0	72
1	1	0	1	1	69
1	1	1	0	0	67
1	1	1	0	1	64
1	1	1	1	0	62
1	1	1	1	1	60

DIVC [1:0]: division ratio for internal clocks for Partial Mode On.

DIVC [1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2

RTNC [4:0]: It is used to set 1H (line) period for Partial Mode On.

RTNC [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNC [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNC [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction	EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIVC [1:0]	RTNC [4:0]
Power On Sequence	2'h00h	5'h1Fh
SW Reset	2'h00h	5'h1Fh
HW Reset	2'h00h	5'h1Fh

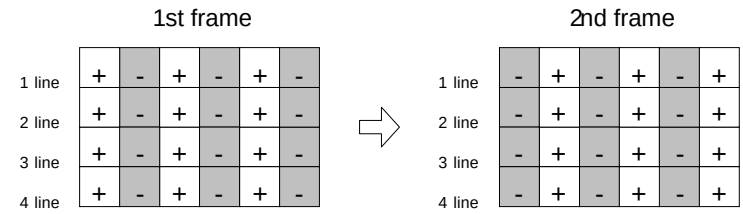
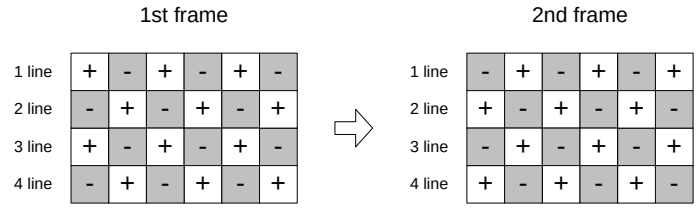
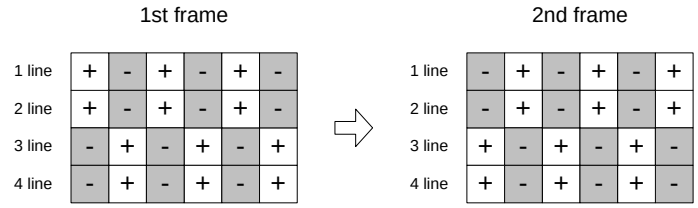
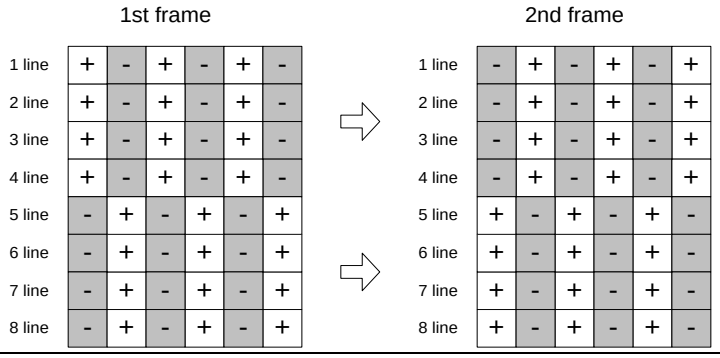
8.3.5. Display Inversion Control (B4h)

B4h	INVTR (Display Inversion Control)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
1st Parameter	1	1	↑	XX	DINVA[1:0]		0	0	0	0	0	0	80
2ndParameter	1	1	↑	XX	DINVB[1:0]		0	0	0	0	0	0	00

Description

DINVA[1:0] : Set the inversion mode in normal mode.

DINVB[1:0] : Set the inversion mode in Idle mode.

DINV [1:0]	Inversion mode	
2'b00	Column inversion	
2'b01	1-dot inversion	
2'b10	2-dot inversion	
2'b11	4-dot inversion	

Restriction	EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DINVA[1:0]	DINVB[1:0]
Power On Sequence	2'b10	2'b00
SW Reset	2'b10	2'b00
H/W Reset	2'b10	2'b00

8.3.6. Blanking Porch Control (B5h)

B5h	PRCTR (Blanking Porch)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1st Parameter	1	1	↑	XX	VFP [7:0]								02
2nd Parameter	1	1	↑	XX	VBP [7:0]								02
3rd Parameter	1	1	↑	XX	0	0	0	HFP [4:0]					0A
4th Parameter	1	1	↑	XX	HBP [7:0]								14

Description

VFP [7:0] / VBP [7:0]: The VFP [7:0] and VBP [7:0] bits specify the line number of vertical front and back porch period respectively.

VFP [7:0] VBP [7:0]	Number of front/back porch (unit:HSYNC)	VFP [7:0] VBP [7:0]	Number of front/back porch (unit:HSYNC)
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
0000110	6	1000110	70
0000111	7	1000111	71
0001000	8	1001000	72
0001001	9	1001001	73
0001010	10	1001010	74
0001011	11	1001011	75
0001100	12	1001100	76
0001101	13	1001101	77
: :	: :	: :	: :
0111101	61	1111101	125
0111110	62	1111110	126
0111111	63	1111111	127

Note: VFP + VBP ≦ 254 HSYNC signals

HFP [4:0] / HBP [7:0]: The HFP [4:0] and HBP [7:0] bits specify the line number of horizontal front and back porch period respectively.

HFP [4:0] HBP [7:0]	Number of the front/back porch (unit:DOTCLK)
00000	Setting prohibited
00001	Setting prohibited
00010	2
00011	3
00100	4
00101	5
00110	6
00111	7
01000	8
01001	9
01010	10
01011	11
01100	12
01101	13
01110	14
01111	15

HFP [4:0] HBP [7:0]	Number of the front/back porch (unit:DOTCLK)
10000	16
10001	17
10010	18
10011	19
10100	20
10101	21
10110	22
10111	23
11000	24
11001	25
11010	26
11011	27
11100	28
11101	29
:	:
11111111	255

**HBP need to setting more than 58 clock and less than 200 clocks in By-pass mode. There is 8 bit setting in HBP register.*

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>VFP [7:0]</th><th>VBP [7:0]</th><th>HFP [4:0]</th><th>HBP [7:0]</th></tr>
<tr><td>Power On Sequence</td><td>8’h02h</td><td>8’h02h</td><td>5’h0Ah</td><td>8’h14h</td></tr>
<tr><td>SW Reset</td><td>8’h02h</td><td>8’h02h</td><td>5’h0Ah</td><td>8’h14h</td></tr>
<tr><td>HW Reset</td><td>8’h02h</td><td>8’h02h</td><td>5’h0Ah</td><td>8’h14h</td></tr>
</table>
</td></tr>
</table>

8.3.7. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
1st Parameter	1	1	↑	XX	0	0	0	0	PTG [1:0]		PT [1:0]		0A
2nd Parameter	1	1	↑	XX	1	GS	SS	SM	ISC [3:0]				02
3rd Parameter	1	1	↑	XX	0	0	NL [5:0]						27
4th Parameter	1	1	↑	XX	0	0	PCDIV [5:0]						04

Description

PTG [1:0]: Set the scan mode in non-display area.

PTG1	TG0	Gate outputs in non-display area	Source outputs in non-display area
0	0	Normal scan	Set with the PT [1:0] bits
0	1	Setting prohibited	---
1	0	Interval scan	Set with the PT [1:0] bits
1	1	Setting prohibited	---

PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

PT [1:0]		Source output on non-display area
0	0	V63
0	1	V0
1	0	AGND
1	1	Hi-Z

SS: This bit controls MPU to memory write/read direction by column address order.

SS	Source Output Scan Direction
0	S1 → S720
1	S720 → S1

ISC [3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] ="10" to select interval scan.

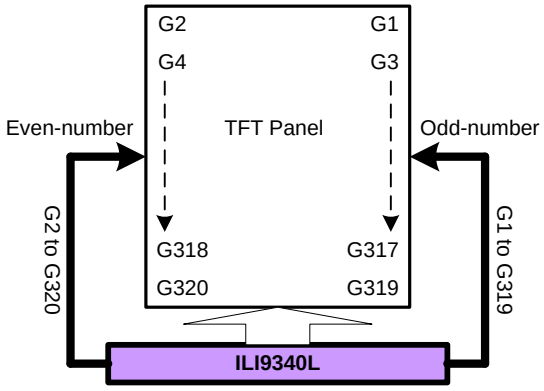
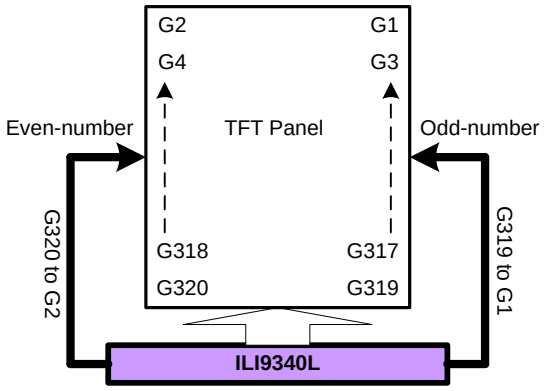
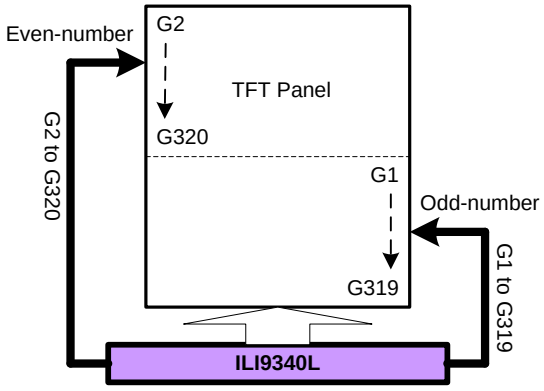
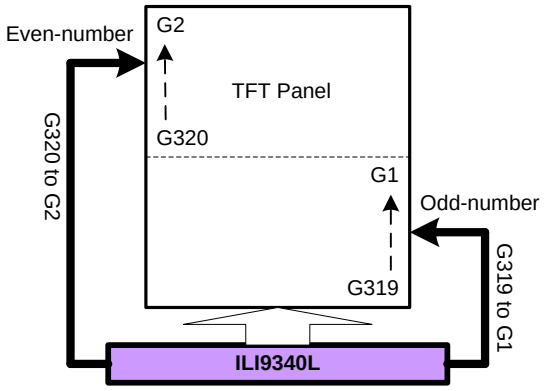
Then scan cycle is set as odd number from 1~31 frame periods. The polarity is inverted every scan cycle.

ISC [3:0]	Scan Cycle	f_{FLM} = 60Hz
0000	1 frame	17ms
0001	3 frames	51ms
0010	5 frames	85ms
0011	7 frames	119ms
0100	9 frames	153ms
0101	11 frames	187ms
0110	13 frames	221ms
0111	15 frames	255ms
1000	17 frames	289ms
1001	19 frames	323ms
1010	21 frames	357ms
1011	23 frames	391ms
1100	25 frames	425ms
1101	27 frames	459ms
1110	29 frames	493ms
1111	31 frames	527ms

GS: Sets the direction of scan by the gate driver in the range determined by NL [5:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction
0	G1 → G320
1	G320 → G1

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ …… ….→G317→G318→G319→G320
0	1		G320→G319->G318→G317→…… …. →G4→G3→G2→G1
1	0		G1→G3→……...→G317→G319→ G2→G4→……→G318→G320
1	1		G320→G318→……...→G4→G2→ G319→G317→……→G3→G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL [5:0]						LCD Drive Line
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines
0	0	0	1	1	0	56 lines
0	0	0	1	1	1	64 lines
0	0	1	0	0	0	72 lines
0	0	1	0	0	1	80 lines
0	0	1	0	1	0	88 lines
0	0	1	0	1	1	96 lines
0	0	1	1	0	0	104 lines
0	0	1	1	0	1	112 lines
0	0	1	1	1	0	120 lines
0	0	1	1	1	1	128 lines
0	1	0	0	0	0	136 lines
0	1	0	0	0	1	144 lines
0	1	0	0	1	0	152 lines
0	1	0	0	1	1	160 lines
0	1	0	1	0	0	168 lines

NL [5:0]						LCD Driver Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines
0	1	1	0	1	1	224 lines
0	1	1	1	0	0	232 lines
0	1	1	1	0	1	240 lines
0	1	1	1	1	0	248 lines
0	1	1	1	1	1	256 lines
1	0	0	0	0	0	264 lines
1	0	0	0	0	1	272 lines
1	0	0	0	1	0	280 lines
1	0	0	0	1	1	288 lines
1	0	0	1	0	0	296 lines
1	0	0	1	0	1	304 lines
1	0	0	1	1	0	312 lines
1	0	0	1	1	1	320 lines
Others						Setting inhibited

PCDIV [5:0]: Number of DOTCLK during internal clock PCLKD's high / low period. In units of 1 clock. PCDIV specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 615KHz is the smallest. Set PCDIV follow the restriction.

(Number of PCLK in 1H) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV.

$$\text{external fosc} = \frac{\text{DOTCLK}}{2 \times (\text{PCDIV} + 1)}$$

Restriction

EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value							
	PTG [1:0]	PT [1:0]	GS	SS	SM	ISC [3:0]	NL [5:0]	PCDIV [5:0]
Power On Sequence	2'b10	2'b10	1'b0	1'b0	1'b0	4'b0010	6'h27	6'h04
SW Reset	2'b10	2'b10	1'b0	1'b0	1'b0	4'b0010	6'h27	6'h04
HW Reset	2'b10	2'b10	1'b0	1'b0	1'b0	4'b0010	6'h27	6'h04

8.3.8. Power Control (BAh)

BBh	PWCTRL (VCOM/VRH/VDV Control)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	1	1	BAh
1st Parameter	1	1	↑	XX	1	VCOM[6:0]							30
2nd Parameter	1	1	↑	XX	1	0	VRH[5:0]						0B
3rd Parameter	1	1	↑	XX	1	0	VDV[5:0]						20

Description

VCOM [6:0]

VCOM [6:0]	VCOM (V)	VCOM [6:0]	VCOM (V)	VCOM [6:0]	VCOM (V)	VCOM [6 0]	VCOM (V)	VCOM [6:0]	VCOM (V)	VCOM [6:0]	VCOM (V)	VCOM [6:0]	VCOM (V)	VCOM [6:0]	VCOM (V)
00h	0.3	10h	0.5	20h	0.7	30h	0.9	40h	1.1	50h	1.3	60h	1.5	70h	1.7
01h	0.3125	11h	0.5125	21h	0.7125	31h	0.9125	41h	1.1125	51h	1.3125	61h	1.5125	71h	1.7125
02h	0.325	12h	0.525	22h	0.725	32h	0.925	42h	1.125	52h	1.325	62h	1.525	72h	1.725
03h	0.3375	13h	0.5375	23h	0.7375	33h	0.9375	43h	1.1375	53h	1.3375	63h	1.5375	73h	1.7375
04h	0.35	14h	0.55	24h	0.75	34h	0.95	44h	1.15	54h	1.35	64h	1.55	74h	1.75
05h	0.3625	15h	0.5625	25h	0.7625	35h	0.9625	45h	1.1625	55h	1.3625	65h	1.5625	75h	1.7625
06h	0.375	16h	0.575	26h	0.775	36h	0.975	46h	1.175	56h	1.375	66h	1.575	76h	1.775
07h	0.3875	17h	0.5875	27h	0.7875	37h	0.9875	47h	1.1875	57h	1.3875	67h	1.5875	77h	1.7875
08h	0.4	18h	0.6	28h	0.8	38h	1	48h	1.2	58h	1.4	68h	1.6	78h	1.8
09h	0.4125	19h	0.6125	29h	0.8125	39h	1.0125	49h	1.2125	59h	1.4125	69h	1.6125	79h	1.8125
0Ah	0.425	1Ah	0.625	2Ah	0.825	3Ah	1.025	4Ah	1.225	5Ah	1.425	6Ah	1.625	7Ah	1.825
0Bh	0.4375	1Bh	0.6375	2Bh	0.8375	3Bh	1.0375	4Bh	1.2375	5Bh	1.4375	6Bh	1.6375	7Bh	1.8375
0Ch	0.45	1Ch	0.65	2Ch	0.85	3Ch	1.05	4Ch	1.25	5Ch	1.45	6Ch	1.65	7Ch	1.85
0Dh	0.4625	1Dh	0.6625	2Dh	0.8625	3Dh	1.0625	4Dh	1.2625	5Dh	1.4625	6Dh	1.6625	7Dh	1.8625
0Eh	0.475	1Eh	0.675	2Eh	0.875	3Eh	1.075	4Eh	1.275	5Eh	1.475	6Eh	1.675	7Eh	1.875
0Fh	0.4875	1Fh	0.6875	2Fh	0.8875	3Fh	1.0875	4Fh	1.2875	5Fh	1.4875	6Fh	1.6875	7Fh	1.8875

VDV [5:0]

VDV[5:0]	VDV(V)	VDV[5:0]	VDV(V)	VDV[5:0]	VDV(V)	VDV[5:0]	VDV(V)
00h	-0.8	10h	-0.4	20h	0	30h	0.4
01h	-0.775	11h	-0.375	21h	0.025	31h	0.425
02h	-0.75	12h	-0.35	22h	0.05	32h	0.45
03h	-0.725	13h	-0.325	23h	0.075	33h	0.475
04h	-0.7	14h	-0.3	24h	0.1	34h	0.5
05h	-0.675	15h	-0.275	25h	0.125	35h	0.525
06h	-0.65	16h	-0.25	26h	0.15	36h	0.55
07h	-0.625	17h	-0.225	27h	0.175	37h	0.575
08h	-0.6	18h	-0.2	28h	0.2	38h	0.6
09h	-0.575	19h	-0.175	29h	0.225	39h	0.625

0Ah	-0.55	1Ah	-0.15	2Ah	0.25	3Ah	0.65
0Bh	-0.525	1Bh	-0.125	2Bh	0.275	3Bh	0.675
0Ch	-0.5	1Ch	-0.1	2Ch	0.3	3Ch	0.7
0Dh	-0.475	1Dh	-0.075	2Dh	0.325	3Dh	0.725
0Eh	-0.45	1Eh	-0.05	2Eh	0.35	3Eh	0.75
0Fh	-0.425	1Fh	-0.025	2Fh	0.375	3Fh	0.775

VRH [5:0] Setting for VREG1OUT

VRH[5:0]	VREG1OUT(V)	VRH[5:0]	VREG1OUT (V)
00h	3.55+(VCOM+0.5VDV)	15h	4.6+(VCOM+0.5VDV)
01h	3.6+(VCOM+0.5VDV)	1 h	4.65+(VCOM+0.5VDV)
02h	3.65+(VCOM+0.5VDV)	17h	4.7+(VCOM+0.5VDV)
03h	3.7+(VCOM+0.5VDV)	18h	4.75+(VCOM+0.5VDV)
04h	3.75+(VCOM+0.5VDV)	19h	4.8+(VCOM+0.5VDV)
05h	3.8+(VCOM+0.5VDV)	1Ah	4.85+(VCOM+0.5VDV)
06h	3.85+(VCOM+0.5VDV)	1Bh	4.9+(VCOM+0.5VDV)
07h	3.9+(VCOM+0.5VDV)	1Ch	4.95+(VCOM+0.5VDV)
08h	3.95+(VCOM+0.5VDV)	1Dh	5+(VCOM+0.5VDV)
09h	4+(VCOM+0.5VDV)	1Eh	5.05+(VCOM+0.5VDV)
0Ah	4.05+(VCOM+0.5VDV)	1Fh	5.1+(VCOM+0.5VDV)
0Bh	4.1+(VCOM+0.5VDV)	20h	5.15+(VCOM+0.5VDV)
0Ch	4.15+(VCOM+0.5VDV)	21h	5.2+(VCOM+0.5VDV)
0Dh	4.2+(VCOM+0.5VDV)	22h	5.25+(VCOM+0.5VDV)
0Eh	4.25+(VCOM+0.5VDV)	23h	5.3+(VCOM+0.5VDV)
0Fh	4.3+(VCOM+0.5VDV)	24h	5.35+(VCOM+0.5VDV)
10h	4.35+(VCOM+0.5VDV)	25h	5.4+(VCOM+0.5VDV)
11h	4.4+(VCOM+0.5VDV)	26h	5.45+(VCOM+0.5VDV)
12h	4.45+(VCOM+0.5VDV)	27h	5.5+(VCOM+0.5VDV)
13h	4.5+(VCOM+0.5VDV)	28h~3Fh	Reserved
14h	4.55+(VCOM+0.5VDV)	--	--

VRH [5:0] Setting for VREG2OUT

VRH[5:0]	VREG2OUT (V)	VRH[5:0]	VREG2OUT (V)
00h	-3.55+(VCOM-0.5VDV)	15h	-4.6+(VCOM-0.5VDV)
01h	-3.6+(VCOM-0.5VDV)	16h	-4.65+(VCOM-0.5VDV)
02h	-3.65+(VCOM-0.5VDV)	17h	-4.7+(VCOM-0.5VDV)
03h	-3.7+(VCOM-0.5VDV)	18h	-4.75+(VCOM-0.5VDV)
04h	-3.75+(VCOM-0.5VDV)	19h	-4.8+(VCOM-0.5VDV)
05h	-3.8+(VCOM-0.5VDV)	1Ah	-4.85+(VCOM-0.5VDV)
06h	-3.85+(VCOM-0.5VDV)	1Bh	-4.9+(VCOM-0.5VDV)
07h	-3.9+(VCOM-0.5VDV)	1Ch	-4.95+(VCOM-0.5VDV)
08h	-3.95+(VCOM-0.5VDV)	1Dh	-5+(VCOM-0.5VDV)
09h	-4+(VCOM-0.5VDV)	1Eh	-5.05+(VCOM-0.5VDV)
0Ah	-4.05+(VCOM-0.5VDV)	1Fh	-5.1+(VCOM-0.5VDV)
0Bh	-4.1+(VCOM-0.5VDV)	20h	-5.15+(VCOM-0.5VDV)
0Ch	-4.15+(VCOM-0.5VDV)	21h	-5.2+(VCOM-0.5VDV)
0Dh	-4.2+(VCOM-0.5VDV)	22h	-5.25+(VCOM-0.5VDV)
0Eh	-4.25+(VCOM-0.5VDV)	23h	-5.3+(VCOM-0.5VDV)
0Fh	-4.3+(VCOM-0.5VDV)	24h	-5.35+(VCOM-0.5VDV)
10h	-4.35+(VCOM-0.5VDV)	25h	-5.4+(VCOM-0.5VDV)
11h	-4.4+(VCOM-0.5VDV)	26h	-5.45+(VCOM-0.5VDV)
12h	-4.45+(VCOM-0.5VDV)	27h	-5.5+(VCOM-0.5VDV)
13h	-4.5+(VCOM-0.5VDV)	28h~3Fh	Reserved
14h	-4.55+(VCOM-0.5VDV)	--	--

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	VCOM[6:0]	VRH[5:0]	VDV[5:0]
Power On Sequence	7'h30	5'h0B	5'h20
S/W Reset	7'h30	5'h0B	5'h20
HW Reset	7'h30	5'h0B	5'h20

8.3.9. Power Control 2 (BBh)

BBh	Power Control 2												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	1	1	BBh
1st Parameter	1	1	↑	XX	0	VGH_SEL[2:0]			0	VGL_SEL[2:0]			34
2nd Parameter	1	1	↑	XX	0	DDVDH_SEL[2:0]			0	DDVDL_SEL[2:0]			33

Description

VGH Voltage:

VGH_SEL[2:0]	VGH (Voltage)
000	12.2
001	12.6
010	13.0
011	13.4
100	13.8
101	14.2
110	14.6
11	15.0

VGL Voltage:

VGL_SEL [2:0]	VGL (Voltage)
000	-7.0
001	-7.8
010	-8.6
011	-9.4
100	-10.2
101	-11.0
110	-11.8
111	-12.6

DDVDH Voltage:

DDVDH_SEL [2:0]	DDVDH (Voltage)
000	6.1
001	6.2
010	6.3
011	6.4
100	6.5
101	6.6
110	6.7
111	6.8

DDVDL Voltage:

DDVDL_SEL [2:0]	DDVDL (Voltage)
000	-4.3
001	-4.4
010	-4.5
011	-4.6
100	-4.7
101	-4.8
110	-4.9
111	-5.0

Restriction: EXTC should be high to enable this command

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value			
	VGH_SEL	VGL_SEL	DDVDH_SEL	DDVDL_SEL
Power On Sequence	3'h3	3'h4	3'h3	3'h3
SW Reset	3'h3	3'h4	3'h3	3'h3
HW Reset	3'h3	3'h4	3'h3	3'h3

8.3.10. 2 Lane SPI Selection (C6h)

C6h	2 Lane SPI Mode Selection												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	1	0	C6h
1st Parameter	1	1	↑	XX	0	0	0	0	0	TYPE	SPI2LANE	0	00
Description	The command turns on the SPI 2 Lane mode when writes pixel data to frame memory, **SPI2LANE:** When this bit is high level, the mode enables. **TYPE:** This bit sets the pixel format . When type = 0: One pixel display data is sent by 1 time transfers. When type = 1: Two pixels display data is sent by 3 time transfers.												
Restriction	EXTC should be high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TYPE	SPI2LANE
Power On Sequence	1'b0	1'b0
SW Reset	1'b0	1'b0
HW Reset	1'b0	1'b0

8.3.11. Level 3 Command Eable Control (CFh)

CFh	L3CMDEC (Level 3 Command Eable Control)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	1	1	1	CFh
1st Parameter	1	1	↑	XX	0	0	0	0	0	1	0	0	04
2nd Parameter	1	1	↑	XX	0	0	0	0	0	0	0	EXTC	00
Description	**EXTC**=0 Disable all command function which need EXTC **EXTC**=1 Enable all command function which need EXTC												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	EXTC
Power On Sequence	1'b0
SW Reset	1'b0
HW Reset	1'b0

8.3.12. Read ID4 (D5h)

D5h	RDID4 (Read ID4)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	1	0	1	D5h
1st Parameter	1	↑	1	XX	0	0	0	0	0	0	0	0	00h
2ndParameter	1	↑	1	XX	1	0	0	1	0	0	1	1	93h
3rdParameter	1	↑	1	XX	0	1	0	0	0	0	0	0	40h
Description	Read IC device code. The 3 parameters mean the IC model name.												
Restriction	EXTC should be high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24'h009340h
SW Reset	24'h009340h
HW Reset	24'h009340h

8.3.13. Entry Mode Set (D6h)

D6h	ETMOD (Entry Mode Set)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	1	1	0	D6h
Parameter	1	1	↑	XX	0	0	0	0	0	0	DSTB	GAS	00

Description

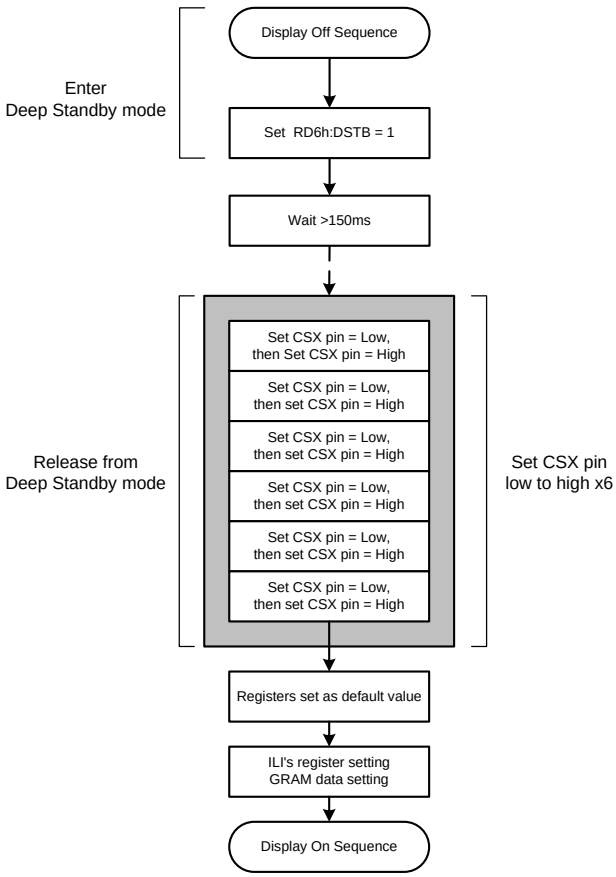
GAS: Low voltage detection (LVD) control.

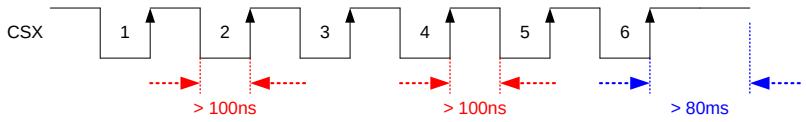
GAS	Low voltage detection
0	Enable
1	Disable

DSTB: Deep Standby control.

DSTB	Deep Standby
1	Enable
0	Disable

Deep Standby Mode Entry/Exit Flow





<table>
<tr><td></td><td>Note： The ILI9340X provides two ways to exit the Deep Standby Mode：
(1) Exit Deep Standby Mode by pull down CSX to low (“0”) 6 times.
(2) Input a RESX pulse with effective low level duration to start up the inside logic regulator and makes a transition to the initial state.</td></tr>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>GAS</th><th>DSTB</th></tr>
<tr><td>Power On Sequence</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>SW Reset</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>HW Reset</td><td>1’b0</td><td>1’b0</td></tr>
</table>
</td></tr>
</table>

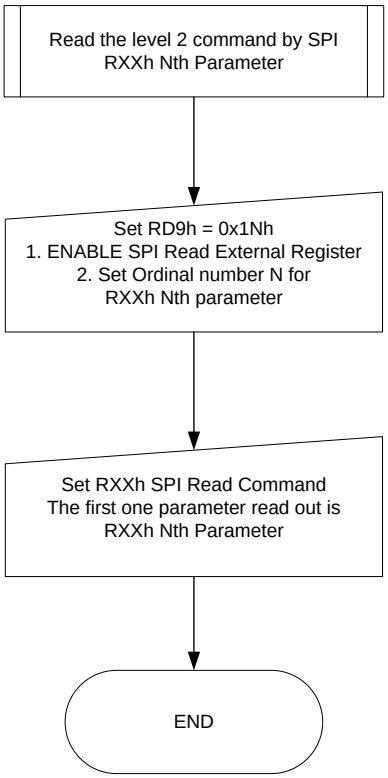
8.3.14. Get External Register by SPI (D9h)

D9h	XREG (Get External Register)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	0	1	D9h
1st Parameter	1	1	↑	XX	0	0	0	ENSPI	SPI_EXT_ORD [3:0]				00

Description

ENSPI : This command is used to enable the SPI interface to access the level 2 commands.

SPI_EXT_ORD [3:0]: Th SPI will get the one desired parameter of the external register by setting this ordinal number.



Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	ENSPI	SPI_EXT_ORD [3:0]
Power On Sequence	1'b0	4'b0000
SW Reset	1'b0	4'b0000
HW Reset	1'b0	4'b0000

8.3.15. Digital Gamma Control 1 (E2h)

E2h	DGAMCTRL (Digital Gamma Control 1)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
1st Parameter	1	1	↑	XX	RCA0 [7:0]								XX
:	1	1	↑	XX	RCAn [7:0]								XX
64th Parameter	1	1	↑	XX	RCA63 [7:0]								XX
Description	**RCAx [7:0]:** Gamma Macro-adjustment registers for red gamma curve.												
Restriction	EXTC should be high to enable this command												

Register Availability

Status	Availa ility
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	RCAx [7:0]
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

8.3.16. Digital Gamma Control 1 (E3h)

E3h	DGAMCTRL (Digital Gamma Control 2)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
1st Parameter	1	1	↑	XX	BCA0 [7:0]								XX
:	1	1	↑	XX	BCAn [7:0]								XX
64th Parameter	1	1	↑	XX	BCA63 [7:0]								XX
Description	**BCAx [7:0]:** Gamma Macro-adjustment registers for blue gamma curve.												
Restriction	EXTC should be high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	BCAx [7:0]
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

8.3.17. Positive Gamma Correction (E4h)

E4h	PGAMCTRL (Positive Gamma Control)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	1	0	0	E4h
1st Parameter	1	1	↑	XX	0	0	0	0	VP0 [3:0]				00
2ndParameter	1	1	↑	XX	0	0	VP1 [5:0]						05
3rdParameter	1	1	↑	XX	0	0	VP2 [5:0]						12
4th Parameter	1	1	↑	XX	0	0	0	0	VP4 [3:0]				09
5th Parameter	1	1	↑	XX	0	0	0	VP6 [4:0]					17
6th Parameter	1	1	↑	XX	0	0	0	0	VP13 [3:0]				08
7th Parameter	1	1	↑	XX	0	VP20 [6:0]							40
8th Parameter	1	1	↑	XX	VP36 [3:0]				VP27 [3:0]				55
9th Parameter	1	1	↑	XX	0	VP43 [6:0]							50
10thParameter	1	1	↑	XX	0	0	0	0	VP50 [3:0]				04
11thParameter	1	1	↑	XX	0	0	0	VP57 [4:0]					0A
12thParameter	1	1	↑	XX	0	0	0	0	VP59 [3:0]				07
13thParameter	1	1	↑	XX	0	0	VP61 [5:0]						21
14thParameter	1	1	↑	XX	0	0	VP62 [5:0]						24
15thParameter	1	1	↑	XX	0	0	0	0	VP63 [3:0]				0D
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction	EXTC should be high to enable this command												
Note													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

8.3.18. Negative Gamma Correction (E5h)

E5h	NGAMCTRL (Negative Gamma Correction)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	1	0	1	E5h
1st Parameter	1	1	↑	XX	0	0	0	0	VN0 [3:0]				00
2ndParameter	1	1	↑	XX	0	0	VN1 [5:0]						05
3rdParameter	1	1	↑	XX	0	0	VN2 [5:0]						11
4th Parameter	1	1	↑	XX	0	0	0	0	VN4 [3:0]				09
5th Parameter	1	1	↑	XX	0	0	0	VN6 [4:0]					17
6th Parameter	1	1	↑	XX	0	0	0	0	VN13 [3:0]				09
7th Parameter	1	1	↑	XX	0	VN20 [6:0]							40
8th Parameter	1	1	↑	XX	VN36 [3:0]				VN27 [3:0]				46
9th Parameter	1	1	↑	XX	0	VN43 [6:0]							4E
10thParameter	1	1	↑	XX	0	0	0	0	VN50 [3:0]				08
11thParameter	1	1	↑	XX	0	0	0	VN57 [4:0]					0F
12thParameter	1	1	↑	XX	0	0	0	0	VN59 [3:0]				0C
13thParameter	1	1	↑	XX	0	0	VN61 [5:0]						21
14thParameter	1	1	↑	XX	0	0	VN62 [5:0]						25
15thParameter	1	1	↑	XX	0	0	0	0	VN63 [3:0]				0D
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction	EXTC should be high to enable this command												
Note													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

8.3.19. MADCTL EOR (ECh)

ECh	MADCTL EOR												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	1	0	0	ECh
1st Parameter	1	1	↑	XX	MY_EOR	MX_EOR	MV_EOR	ML_EOR	BGR_EOR	0	0	REV	49

Description

MY_EOR / MX_EOR / MV_EOR /ML_EOR/ BGR_EOR:

The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of MADCTL Parameter.

REV: Select whether the liquid crystal type is normally white type or normally black type.

REV	Liquid crystal type
0	Normally black
1	Normally white

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	MY_EOR	MX_EOR	MV_EOR	ML_EOR	BGR_EOR	REV
Power On Sequence	1'b0	1'b1	1'b0	1'b0	1'b1	1'b1
SW Reset	1'b0	1'b1	1'b0	1'b0	1'b1	1'b1
HW Reset	1'b0	1'b1	1'b0	1'b0	1'b1	1'b1

8.3.20. LED_EN/LED_PWM Control (F1h)

<table>
<tr><th>ECh</th><th colspan="13">MADCTL EOR</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>F1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>50h</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>LED_EN_OEB</td><td>LED_EN_OUT</td><td>LED_PWM_OEB</td><td>LED_PWM_OUT</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="13">LED_EN (Output Pin) Control:
<table><tr><th>LED_EN_OEB</th><th>LED_EN_OUT</th><th>LED_EN</th></tr><tr><td>1</td><td>X</td><td>Hi-Z</td></tr><tr><td>0</td><td>0</td><td>GND</td></tr><tr><td>0</td><td>1</td><td>IOVCC</td></tr></table>LED_PWM (Output Pin) Control:<table><tr><th>LED_PWM_OEB</th><th>LED_PWM_OUT</th><th>LED_PWM</th></tr><tr><td>1</td><td>X</td><td>Hi-Z</td></tr><tr><td>0</td><td>0</td><td>GND</td></tr><tr><td>0</td><td>1</td><td>IOVCC</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>No</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr><tr><th>LED_EN_OEB</th><th>LED_EN_OUT</th><th>LED_PWM_OEB</th><th>LED_PWM_OUT</th></tr><tr><td>Power On Sequence</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr><tr><td>SW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr><tr><td>HW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr></table></td></tr>
</table>

8.3.21. Interface Control (F6h)

F6h	IFCTL (Data Format Selection)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
1st Parameter	1	1	↑	XX	0	0	EPF [1:0]		0	0	MDT [1:0]		00
2nd Parameter	1	1	↑	XX	0	0	ENDIAN	0	DM [1:0]		RM	RIM	00

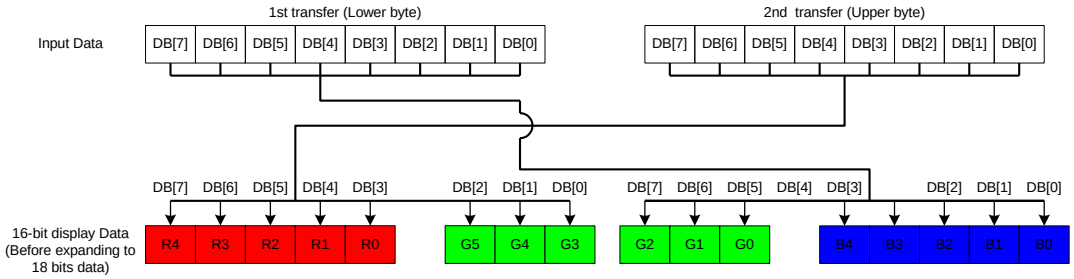
Description

MDT [1:0]: Select the method of display data transferring.

ENDIAN: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

ENDIAN	Data transf r Mode
0	Normal (MSB first, default)
1	Little Endian (LSB first)

Note: Little Endian is valid on only 65K 8-bit and 9-bit MCU interface mode.



DM [1:0]: Select the display operation mode.

DM [1]	DM [0]	Display Operation Mode
0	0	Internal clock operation
0	1	RGB Interface Mode
1	0	VSYNC interface mode
1	1	Setting disabled

The DM [1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RM: Select the interface to access the GRAM.

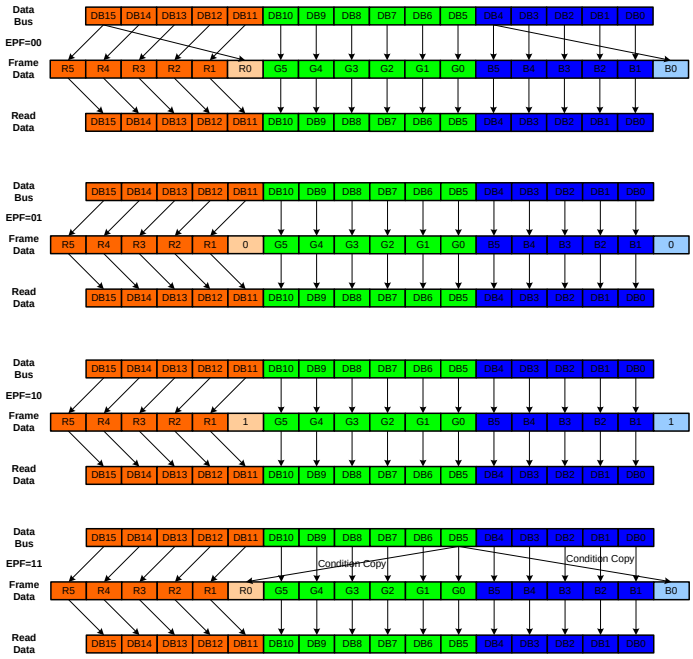
Set RM to "1" when writing display data by the RGB interface.

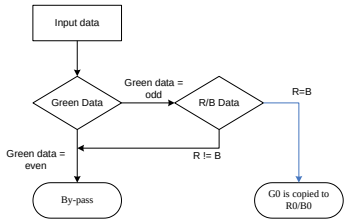
RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
0	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
1	110 (262K color)	6- bit RGB interface (3 transfer/pixel)
	101 (65K color)	6- bit RGB interface (3 transfer/pixel)

EPF [1:0]: 65K color mode data format.





EPF [1:0]	Expand 16 bbp (R,G,B) to 18bbp (R,G,B)
00	MSB is inputted to LSB r [5:0] = {R [4:0], R [4]} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], B [4]}
01	"0" is inputted to LSB r [5:0] = {R [4:0], 0} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 0} Exception: R [4:0], B[4:0 = 5'h1F → r [5:0], [5:] = 6'h3F
10	"1" is inputted to LSB r [5:0] = {R [4:0], 1} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 1} Exception: R [4:0], B[4:0] = 5'h00 → r [5:0], b[5:0] = 6'h00
11	Compare R [4:0], G [5:1], B [4:0] case: Case 1: R=G=B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]} Case 2: R=B≠G → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 3: R=G≠B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]}

Restriction	EXTC should be high to enable this command

Register Availability

Status	Availabil ty
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	EPF [1:0]	MDT [1:0]	ENDIAN	DM [1:0]	RM	RIM
Power On Sequence	2'b00	2'b00	1'b0	2'b00	1'b0	1'b0
SW Reset	2'b00	2'b00	1'b0	2'b00	1'b0	1'b0
HW Reset	2'b00	2'b00	1'b0	2'b00	1'b0	1'b0

8.3.22. NV Memory Write (FDh)

FDh	NVMWR (NV Memory Write)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	0	1	FDh
1st Parameter	1	1	↑	XX	PGM_ADR [7:0]								XX
2nd Parameter	1	1	↑	XX	PGM_ADR [15:8]								XX
3rd Parameter	1	1	↑	XX	PGM_DATA [7:0]								XX

Description

This command is used to program the NV memory data. After a successful MTP operation, the information of PGM_DATA [7:0] will programmed to NV memory.

PGM_ADR [15:0]: The select bits of ID1, ID2, ID3 ,VCOM , MADCTL and Gamma OTP programming.

PGM_DATA [7:0]:The programmed data.

PGM_ADR [15：0]	PGM_DATA [7：0]								Programmed NV Memory Selection	Check ADDR
0001h	ID1								ID1 programming	EBP1
0002h	ID2								ID2 programming	EBP2
0003h	ID3								ID3 programming	EBP3
0005h	VCOM								VCOM programming	BAP1
0004h	MY	MX	MV	ML	BGR	0	0	REV	MADCTL programming	ECP1
0043h	0	0	0	0	VP0[3:0]				PGAMCTRL (Positive Gamma Control) programming	E4P1
0044h	0	0	VP1[5:0]							E4P2
0045h	0	0	VP2[5:0]							E4P3
0046h	0	0	0	0	VP4[3:0]					E4P4
0047h	0	0	0	VP6[4:0]						E4P5
0048h	0	0	0	0	VP13[3:0]					E4P6
0049h	0	VP20[6:0]								E4P7
004Ah	VP36[3:0]				VP27[3:0]					E4P8
004Bh	0	VP43[6:0]								E4P9
004Ch	0	0	0	0	VP50[3:0]					E4P10
004Dh	0	0	0	VP57[4:0]						E4P11
00C7h	0	0	0	0	VP59[3:0]					E4P12
00C8h	0	0	VP61[5:0]							E4P13
00C9h	0	0	VP62[5:0]							E4P14
00CAh	0	0	`0	0	VP63[3:0]					E4P15
00CB	0	0	0	0	VN0[3:0]				NGAMCTRL (Negative Gamma Control) programming	E5P1
00CC	0	0	VN1[5:0]							E5P2
00CD	0	0	VN2[5:0]							E5P3
00CE	0	0	0	0	VN4[3:0]					E5P4
00CF	0	0	0	VN6[4:0]						E5P5
00D0	0	0	0	0	VN13[3:0]					E5P6
00D1	0	VN20[6:0]								E5P7
00D2	VN36[3:0]				VN27[3:0]					E5P8
00D3	0	VN43[6:0]								E5P9
00D4	0	0	0	0	VN50[3:0]					E5P10
00D5	0	0	0	VN57[4:0]						E5P11

	00D6	0	0	0	0	VN59[3:0]			E5P12
	00D7	0	0	VN61[5:0]					E5P13
	00D8	0	0	VN62[5:0]					E5P14
	00D9	0	0	0	0	VN63[3:0]			E5P15

Restriction

EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	PGM_ADR [15:0]	PGM_DATA [7:0]
Power On Sequence	16'h0000	MTP value
SW Reset	16'h0000	MTP value
HW Reset	16'h0000	MTP value

8.3.23. NV Memory Protection Key (FEh)

FEh	NVMPKEY (NV Memory Protection Key)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
1st Parameter	1	1	↑	XX	KEY [23:16]								55
2nd Parameter	1	1	↑	XX	KEY [15:8]								AA
3rd Parameter	1	1	↑	XX	KEY [7:0]								66
Description	**KEY [23:0]:** NV memory programming protection key. When writing MTP data to D1h, this register must be set to 0x55AA66h to enable MTP programming. If D1h register is not written with 0x55AA66h, then NV memory programming will be aborted.												
Restriction	EXTC should be high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	KEY [23:0]=55AA66h
SW Reset	KEY [23:0]=55AA66h
HW Reset	KEY [23:0]=55AA66h

8.3.24. NV Memory Status Read (FFh)

D2h	RDNVM (NV Memory Status Read)												
	DCX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	1	1	FFh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	MADCTL_CNT [1:0]		ID3_CNT [1:0]		ID2_CNT [1:0]		ID1_CNT [1:0]		XX
3rd Parameter	1	↑	1	XX	OTP_BUSY	0	0	GAMMA_MARK	0	VMF_MARK [2:0]			XX

Description

ID1_CNT [1:0] / ID2_CNT [1:0] / ID3_CNT [1:0] /MADCTL_CNT [1:0]: NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory.

ID1_CNT [1:0] / ID2_CNT [1:0] ID3_CNT [1:0] / MADCTL_CNT [1:0]		Description
Status		Availability
0	0	No Programmed
0	1	Programmed 1 time
1	1	Programmed 2 times

VMF_MARK [2:0]: NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory.

VMF_MARK [2:0]			Description
Status			Availability
0	0	0	No Programmed
0	0	1	Programmed 1 time
0	1	1	Programmed 2 times
1	1	1	Programmed 3 times

OTP_BUSY: The status bit of NV memory programming.

BUSY	The Status of NV Memory
0	Idle
1	Busy

GAMMA_MARK: NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory.

Restriction: EXTC should be high to enable this command

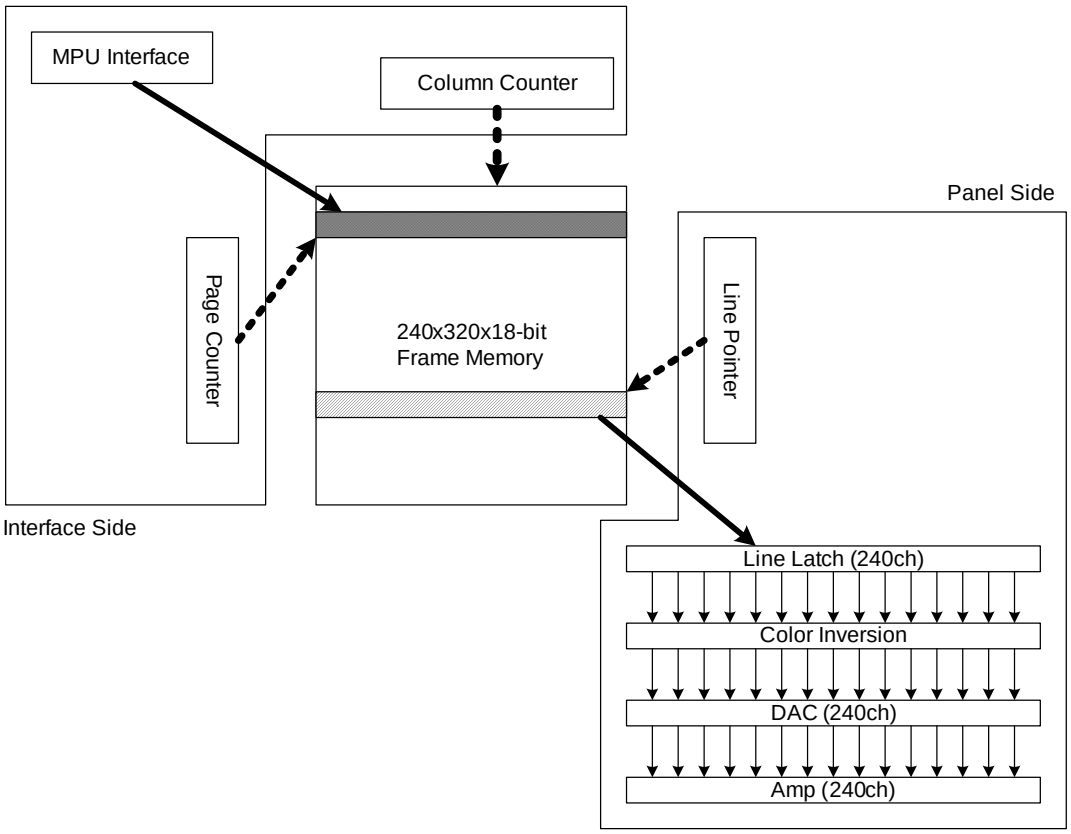
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

9. Display Data RAM

9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.

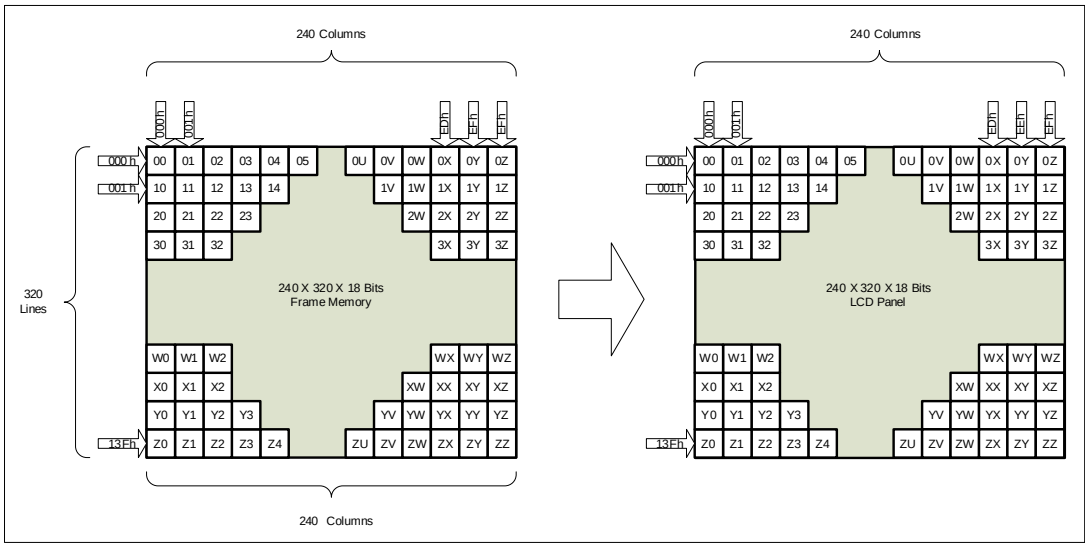


9.2. Memory to Display Address Mapping

9.2.1. Normal Display On or Partial Mode On, Vertical Scroll Mode Off

In this mode, the content of frame memory within an area where column pointer is 0000h to 00Efh and page pointer is 0000h to 013Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)

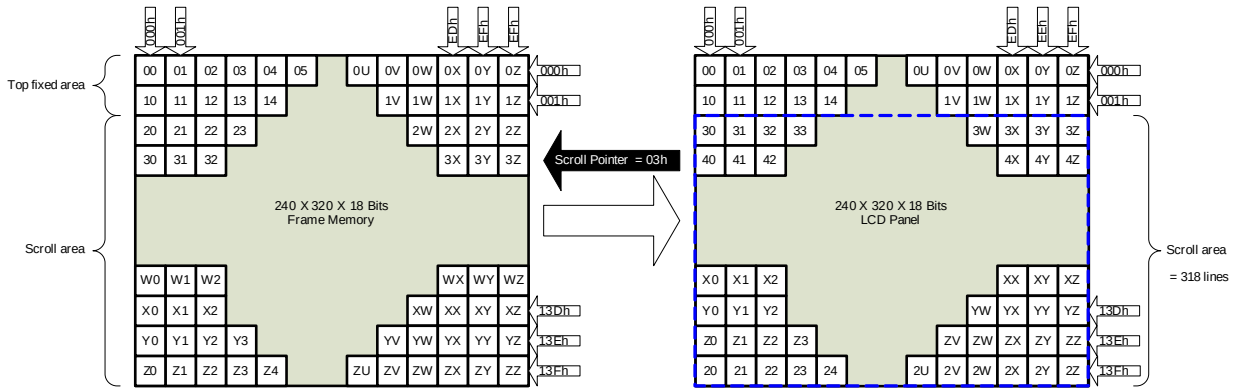


9.2.2. Vertical Scroll Mode

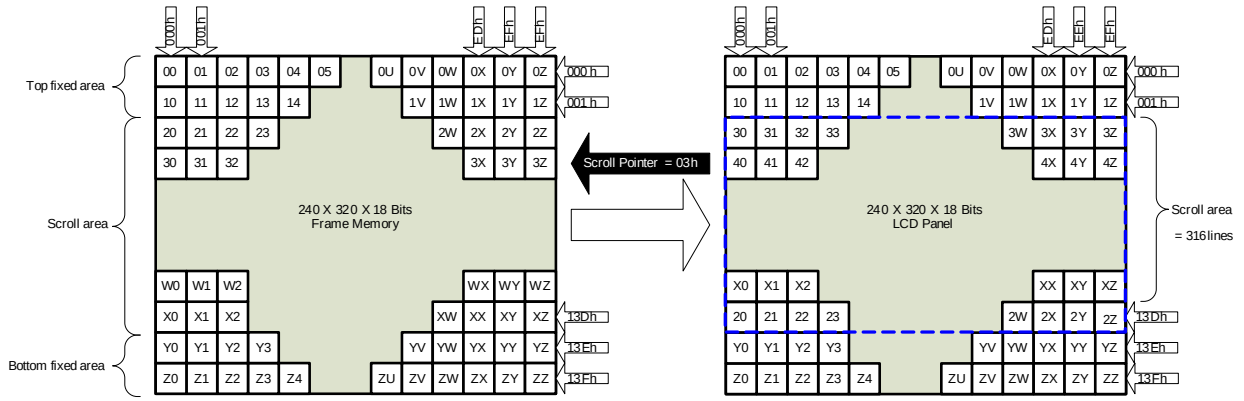
There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

The Vertical Scroll Mode function is explained by these examples in the following.

TFA=2, VSA=318, BFA=0 when MADCTL ML bit = 0



TFA=2, VSA=316, BFA=2 when MADCTL ML bit = 0



Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.

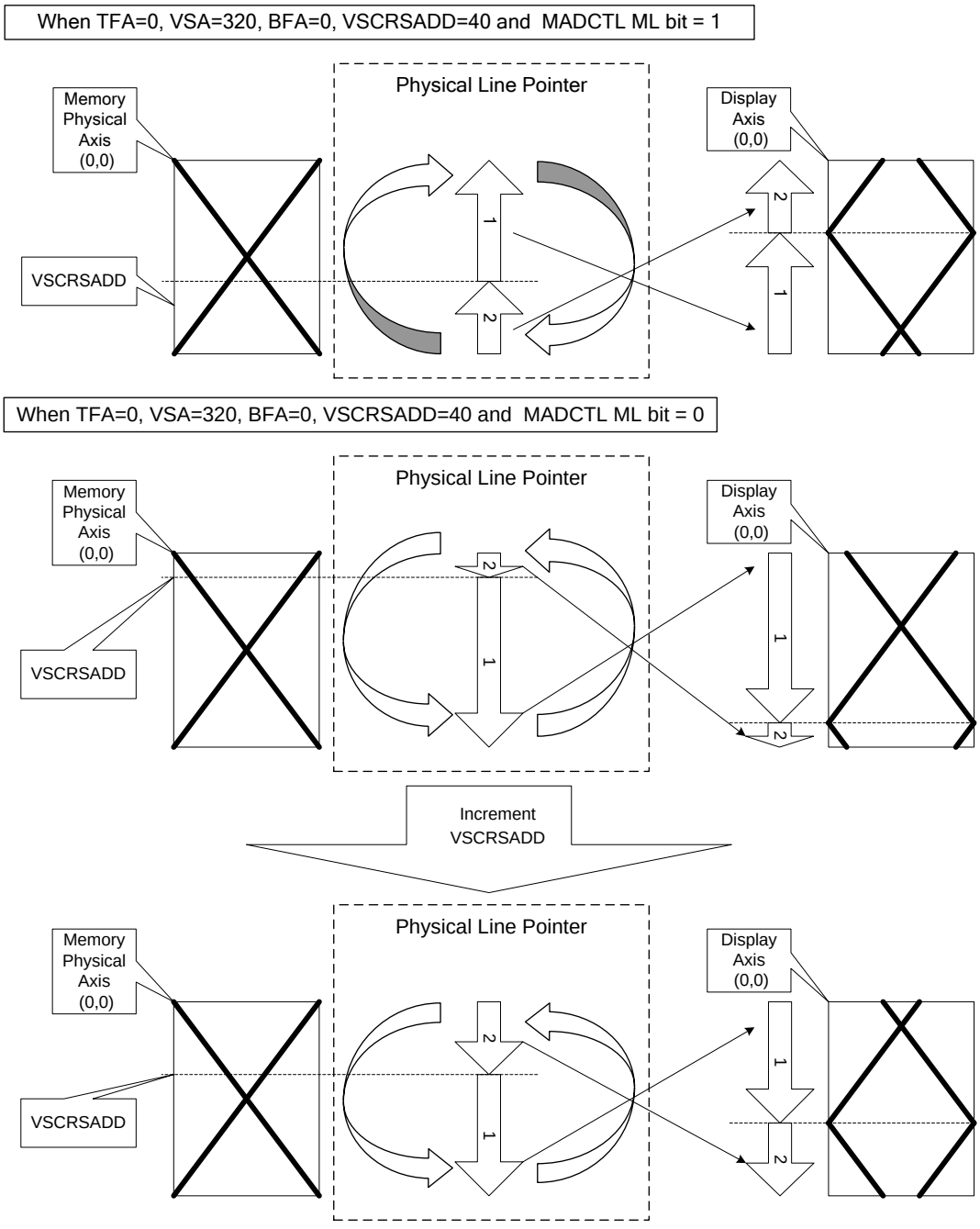
9.2.3. Vertical Scroll Example

9.2.4. Case1: TFA+VSA+BFA < 320

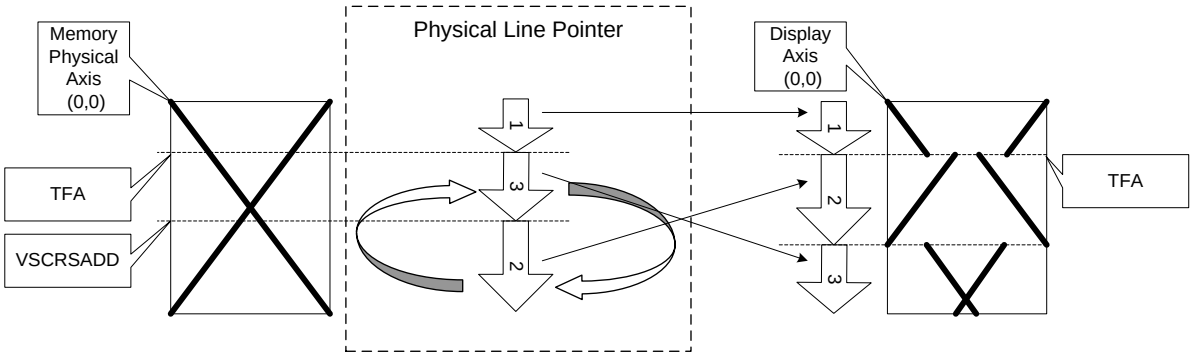
This setting is prohibited, unless unexpected picture will be shown.

9.2.5. Case2: TFA+VSA+BFA = 320 (Rolling Scrolling)

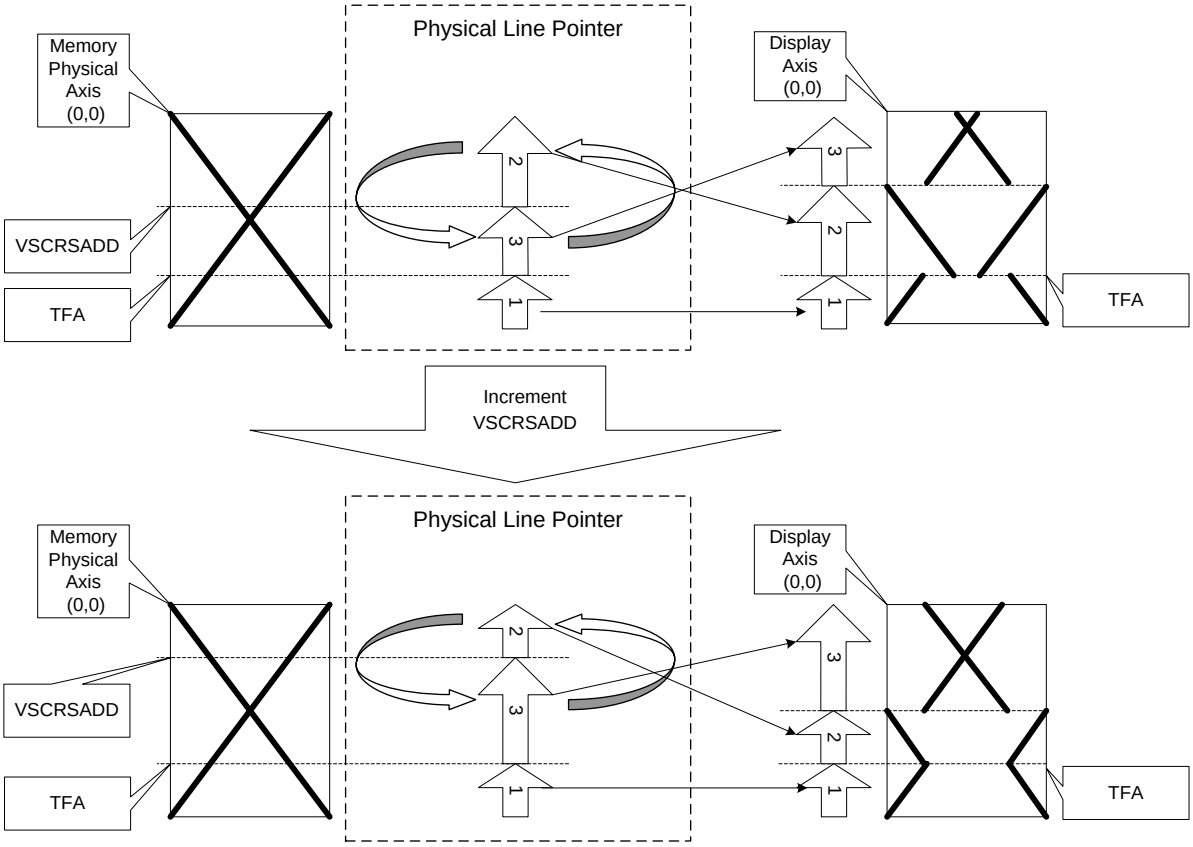
The operation of Rolling Scrolling is explained by these examples in the following.



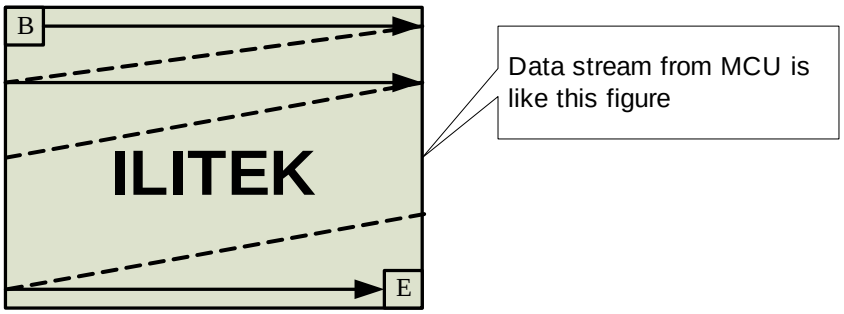
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



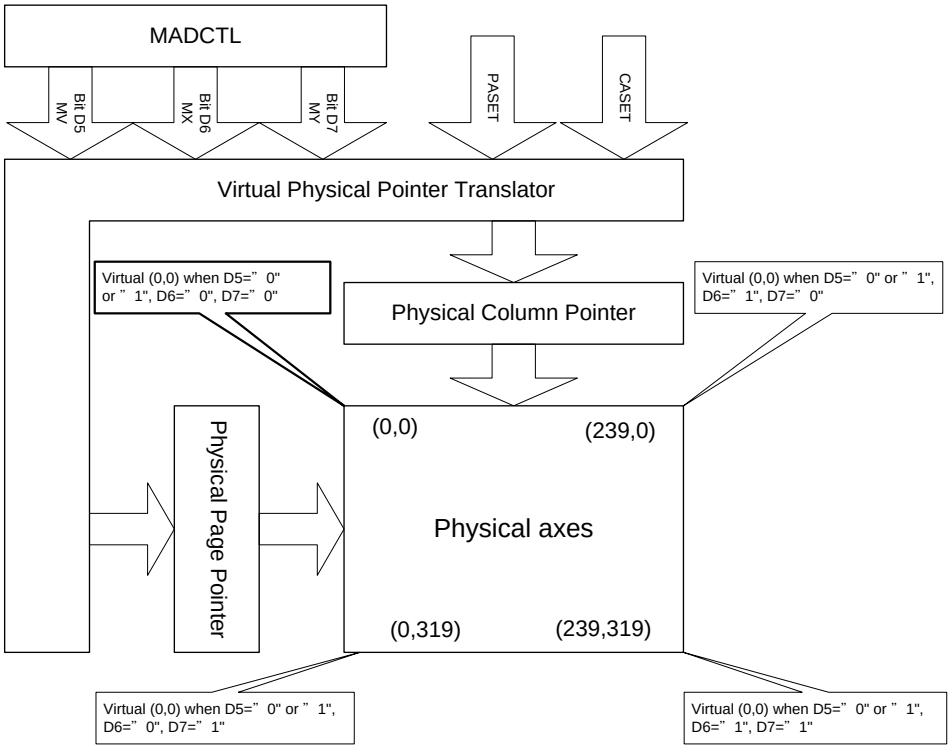
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



9.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits D5, D6, and D7 as described below.



D5	D6	D7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

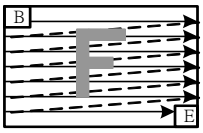
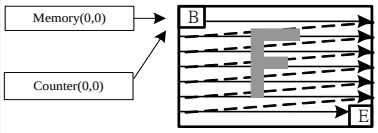
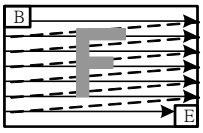
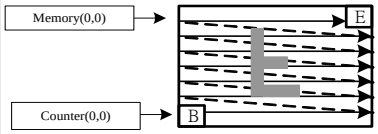
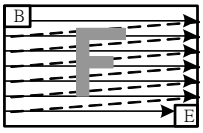
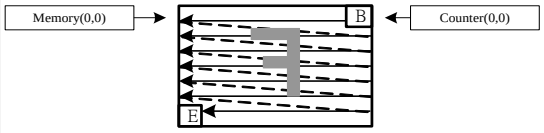
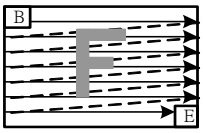
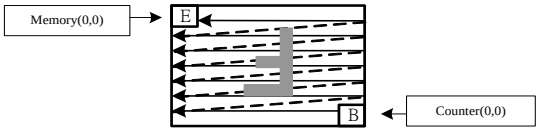
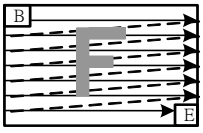
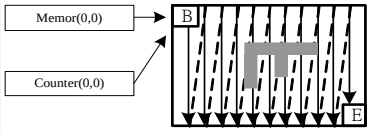
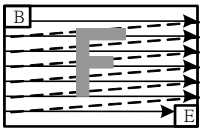
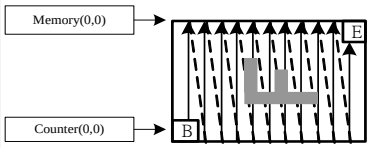
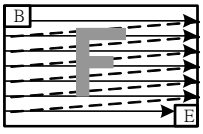
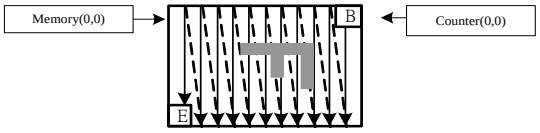
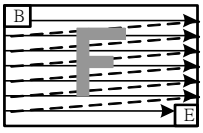
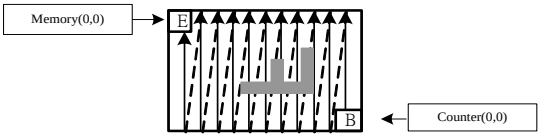
Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

Note:Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits D7, D6 and D5.

The write order for each pixel unit is

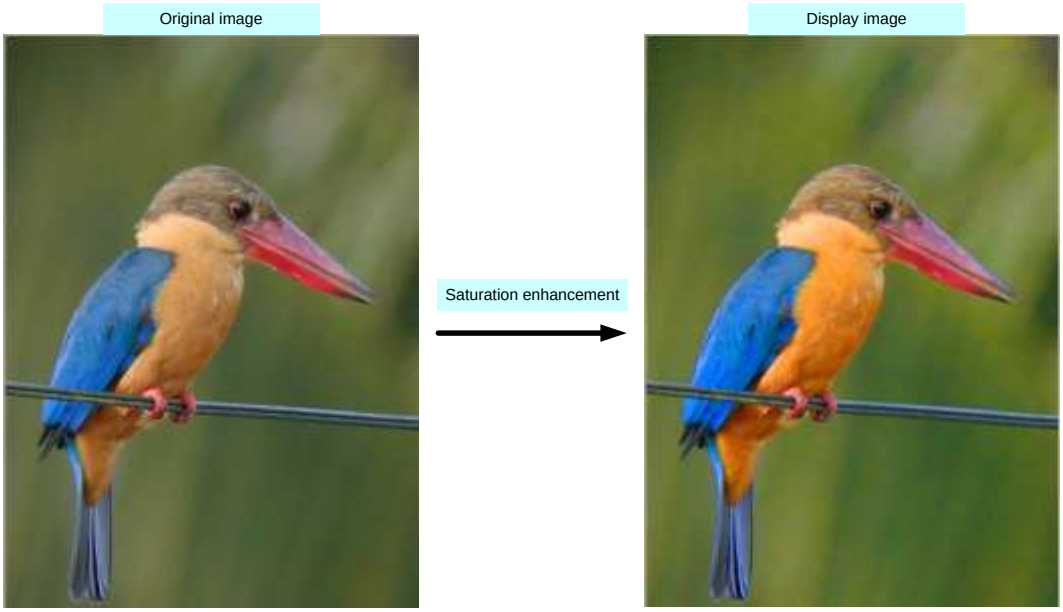
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MPU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
XY Exchange X-Mirror	1	1	0		
XY Exchange XY-Mirror	1	1	1		

10. Color Enhancement function

The Color Enhancement Function enhances saturation by calculating image data of the displayed on the liquid crystal panel . The saturation enhancement coefficients of red, yellow, green, cyan, blue, magenta…, are set independently. The function enhances color and makes pixel colors more vivid.



Saturation Enhancement image

The display image with color enhanced is generated when the saturation enhancement coefficients of the input image are 1.0 or more. See the saturation diagram, the colors of the input image are enhanced.

The both colors green and magenta keep the original gary value without enhanced.

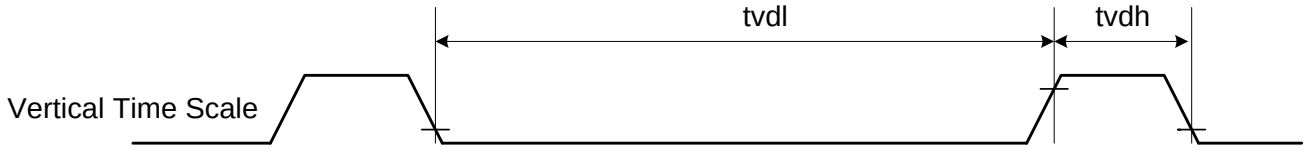
11. Tearing Effect Output

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

11.1. Tearing Effect Line Modes

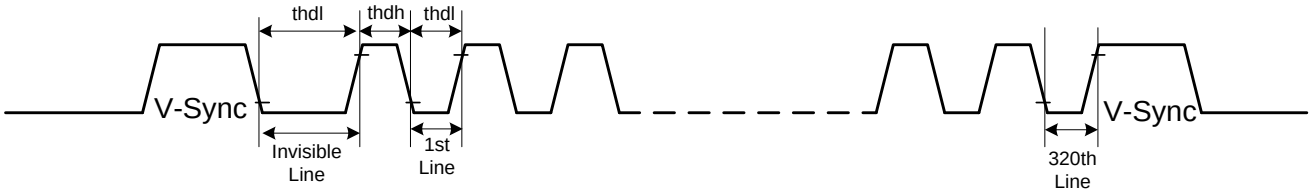
Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

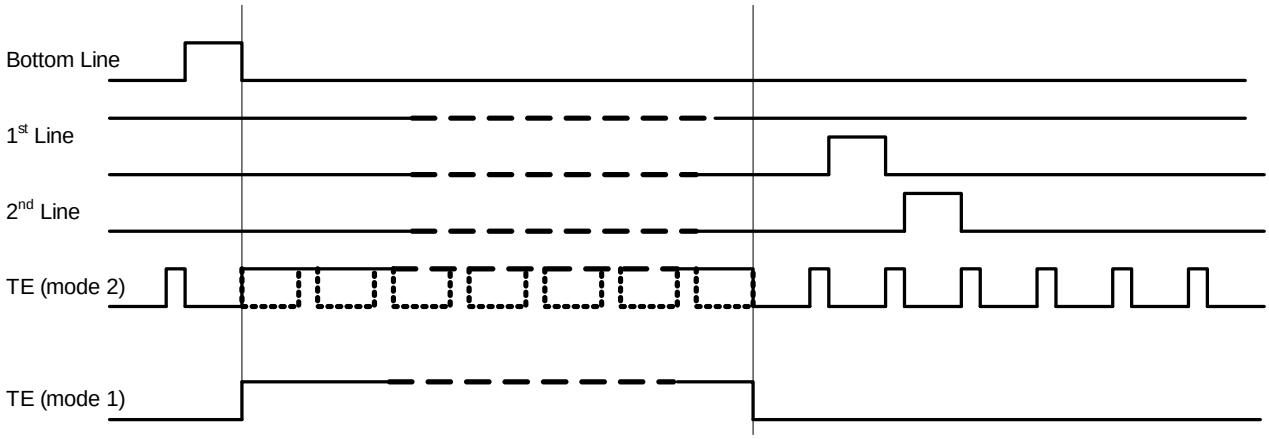
Tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 320 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

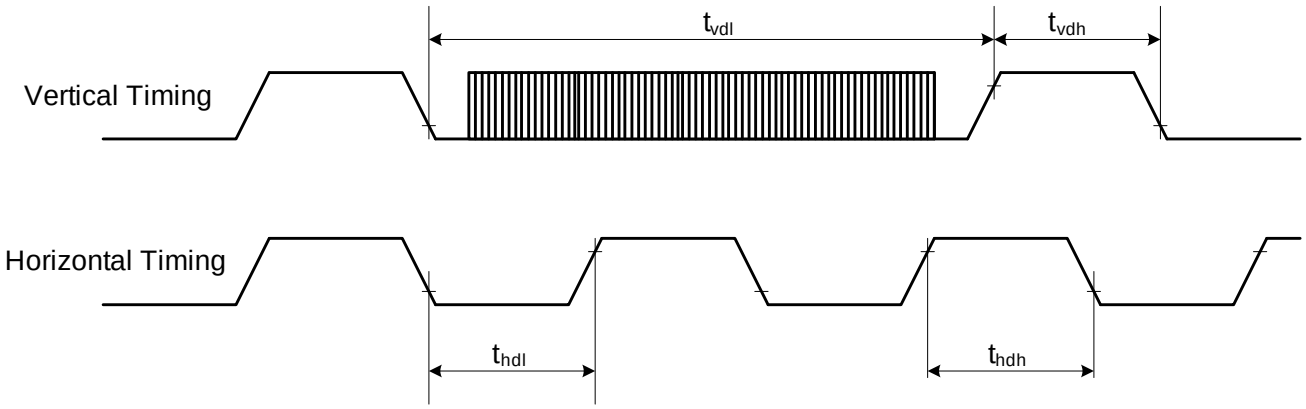
Thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

11.2. Tearing Effect Line Timings

The tearing effect signal is described below:

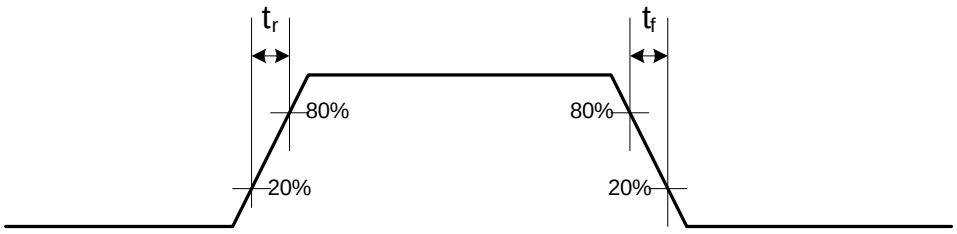


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	--	--	--	ms	
t_{vdh}	Vertical timing high duration	1000	--	--	us	
t_{hdl}	Horizontal timing low duration	--	--	--	us	
t_{hdh}	Horizontal timing high duration	--	--	500	us	

Note:

1. The timings in Table as above apply when MADCTL D4=0 and D4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

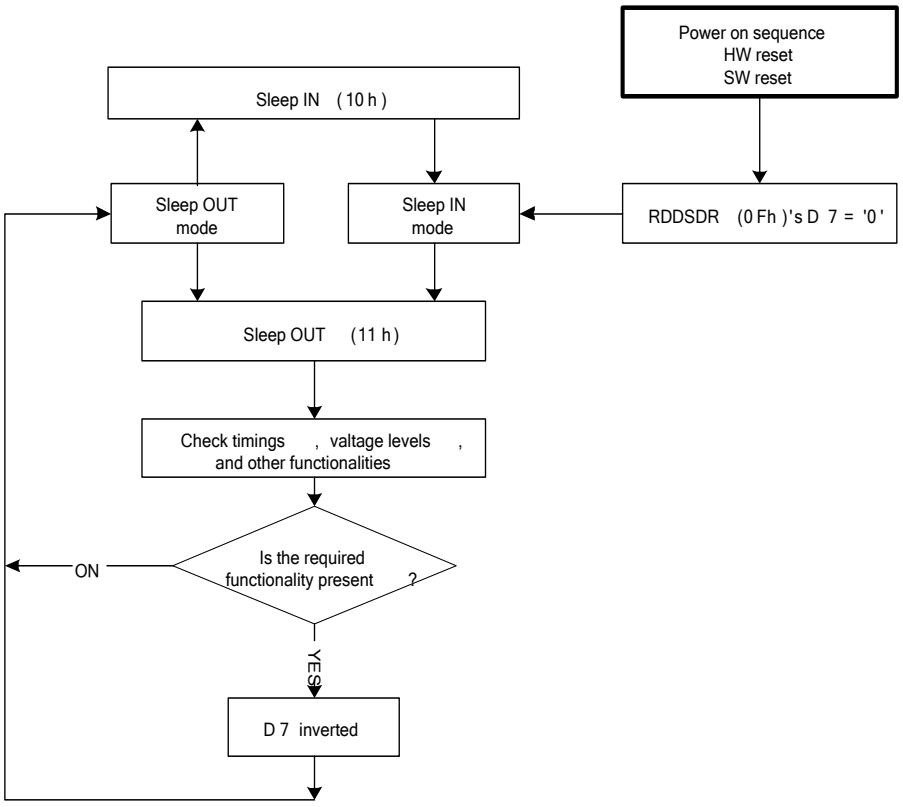
12. Sleep Out – Command and Self-Diagnostic Functions of the Display Module

12.1. Register loading Detection

The Sleep Out command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from NV Memory(or similar device) to registers of the display controller is working properly.

If the register loading detection is successfully, there is inverted (= increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If it is failure, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

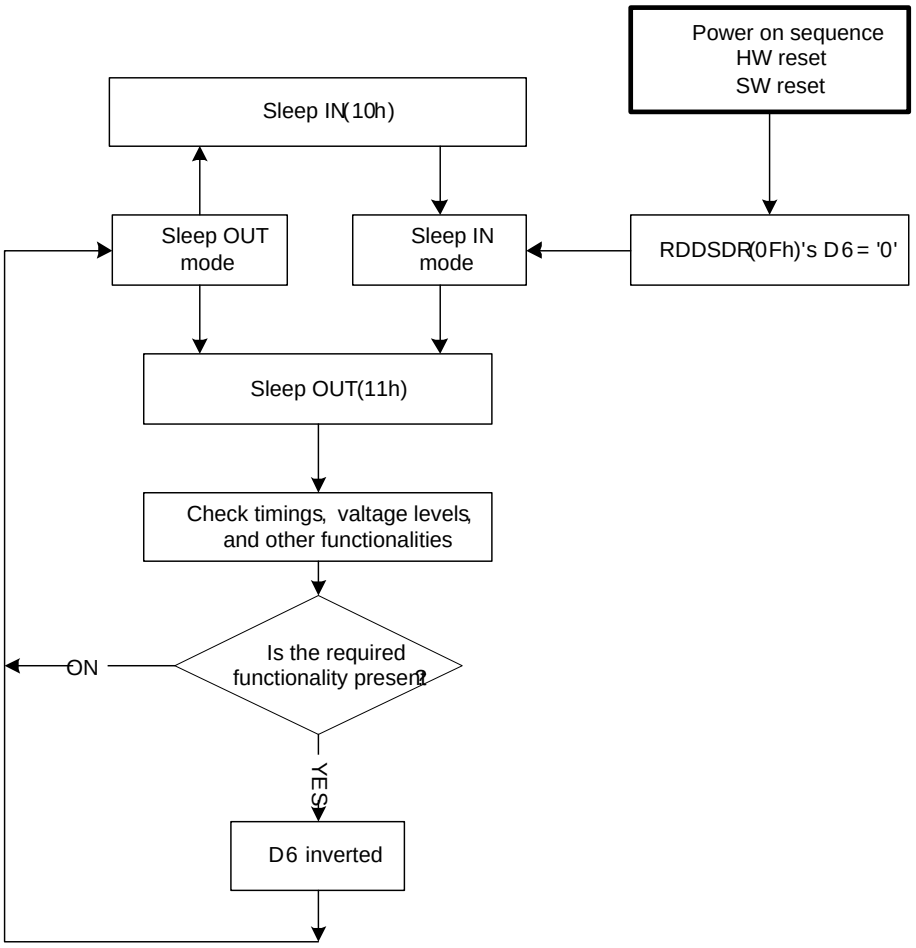


12.2. Functionality Detection

The Sleep Out command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out command, when there is changing from Sleep In mode to Sleep Out mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out command is sent in Sleep Out mode.

13. Power On/Off Sequence

IOVCC and VCI can be applied in any order. During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

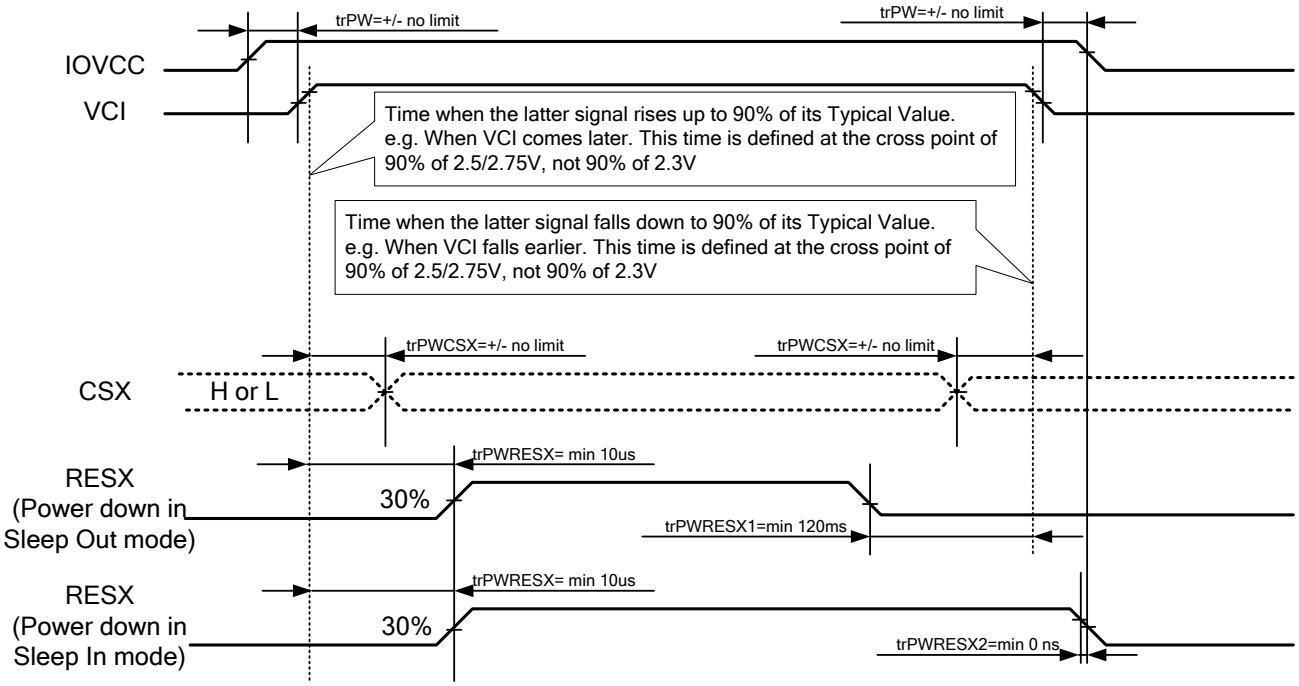
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 13.1 and 13.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

13.1. RESX line is held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

13.2. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9340X will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” actives.

14. Power Level Definition

14.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

   In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

   In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

   In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

   In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

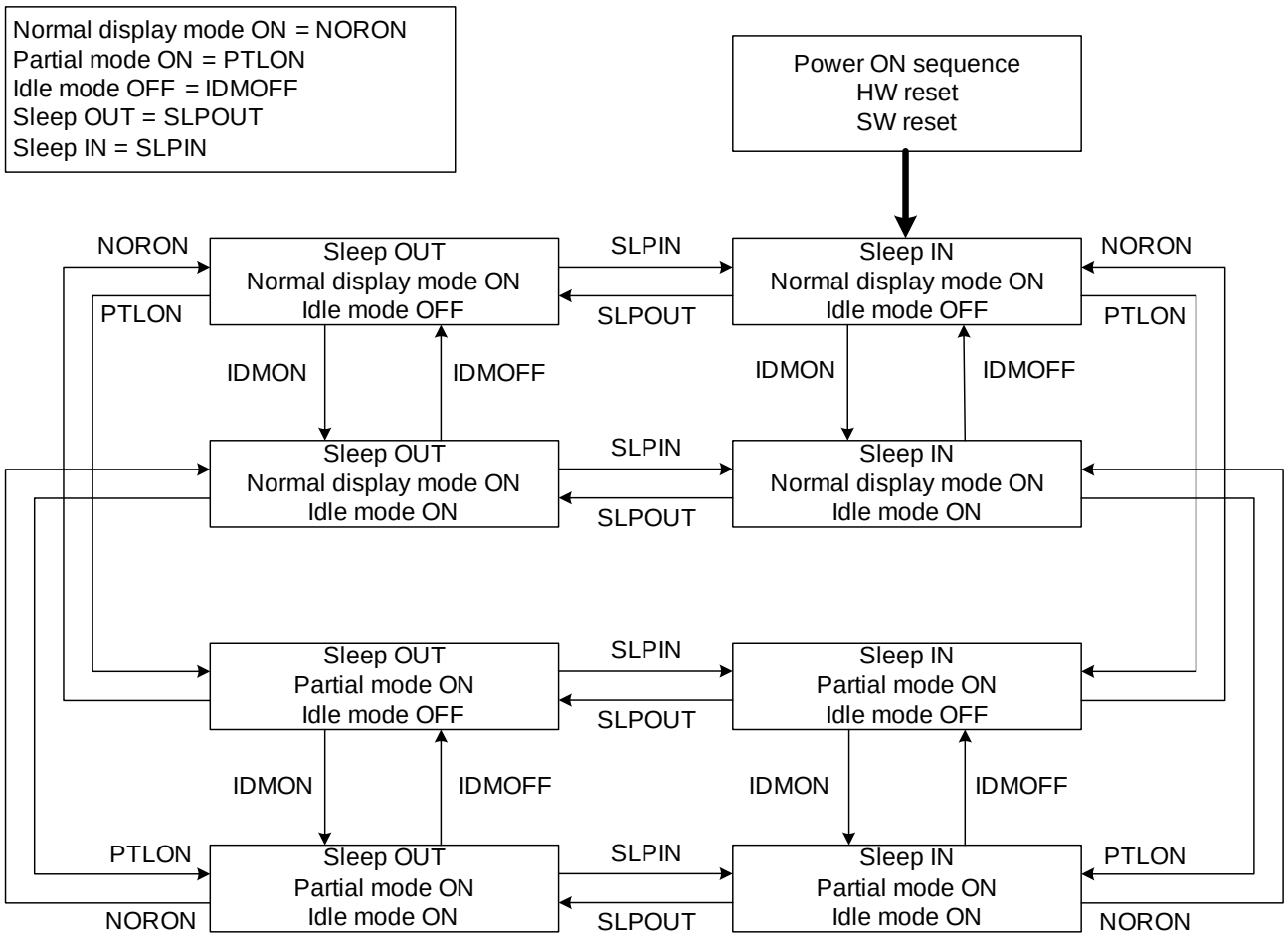
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.

6. Power Off Mode.

   In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

14.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

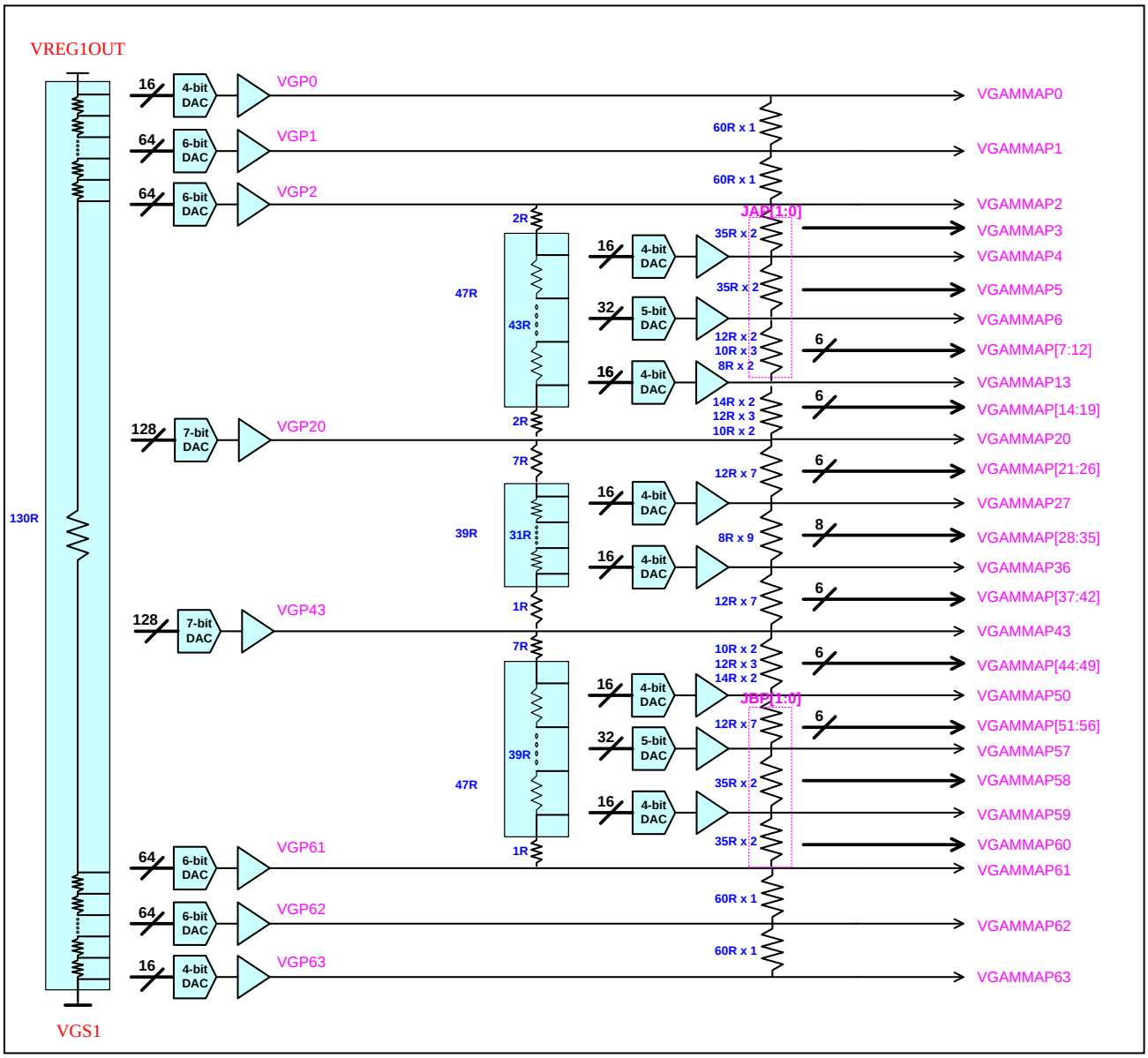
Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

15. Gamma Curves Selection

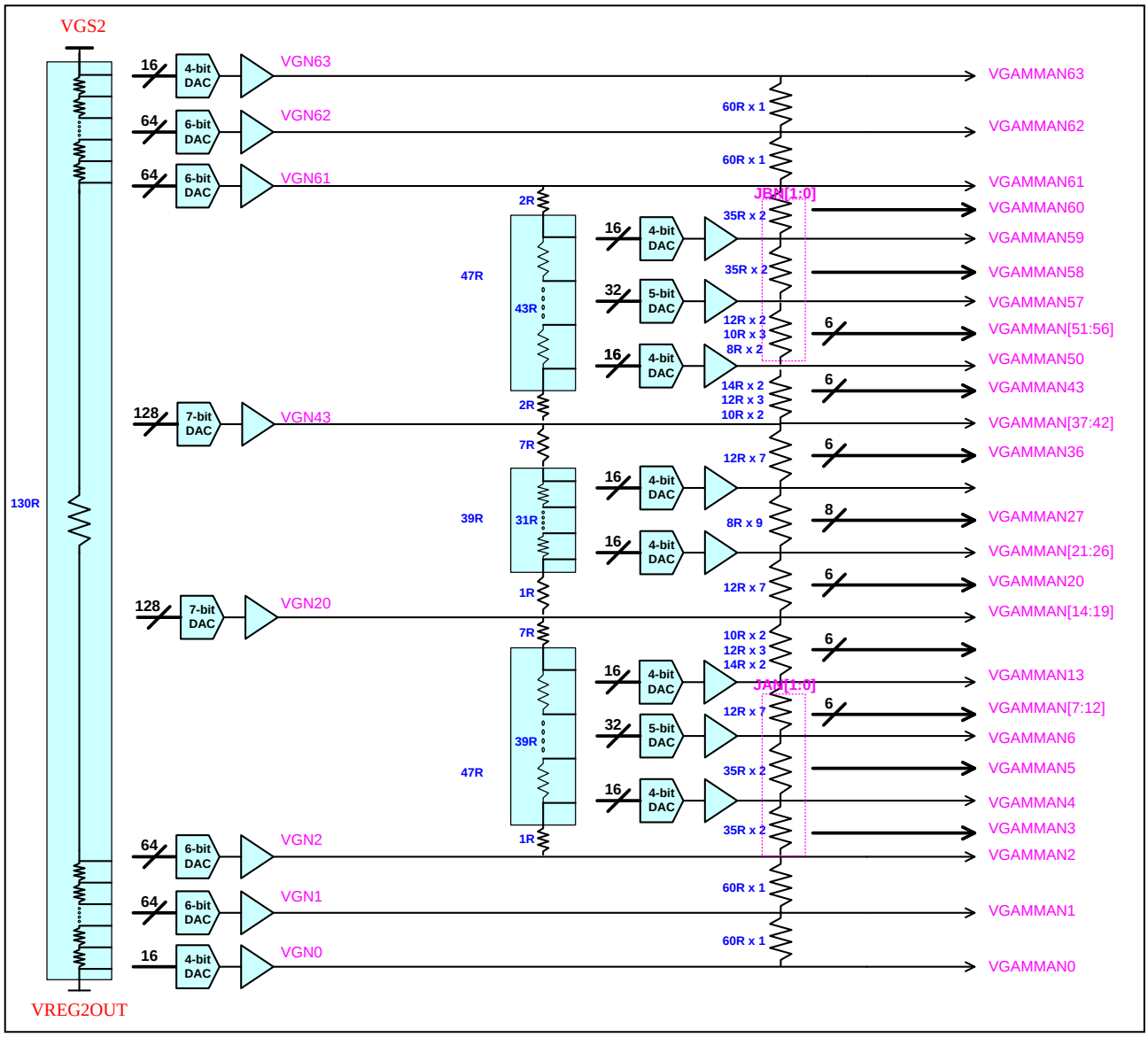
ILI9340X provide one gamma curves (Gamma2.2).

15.1. Gamma Default Values

Positive Gamma Control (E4h)



Negative Gamma Control (E5h)



Positive polarity	Resister stream	Gamma 64 grayscale voltage calculation formula
VGAMMAP0	non	VGS1+ΔVDHP(130R-1R*VP0[3:0])/130R
VGAMMAP1	non	VGS1+ΔVDHP(130R-1R*VP0[5:0])/130R
VGAMMAP2	non	VGS1+ΔVDHP(130R-1R*VP0[5:0])/130R
VGAMMAP3	variable	VGAMMAP4+(VGAMMP2-VGAMMAP4)*JAP[1:0]
VGAMMAP4	variable	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((40R-1R*VP4[3:0])/47R)
VGAMMAP5	variable	VGAMMAP6+(VGAMMP4-VGAMMAP6)*JAP[1:0]
VGAMMAP6	variable	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((45R-1R*VP6[4:0])/47R)
VGAMMAP7	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP8	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP9	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP10	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP11	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP12	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP13	variable	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((17R-1R*VP13[3:0])/47R)
VGAMMAP14	1.4R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(7R)/(8.4R)
VGAMMAP15	1.4R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(5.6R)/(8.4R)
VGAMMAP16	1.2R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(4.4R)/(8.4R)
VGAMMAP17	1.2R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(3.2R)/(8.4R)
VGAMMAP18	1.2R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(2R)/(8.4R)
VGAMMAP19	1R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(1R)/(8.4R)
VGAMMAP20	1R	VGS1+ΔVDHP(130R-1R*VP20 [6:0])/130R : VP20 [6:0] = 0~63 VGS1+ΔVDHP(129R-1R*VP20 [6:0])/130R : VP20 [6:0] = 64~127
VGAMMAP21	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(7.2R)/(8.4R)
VGAMMAP22	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(6R)/(8.4R)
VGAMMAP23	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(4.8R)/(8.4R)
VGAMMAP24	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(3.6R)/(8.4R)
VGAMMAP25	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(2.4R)/(8.4R)
VGAMMAP26	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(1.2R)/(8.4R)
VGAMMAP27	1.2R	VGAMMAP43+(VGAMMAP20-VGAMMAP43)*((32R-1R*VP27[3:0])/39R)
VGAMMAP28	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(9.6R)/(10.8R)
VGAMMAP29	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(8.4R)/(10.8R)
VGAMMAP30	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(7.2R)/(10.8R)
VGAMMAP31	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(6R)/(10.8R)
VGAMMAP31	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(4.8R)/(10.8R)
VGAMMAP33	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(3.6R)/(10.8R)
VGAMMAP34	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(2.4R)/(10.8R)

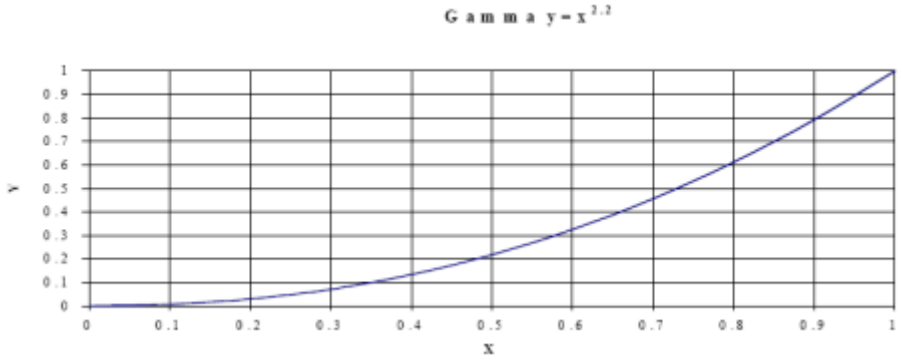
VGAMMAP35	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(1.2R)/(10.8R)
VGAMMAP36	1.2R	VGAMMAP43+(VGAMMAP20-VGAMMAP43)*((16R-1R*VP36[3:0])/39R)
VGAMMAP31	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(7.2R)/(8.4R)
VGAMMAP38	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(6R)/(8.4R)
VGAMMAP39	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(4.8R)/(8.4R)
VGAMMAP40	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(3.6R)/(8.4R)
VGAMMAP41	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(2.4R)/(8.4R)
VGAMMAP42	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(1.2R)/(8.4R)
VGAMMAP43	1.2R	VGS1+ΔVDHP(130R-1R*VP43 [6:0])/130R : VP43 [6:0] = 0~63 VGS1+ΔVDHP(129R-1R*VP43 [6:0])/130R : VP43 [6:0] = 64~127
VGAMMAP44	1R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(7.4R)/(8.4R)
VGAMMAP45	1R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(6.4R)/(8.4R)
VGAMMAP46	1.2R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(5.2R)/(8.4R)
VGAMMAP47	1.2R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(4R)/(8.4R)
VGAMMAP48	1.2R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(2.8R)/(8.4R)
VGAMMAP49	1.4R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(1.4R)/(8.4R)
VGAMMAP50	1.4R	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((40R-1R*VP50[3:0])/47R)
VGAMMAP51	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP52	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP53	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP54	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP55	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP56	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP57	variable	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((31R-1R*VP57[3:0])/47R)
VGAMMAP58	variable	VGAMMAP59+(VGAMMP57-VGAMMAP59)*JBP[1:0]
VGAMMAP59	variable	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((21R-1R*VP59[3:0])/47R)
VGAMMAP60	variable	VGAMMAP61+(VGAMMP59-VGAMMAP61)*JBP[1:0]
VGAMMAP61	variable	VGS1+ΔVDHP(65R-1R*VP61[5:0])/130R
VGAMMAP62	non	VGS1+ΔVDHP(65R-1R*VP62[5:0])/130R
VGAMMAP63	non	VGS1+ΔVDHP(23R-1R*VP63[3:0])/130R

Negative polarity	Resister stream	Gamma 64 grayscale voltage calculation formula
VGAMMAN0	non	VGS2+ΔVDHN(130R-1R*VN0[3:0])/130R
VGAMMAN1	non	VGS2+ΔVDHN(130R-1R*VN0[5:0])/130R
VGAMMAN2	non	VGS2+ΔVDHN(130R-1R*VN0[5:0])/130R
VGAMMAN3	variable	VGAMMAN4+(VGAMMN2-VGAMMAN4)*JAN[1:0]
VGAMMAN4	variable	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((40R-1R*VN4[3:0])/47R)
VGAMMAN5	variable	VGAMMAN6+(VGAMMN4-VGAMMAN6)*JAN[1:0]

VGAMMAN6	variable	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((45R-1R*VN6[4:0])/47R)
VGAMMAN7	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN8	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN9	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN10	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN11	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN12	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN13	variable	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((17R-1R*VN13[3:0])/47R)
VGAMMAN14	1.4R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(7R)/(8.4R)
VGAMMAN15	1.4R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(5.6R)/(8.4R)
VGAMMAN16	1.2R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(4.4R)/(8.4R)
VGAMMAN17	1.2R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(3.2R)/(8.4R)
VGAMMAN18	1.2R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(2R)/(8.4R)
VGAMMAN19	1R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(1R)/(8.4R)
VGAMMAN20	1R	VGS2+ΔVDHN(130R-1R*VN20 [6:0])/130R : VN20 [6:0] = 0~63 VGS2+ΔVDHN(129R-1R*VN20 [6:0])/130R : VN20 [6:0] = 64~127
VGAMMAN21	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(7.2R)/(8.4R)
VGAMMAN22	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(6R)/(8.4R)
VGAMMAN23	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(4.8R)/(8.4R)
VGAMMAN24	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(3.6R)/(8.4R)
VGAMMAN25	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(2.4R)/(8.4R)
VGAMMAN26	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(1.2R)/(8.4R)
VGAMMAN27	1.2R	VGAMMAN43+(VGAMMAN20-VGAMMAN43)*((32R-1R*VN27[3:0])/39R)
VGAMMAN28	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(9.6R)/(10.8R)
VGAMMAN29	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(8.4R)/(10.8R)
VGAMMAN30	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(7.2R)/(10.8R)
VGAMMAN31	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(6R)/(10.8R)
VGAMMAN31	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(4.8R)/(10.8R)
VGAMMAN33	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(3.6R)/(10.8R)
VGAMMAN34	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(2.4R)/(10.8R)
VGAMMAN35	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(1.2R)/(10.8R)
VGAMMAN36	1.2R	VGAMMAN43+(VGAMMAN20-VGAMMAN43)*((16R-1R*VN36[3:0])/39R)
VGAMMAN31	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(7.2R)/(8.4R)
VGAMMAN38	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(6R)/(8.4R)
VGAMMAN39	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(4.8R)/(8.4R)
VGAMMAN40	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(3.6R)/(8.4R)
VGAMMAN41	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(2.4R)/(8.4R)
VGAMMAN42	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(1.2R)/(8.4R)

VGAMMAN43	1.2R	VGS2+ΔVDHN(130R-1R*VN43 [6:0])/130R : VN43 [6:0] = 0~63 VGS2+ΔVDHN(129R-1R*VN43 [6:0])/130R : VN43 [6:0] = 64~127
VGAMMAN44	1R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(7.4R)/(8.4R)
VGAMMAN45	1R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(6.4R)/(8.4R)
VGAMMAN46	1.2R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(5.2R)/(8.4R)
VGAMMAN47	1.2R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(4R)/(8.4R)
VGAMMAN48	1.2R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(2.8R)/(8.4R)
VGAMMAN49	1.4R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(1.4R)/(8.4R)
VGAMMAN50	1.4R	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((40R-1R*VN50[3:0])/47R)
VGAMMAN51	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN52	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN53	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN54	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN55	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN56	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN57	variable	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((31R-1R*VN57[3:0])/47R)
VGAMMAN58	variable	VGAMMAN59+(VGAMMN57-VGAMMAN59)*JBN[1:0]
VGAMMAN59	variable	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((21R-1R*VN59[3:0])/47R)
VGAMMAN60	variable	VGAMMAN61+(VGAMMN59-VGAMMAN61)*JBN[1:0]
VGAMMAN61	variable	VGS2+ΔVDHN(65R-1R*VN61[5:0])/130R
VGAMMAN62	non	VGS2+ΔVDHN(65R-1R*VN62[5:0])/130R
VGAMMAN63	non	VGS2+ΔVDHN(23R-1R*VN63[3:0])/130R

15.1.1. Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$



16. Reset

16.1. Registers

The registers that are initialized are listed as below:

	After Powered On	After Hardware Reset	After Software Reset
Frame Memory	Random	No Change	No Change
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display	Off	Off	Off
Idle	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	00EF h	00EF h	If MADCTL's D5=0:00EF h If MADCTL's D5=1:013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	013F h	013F h	If MADCTL's D5 = 0:013F h If MADCTL's D5=1:00EF h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	013F h	013F h	013F h
Memory Data Access Control	00 h	00 h	No Change
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	No Change
RDDCOLMOD	06 h	06 h	06 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.

Note 2: After Powered-On Reset finishes within 10µs after both VCI *& IOVCC are applied.*

Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

16.2. Output Pins, I/O Pins

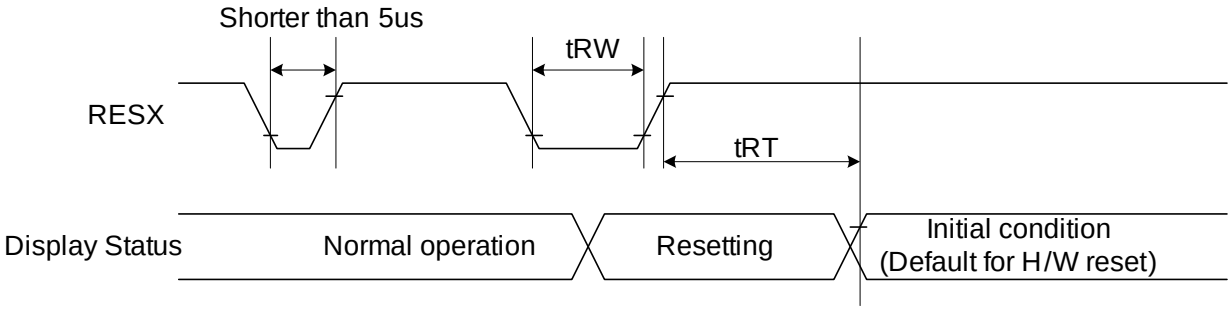
	After Power On	After Hardware Reset	After Software Reset
TE line	Low	Low	Low
DB[17:0] (output driver)	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)

Note 1: There will be no output from DB [17:0] during Power On/Off sequence, hardware reset and software reset.

16.3. Input Pins

	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See Chapter 13	Input valid	Input valid	Input valid	See Chapter 13
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
DCX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
DB[17:0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid

16.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

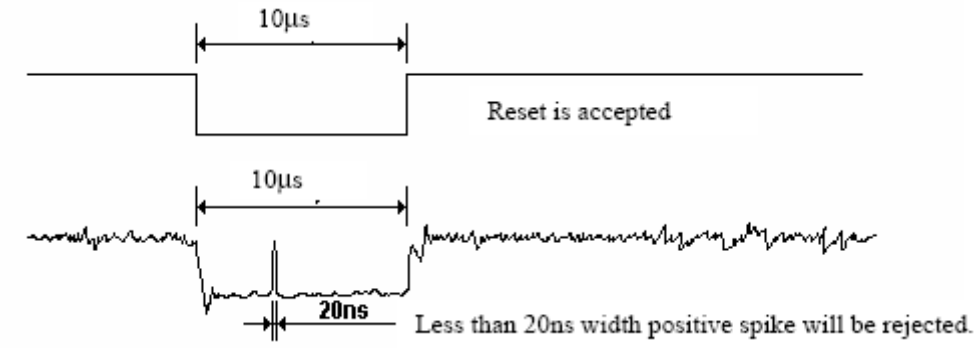
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

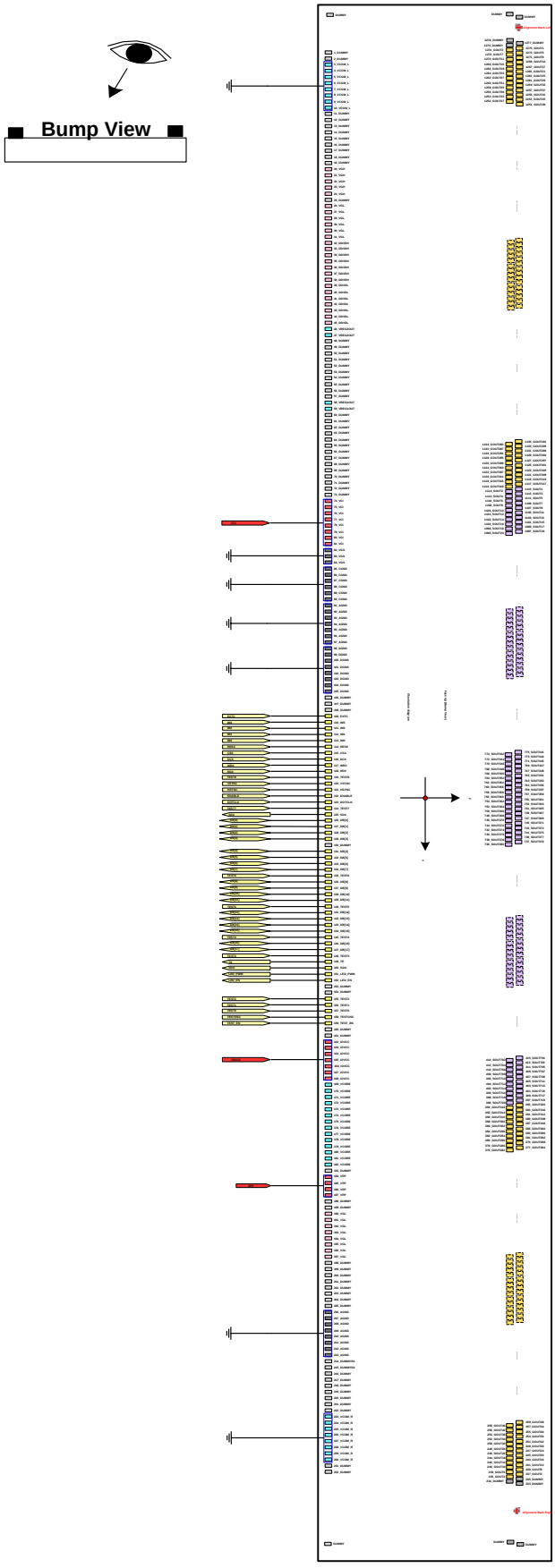


Note 5: When Reset applied during Sleep In Mode.

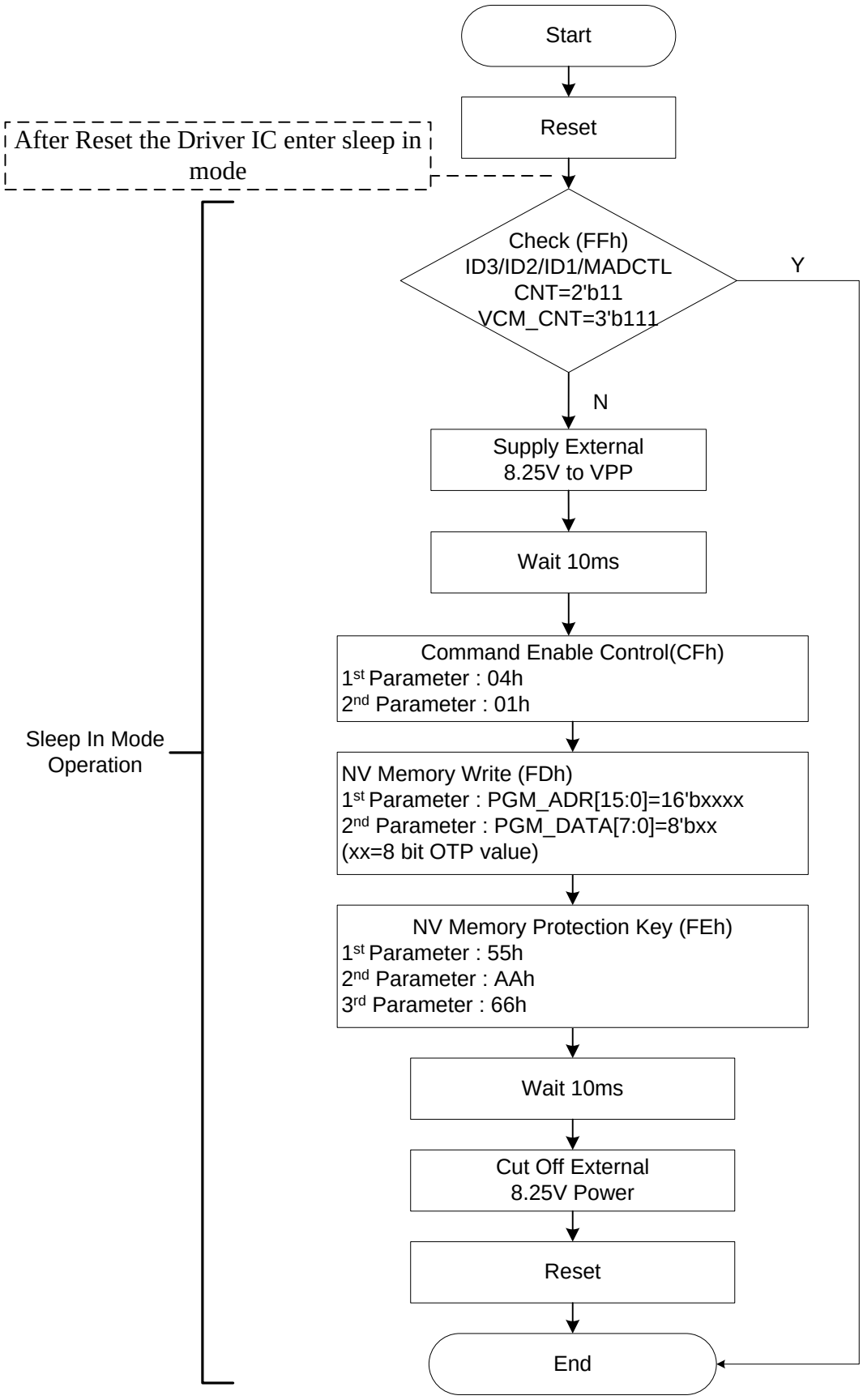
Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

17. Configuration of Power Supply Circuit



18. NV Memory Programming Flow



19. Electrical Characteristics

19.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9340X is used out of the absolute maximum ratings, ILI9340X may be permanently damaged. To use ILI9340X within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9340X will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.0
Supply voltage (Logic)	IOVCC	V	-0.3 ~ +4.0
Supply voltage (Digital)	VCORE	V	-0.3 ~ +2.0
Driver supply voltage	VGH-VGL	V	-0.3 ~ +30.0
Logic input voltage range	VIN	V	-0.3 ~ IOVCC + 0.5
Logic output voltage range	VO	V	-0.3 ~ IOVCC + 0.5
Operating temperature	Topr	℃	-40 ~ +85
Storage temperature	Tstg	℃	-40 ~ +110
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

19.2. DC Characteristics

19.2.1. General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.65	1.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	15.0	Note3
Gate Driver Low Voltage	VGL	V	-	-12.6	-	-7.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	27.6	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	GND	-	0.3*IOVCC	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	GND	-	0.2*IOVCC	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=IOVCC or GND	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM Amplitude	VCOMA	V			GND		Note3
Source Driver							
Source Output Range	Vsout	V	-	VREG2OUT	-	VREG1OUT	Note4

Note 1: IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=GND=0V, Ta=-30 to 80 ℃.

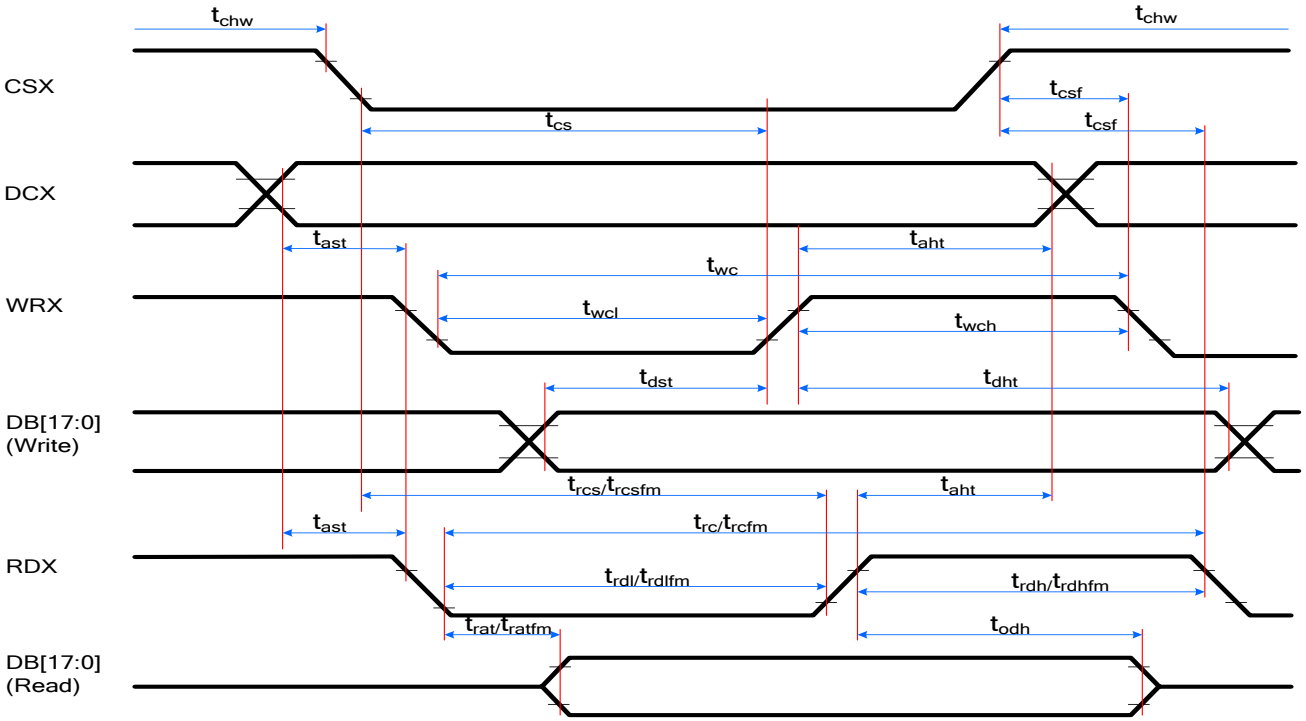
Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, DB[17:0], DCX, RESX, TE, DOTCLK, VSYNC, HSYNC, ENABLE, SDA, SCL, IM3, IM2, IM1, IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

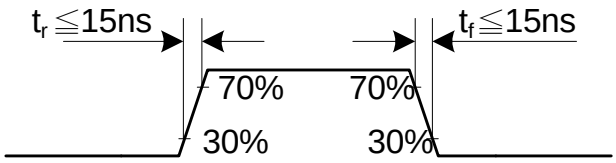
19.3. AC Characteristics

19.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ/Ⅱ system)

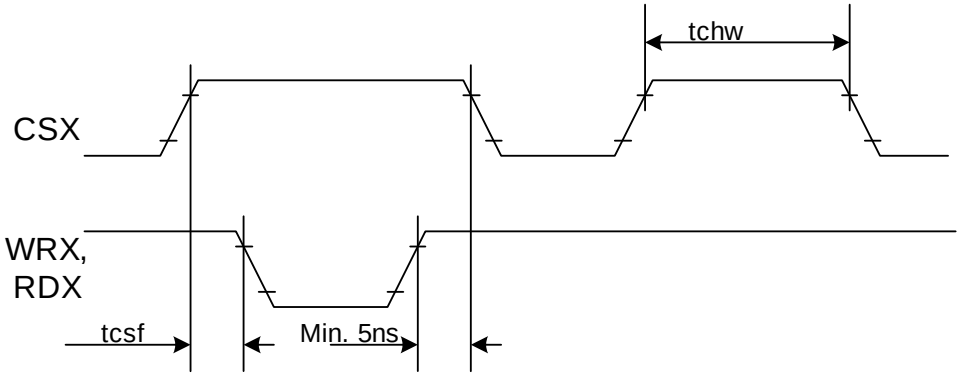


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX “H” pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB[17:0],DB[15:0], DB[8:0], DB[7:0] DB[17:10],DB[8:1] DB[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	todh	Read output disable time	20	80	ns	

Note: Ta = -30 to 80 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, GND=0V

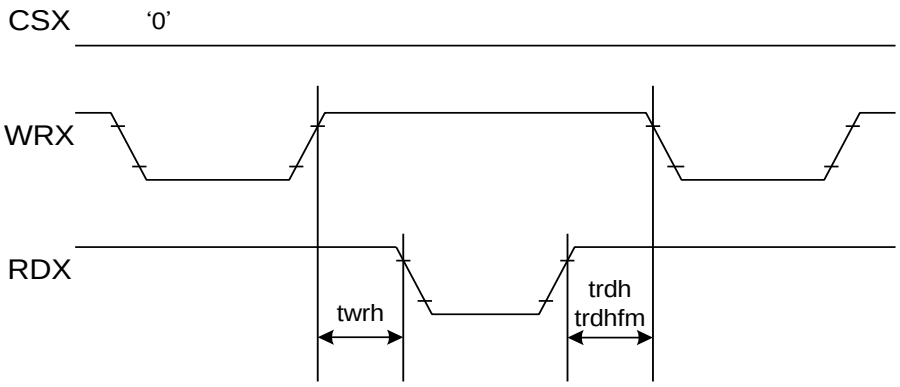


CSX timings :



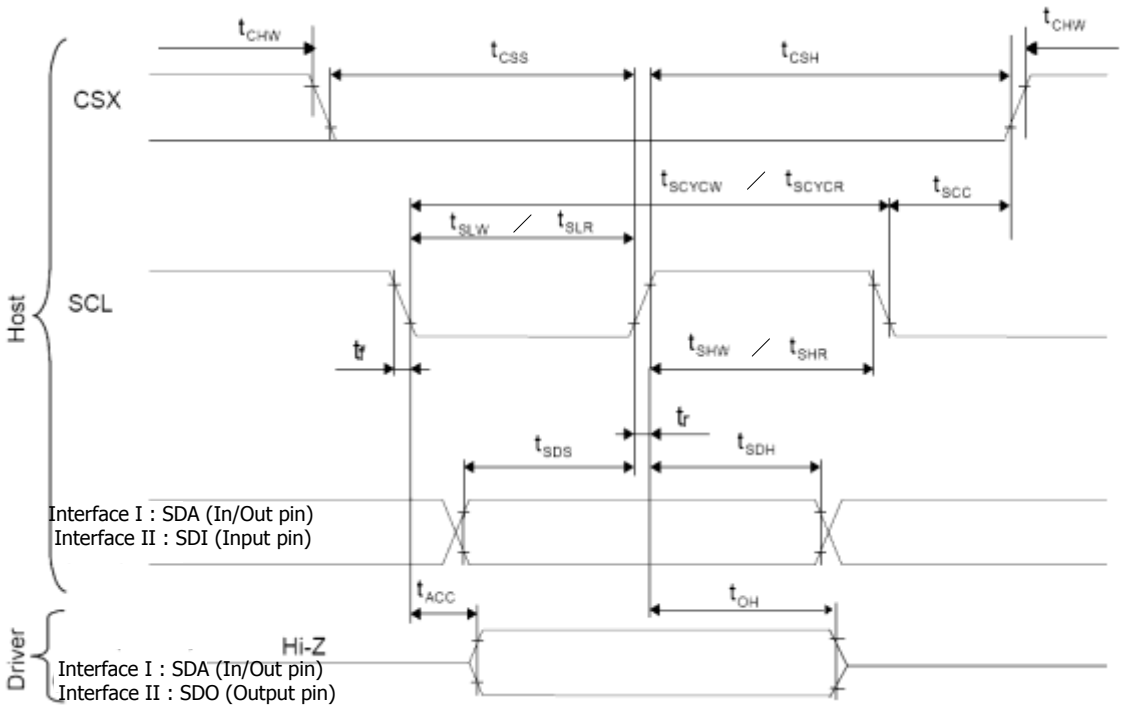
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



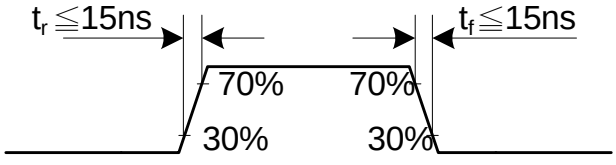
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

19.3.2. Display Serial Interface Timing Characteristics (3-line SPI system)

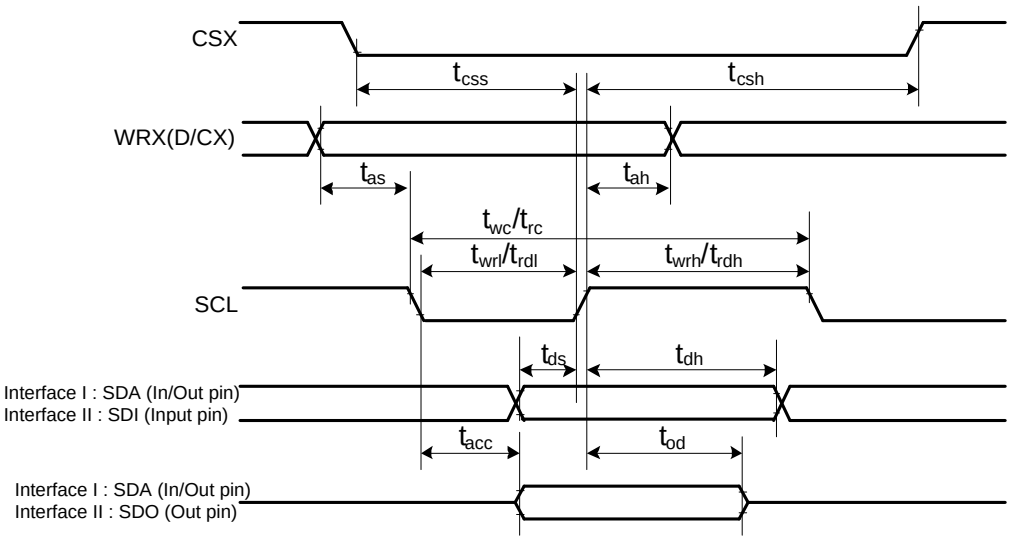


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	t_{SCYCW}	Serial Clock Cycle (Write)	66	-	ns	
	t_{SHW}	SCL “H” Pulse Width (Write)	33	-	ns	
	t_{SLW}	SCL “L” Pulse Width (Write)	33	-	ns	
	t_{SCYCW}	Serial Clock Cycle (Write RGB data)	15	-	ns	MTK-2 lane mode only
	t_{SHW}	SCL “H” Pulse Width (Write RGB data)	4	-	ns	MTK-2 lane mode only
	t_{SLW}	SCL “L” Pulse Width (Write RGB data)	4	-	ns	MTK-2 lane mode only
	t_{SCYCR}	Serial Clock Cycle (Read)	150	-	ns	
	t_{SHR}	SCL “H” Pulse Width (Read)	75	-	ns	
	t_{SLR}	SCL “L” Pulse Width (Read)	75	-	ns	
SDA / SDI (Input)	t_{SDS}	Data setup time (Write)	30	-	ns	
	t_{SDH}	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	t_{ACC}	Access time (Read)	10	-	ns	
	t_{OH}	Output disable time (Read)	10	70	ns	
CSX	t_{SCC}	SCL-CSX	20	-	ns	
	t_{CHW}	CSX “H” Pulse Width	40	-	ns	
	t_{CSS}	CSX-SCL Time(write)	15	-	ns	
	t_{CSH}		15	-	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=GND=0V

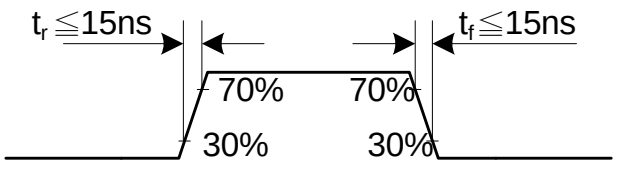


19.3.3. Display Serial Interface Timing Characteristics (4-line SPI system)

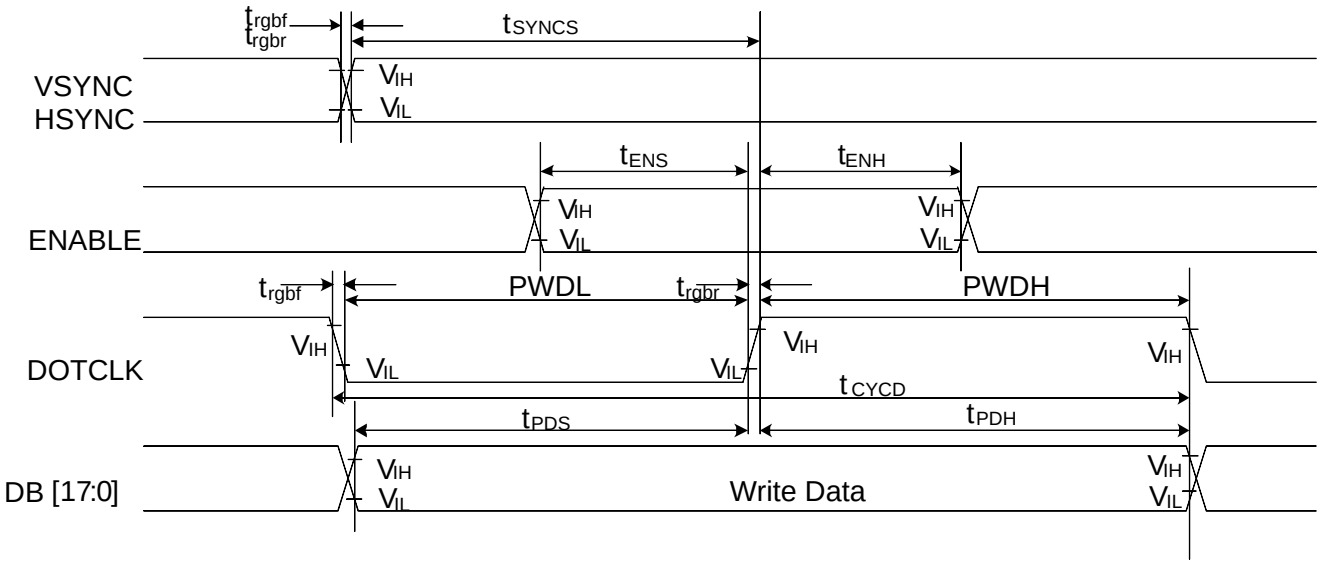


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	Chip select time (Write)	15	-	ns	
	t_{csh}	Chip select hold time (write)	15	-	ns	
SCL	t_{wc}	Serial clock cycle (Write)	66	-	ns	
	t_{wrh}	SCL “H” pulse width (Write)	33	-	ns	
	t_{wrl}	SCL “L” pulse width (Write)	33	-	ns	
	t_{wc}	Serial clock cycle (Write RGB data)	15	-	ns	MTK-2 lane mode only
	t_{wrh}	SCL “H” pulse width (Write RGB data)	4	-	ns	MTK-2 lane mode only
	t_{wrl}	SCL “L” pulse width (Write RGB data)	4	-	ns	MTK-2 lane mode only
	t_{rc}	Serial clock cycle (Read)	150	-	ns	
	t_{rdh}	SCL “H” pulse width (Read)	75	-	ns	
	t_{rdl}	SCL “L” pulse width (Read)	75	-	ns	
D/CX	t_{as}	D/CX setup time	10	-	ns	
	t_{ah}	D/CX hold time (Write / Read)	10	-	ns	
SDA / SDI (Input)	t_{ds}	Data setup time (Write)	30	-	ns	
	t_{dh}	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	t_{acc}	Access time (Read)	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t_{od}	Output disable time (Read)	10	70	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=GND=0V

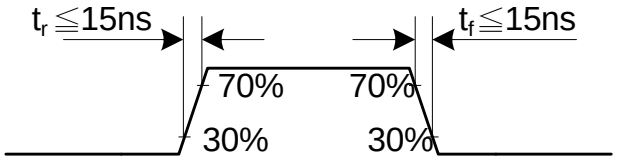


19.3.4. Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	
	PWDL	DOTCLK low-level period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time(18 bit)	66	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	25	-	ns	
	PWDL	DOTCLK low-level pulse period	25	-	ns	
	t_{CYCD}	DOTCLK cycle time (6 bit)	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time		15	ns	

Note: Ta = -30 to 80 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=GND=0V



20. Revision History

Version No.	Date	Page	Description
DTS_V100	2016/11/07	All	New Created
DTS_V101	2016/12/13	P15 P12 P200 P156 P131	P15:VSN change to DDVDL P12:LED_PWM and LED_EN change to TEST_LED1 and TEST_LED2 Test Pin add TEST_LED1 and TEST_LED2 P200:External Power 7.0V change to 8.25V P156:Add Power Control Selection Table. P131:Remove R51/R52 function